

small signal

FET design catalog

November 1982

 **Siliconix**
incorporated
The Discovery Company



small signal

FET Design Catalog November 1982

Product Status and Definitions

DATA SHEET IDENTIFICATION	PRODUCT STATUS	DEFINITION
Preliminary	First Production	Data sheet finalized and limited production quantities available. Initial reliability and characterization curves available.
No Identification Noted	Full Production	Data sheet finalized and application information available. Sampling and production order subject to product demand and manufacturing availability.

NOTE: Siliconix reserves the right to make changes at any time without notice in order to improve design and supply the best product possible

Contents

Section 1. Introduction

How to Use the FET Cross Reference and Index	1-1
FET Cross Reference and Index	1-2
Product Information	1-14
Process Option Flow Chart	1-15
Additional Product Options for European Customers	1-16
Die Process Information	1-17
PC Board Layout and Construction for Low Leakage Applications	1-18

Section 2. Data Sheets

2N2608 2N2609 (JAN)	2-1
2N3329 2N3330 2N3331 2N3332	2-2
2N3382 2N3384 2N3386	2-3
2N3819	2-4
2N3821 2N3822 2N3823	2-5
2N3824	2-6
2N3921 2N3922 2N4084 2N4085	2-7
2N3954 2N3954A 2N3955 2N3955A	2-8
2N3956 2N3957 2N3958	2-9
2N3966	2-10
2N3970 2N3971 2N3972	2-11
2N4091 2N4092 2N4093 JAN TX	2-12
2N4117 2N4117A 2N4118 2N4118A 2N4119 2N4119A	2-13
2N4220 2N4220A 2N4221 2N4221A 2N4222 2N4222A	2-14
2N4223 2N4224	2-15
2N4338 2N4339 2N4340 2N4341	2-16
2N4391 2N4392 2N4393	2-17
2N4416 2N4416A	2-18
2N4856 2N4857 2N4858 2N4859 2N4860 2N4861 JAN TX	2-19
2N4856A 2N4857A 2N4858A 2N4859A 2N4860A 2N4861A	2-20
2N4867 2N4867A 2N4868 2N4868A 2N4869 2N4869A	2-21
2N5018 2N5019	2-22
2N5045 2N5046 2N5047	2-23
2N5114 2N5115 2N5116	2-24
2N5196 2N5197 2N5198 2N5199	2-25
2N5432 2N5433 2N5434	2-26
2N5452 2N5453 2N5454	2-27
2N5457 2N5458 2N5459	2-28
2N5484 2N5485 2N5486	2-29
2N5515 2N5516 2N5517 2N5518 2N5519 2N5520 2N5521 2N5522 2N5523 2N5524	2-30
2N5545 2N5546 2N5547	2-31
2N5564 2N5565 2N5566	2-32
2N5638 2N5639 2N5640	2-33
2N5902 2N5903 2N5904 2N5905 2N5906 2N5907 2N5908 2N5909	2-34
2N5911 2N5912	2-35
3N163 3N164	2-36

Contents (Cont'd)

Section 2. Data Sheets (Cont'd)

CR022 through CR470	2-37
CRR02440 through CRR4300	2-38
DN5564 DN5565 DN5566	2-40
DN5567	2-41
DPAD1 DPAD2 DPAD5 DPAD10 DPAD20 DPAD50 DPAD100	2-42
FN4117 FN4117A FN4118 FN4118A FN4119 FN4119A	2-43
FN4392 FN4393	2-44
J105 J106 J107 J105-18 J106-18 J107-18	2-45
J111 J112 J113 J111-18 J112-18 J113-18	2-47
J174 J175 J176 J177 J174-18 J175-18 J176-18 J177-18	2-48
J201 J202 J203 J204 J201-18 J202-18 J203-18 J204-18	2-49
J210 J211 J212	2-50
J230 J231 J232 J230-18 J231-18 J232-18	2-51
J270 J271 J270-18 J271-18	2-52
J300	2-53
J304 J305	2-54
J308 J309 J310	2-55
J500 J501 J502 J503 J504 J505	2-56
J506 J507 J508 J509 J510 J511	2-57
J552	2-58
J553 J554 J555 J556 J557	2-59
JPAD5 DPAD10 JPAD20 JPAD50 JPAD100 JPAD200 JPAD500	2-60
JR135V JR170V JR200V JR220V JR240V	2-61
MFE823	2-62
MPF102	2-63
MPF108	2-64
MPF109	2-65
MPF111	2-66
MPF112	2-67
P1086 P1086-18 P1087 P1087-18	2-68
PAD1 PAD2 PAD5 PAD10 PAD20 PAD50 PAD100	2-69
PN4091 PN4092 PN4093	2-70
PN4117 PN4117A PN4118 PN4118A PN4119 PN4119A PN4120 PN4120A	2-71
PN4302 PN4303 PN4304 PN4302-18 PN4303-18 PN4304-18	2-72
PN4391 PN4392 PN4393 PN4391-18 PN4392-18 PN4393-18	2-73
PN4416	2-74
PN5163	2-75
SD210DE SD212DE SD214DE	2-76
SD211DE SD213DE SD215DE	2-78
U200 U201 U202	2-80
U231 U232 U233 U234 U235	2-81
U257	2-82
U290 U291	2-83
U304 U305 U306	2-84
U308 U309 U310	2-85

Contents (Cont'd)

Section 2. Data Sheets (Cont'd)

U311	2-86
U401 U402 U403 U404 U405 U406	2-87
U410 U411 U412	2-88
U421 U422 U423 U424 U425 U426	2-89
U427 U428	2-90
U430 U431	2-91
U440 U441 U443 U444	2-92
U1897 U1897-18 U1898 U1898-18 U1899 U1899-18	2-93
VCR2N VCR3P VCR4N VCR5P VCR7N	2-94
VCR11N	2-96

Section 3. Selector Guides

Tips on Selecting the Right FET for Your Application	3-1
Siliconix FET Application Selection Preferences	3-2
How to Choose the Correct FET for Your Application	3-4
JFET Geometry Selector Guide	
Useful JFET Information	3-6
N-Channel JFETs	3-7
P-Channel JFETs	3-8
Product Specifications	
N- and P-Channel Single JFETs	3-9
N-Channel Dual JFETs	3-15
Low Leakage Diodes	3-17
Voltage Controlled Resistors	3-17
P-Channel MOSFETs	3-17
Current Regulator Diodes	3-18

Section 4. Geometry

Useful JFET Parameter Relationships	4-1
VMRA Enhancement-Type P-Channel MOSFET	4-2
NC N-Channel JFETs	4-4
NCL N-Channel JFET Current Regulator Diode	4-7
NH N-Channel JFET	4-8
NIP N-Channel JFET	4-11
NKL N-Channel JFET Current Regulator Diode	4-13
NKM N-Channel JFET Current Regulator Diode	4-14
NKO N-Channel JFET Current Regulator Diode	4-15
NNR Monolithic Dual N-Channel JFET	4-16
NNT Monolithic Dual N-Channel JFETs	4-18
NP N-Channel JFET	4-20
NQP Monolithic Dual N-Channel JFET	4-23
NRL N-Channel JFET	4-25
NS N-Channel JFET	4-27
NT N-Channel JFET	4-29

Contents (Cont'd)

Section 4. Geometry (Cont'd)

NVA N-Channel JFET	4-31
NZA N-Channel JFET	4-32
NZF N-Channel JFET	4-34
PC P-Channel JFET	4-37
PD P-Channel JFET	4-38
PE P-Channel JFET	4-39
PS P-Channel JFET	4-40
VRMA N-Channel FET	4-42

Section 5. Application Notes

AN73-7 An Introduction to FETs	5-1
AN74-4 Audio-Frequency Noise Characteristics of Junction FETs	5-12
AN70-2 FETs for Video Amplifiers	5-20
AN81-3 Composite Op Amp for High Performance	5-28
AN72-1 FETs in Balanced Mixers	5-31
AN73-1 FETs as Voltage-Controlled Resistors	5-41
DI71-1 The FET Constant Current Source	5-50
DI71-9 Wideband UHF Amplifier with High-Performance FETs	5-52
DI73-2 High-Performance FETs in Low-Noise VHF Oscillators	5-55
TA70-2 FET Biasing	5-58
Amplifier Charts	5-66

Section 6. Appendices

Mechanical Data	6-1
Publications Index	6-3
Glossary of Terms and Abbreviations	6-5

Section 7. Other Products

Short-Form Catalog	
Introduction	7-0
Short-Form MOSPOWER Selector Guide	7-2
MOSPOWER Selector Guide	7-4
MOSPOWER Cross Reference List	7-9
MOSPOWER Commercial/Industrial Process Flow	7-18
MOSPOWER Military/Hi-Rel Process Flows	7-19
RF Power FETs Selector Guide	7-20
Analog Switches Selector Guide	7-22
Analog Switches Preferred Parts	7-25
Analog Switches Product Information	7-28
LSI/Linear Product Information	7-32
JAN38510	7-34
BS9000	7-35
Analog Switch and ICs Cross Reference Guide	7-36
Process Option Flow Charts	7-39

Section 8. Worldwide Sales Offices

Sales Offices, Representatives and Distributors	8-1
---	-----

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

How to Use the FET Cross Reference *and* Index

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. Refer to appropriate page number listed under Data Sheet or Geometry column.

Type and classification abbreviations are described as follows:

BF (JFET Plastic)	ENH (Enhancement-Mode Normally-Off)
CR (Current Limited)	JPAD (Plastic Pico Ampere Diode)
CRR (Current Limiter)	JR (Plastic High Voltage Diode)
D (Dual)	N (N-Channel)
DN (Dual N-Channel Metal Can)	P (P-Channel)
DPAD (Dual Pico Ampere Diode)	PAD (Pico Ampere Diode)
FN (N-Channel Metal Can)	SD (N-Channel DMOS)
	MOSPOWER

FET Cross Reference *and* Index

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
1N5283	CL N JFET	CR022	2-37	4-15	2N3071	N JFET	2N4338		
1N5284	CL N JFET	CR024	2-37	4-15	2N3084	N JFET	2N4341		
1N5285	CL N JFET	CR027	2-37	4-15	2N3085	N JFET	2N4341		
1N5286	CL N JFET	CR030	2-37	4-15	2N3086	N JFET	2N4341		
1N5287	CL N JFET	CR033	2-37	4-15	2N3087	N JFET	2N4341		
1N5288	CL N JFET	CR039	2-37	4-15	2N3088	N JFET	2N4339		
1N5289	CL N JFET	CR043	2-37	4-15	2N3088A	N JFET	2N4339		
1N5290	CL N JFET	CR047	2-37	4-15	2N3089	N JFET	2N4339		
1N5291	CL N JFET	CR056	2-37	4-15	2N3089A	N JFET	2N4339		
1N5292	CL N JFET	CR062	2-37	4-15	2N3113	P JFET	2N3329		
1N5293	CL N JFET	CR068	2-37	4-16	2N3277	P JFET	2N2608		
1N5294	CL N JFET	CR075	2-37	4-16	2N3278	P JFET	2N2608		
1N5295	CL N JFET	CR082	2-37	4-16	2N3328	P JFET	2N3438		
1N5296	CL N JFET	CR091	2-37	4-16	2N3329	P JFET	2N3329	2-2	4-39
1N5297	CL N JFET	CR100	2-37	4-16	2N3330	P JFET	2N3330	2-2	4-39
1N5298	CL N JFET	CR110	2-37	4-16	2N3331	P JFET	2N3331	2-2	4-39
1N5299	CL N JFET	CR120	2-37	4-16	2N3332	P JFET	2N3332	2-2	4-39
1N5300	CL N JFET	CR130	2-37	4-16	2N3365	N JFET	2N4340		
1N5301	CL N JFET	CR140	2-37	4-16	2N3366	N JFET	2N4338		
1N5302	CL N JFET	CR150	2-37	4-16	2N3367	N JFET	2N4338		
1N5303	CL N JFET	CR160	2-37	4-17	2N3368	N JFET	2N4341		
1N5304	CL N JFET	CR180	2-37	4-17	2N3369	N JFET	2N4340		
1N5305	CL N JFET	CR200	2-37	4-17	2N3370	N JFET	2N4339		
1N5306	CL N JFET	CR220	2-37	4-17	2N3376	P JFET	2N3329		
1N5307	CL N JFET	CR240	2-37	4-17	2N3378	P JFET	2N3330		
1N5308	CL N JFET	CR270	2-37	4-17	2N3380	P JFET	2N3331		
1N5309	CL N JFET	CR300	2-37	4-17	2N3382	P JFET	2N3382	2-3	4-41
1N5310	CL N JFET	CR330	2-37	4-17	2N3384	P JFET	2N3384	2-3	4-41
1N5311	CL N JFET	CR360	2-37	4-17	2N3386	P JFET	2N3386	2-3	4-41
1N5312	CL N JFET	CR390	2-37	4-17	2N3436	N JFET	2N4341		
1N5313	CL N JFET	CR430	2-37	4-17	2N3437	N JFET	2N4341		
1N5314	CL N JFET	CR470	2-37	4-17	2N3438	N JFET	2N4341		
2N2386	P JFET	2N2608			2N3452	N JFET	2N4340		
2N2386A	P JFET	2N2609			2N3453	N JFET	2N4338		
2N2497	P JFET	2N3329			2N3454	N JFET	2N4338		
2N2498	P JFET	2N3330			2N3455	N JFET	2N4340		
2N2499	P JFET	2N3331			2N3456	N JFET	2N4338		
2N2500	P JFET	2N3332			2N3457	N JFET	2N4338		
2N2601	P JFET	2N2608			2N3458	N JFET	2N4341		
2N2606JAN	P JFET	2N2608JAN			2N3459	N JFET	2N4341		
2N2607	P JFET	2N2608			2N3460	N JFET	2N4340		
2N2607JAN	P JFET	2N2608JAN			2N3574	P JFET	2N3329		
2N2608	P JFET	2N2608	2-1	4-39	2N3575	P JFET	2N3329		
2N2608JAN	P JFET	2N2608JAN	2-1	4-39	2N3578	P JFET	2N2608		
2N2609	P JFET	2N2609	2-1	4-40	2N3608	P MOS ENH	3N163		
2N2609JAN	P JFET	2N2609JAN	2-1	4-40	2N3684	N JFET	2N4339		
2N2841	P JFET	2N3329			2N3685	N JFET	2N4339		
2N2842	P JFET	2N3329			2N3686	N JFET	2N4340		
2N2843	P JFET	2N3329			2N3687	N JFET	2N4341		
2N2844	P JFET	2N2608			2N3819	N JFET	2N3819	2-4	4-10, 4-27
2N3066	N JFET	2N4340			2N3820	P JFET	J270	2-52	4-42
2N3067	N JFET	2N4338			2N3821	N JFET	2N3821	2-5	4-29
2N3068	N JFET	2N4338			2N3822	N JFET	2N3822	2-5	4-29
2N3069	N JFET	2N4341			2N3823	N JFET	2N3823	2-5	4-29
2N3070	N JFET	2N4339			2N3824	N JFET	2N3824	2-6	4-29

FET Cross Reference and Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3909	P JFET	2N2606			2N4340	N JFET	2N4340	2-16	4-22
2N3909A	P JFET	2N3909			2N4341	N JFET	2N4341	2-16	4-22
2N3921	D N JFET	2N3921	2-7	4-27	2N4352	P MOS ENH	3N163		
2N3922	D N JFET	2N3922	2-7	4-27	2N4381	P JFET	2N2609		
2N3954	D N JFET	2N3954	2-8	4-25	2N4382	P JFET	2N5115		
2N3954A	D N JFET	2N3954A	2-8	4-25	2N4391	N JFET	2N4391	2-17	4-4
2N3955	D N JFET	2N3955	2-8	4-25	2N4392	N JFET	2N4392	2-17	4-4
2N3955A	D N JFET	2N3955A	2-8	4-25	2N4393	N JFET	2N4393	2-17	4-4
2N3956	D N JFET	2N3956	2-9	4-25	2N4416	N JFET	2N4416	2-18	4-10
2N3957	D N JFET	2N3957	2-9	4-25	2N4416A	N JFET	2N4416A	2-18	4-10
2N3958	D N JFET	2N3958	2-9	4-25	2N4445	N JFET	2N5432		
2N3966	N JFET	2N3966	2-10	4-10	2N4446	N JFET	2N5433		
2N3967	N JFET	2N4221			2N4447	N JFET	2N5432		
2N3967A	N JFET	2N4221			2N4448	N JFET	2N5433		
2N3968	N JFET	2N4339			2N4856	N JFET	2N4856	2-19	4-4
2N3968A	N JFET	2N4339			2N4856A	N JFET	2N4856A	2-20	4-4
2N3969	N JFET	2N4339			2N4856JAN	N JFET	2N4856JAN		
2N3969A	N JFET	2N3686			2N4856JANTX	N JFET	2N4856JANTX	2-19	4-4
2N3970	N JFET	2N3970	2-11	4-4	2N4856JANTXV	N JFET	2N4856JANTXV		
2N3971	N JFET	2N3971	2-11	4-4	2N4857	N JFET	2N4857	2-19	4-4
2N3972	N JFET	2N3972	2-11	4-4	2N4857A	N JFET	2N4857A	2-20	4-4
2N3993	P JFET	2N3386			2N4857JAN	N JFET	2N4857JAN		
2N3993A	P JFET	2N3386			2N4857JANTX	N JFET	2N4857JANTX	2-19	4-4
2N3994	P JFET	2N3382			2N4857JANTXV	N JFET	2N4857JANTXV		
2N3994A	P JFET	2N3382			2N4858	N JFET	2N4858	2-19	4-4
2N4084	D N JFET	2N4084	2-7	4-27	2N4858A	N JFET	2N4858A	2-20	4-4
2N4085	D N JFET	2N4085	2-7	4-27	2N4858JAN	N JFET	2N4858JAN		
2N4091	N JFET	2N4091	2-12	4-4	2N4858JANTX	N JFET	2N4858JANTX	2-19	4-4
2N4091A	N JFET	2N4091			2N4858JANTXV	N JFET	2N4858JANTXV		
2N4092	N JFET	2N4092	2-12	4-4	2N4859	N JFET	2N4859	2-19	4-4
2N4092A	N JFET	2N4092			2N4859A	N JFET	2N4859A	2-20	4-4
2N4093	N JFET	2N4093	2-12	4-4	2N4859JAN	N JFET	2N4859JAN		
2N4093A	N JFET	2N4093			2N4859JANTX	N JFET	2N4859JANTX	2-19	4-4
2N4117	N JFET	2N4117	2-13	4-31	2N4859JANTXV	N JFET	2N4859JANTXV		
2N4117A	N JFET	2N4117A	2-13	4-31	2N4860	N JFET	2N4860	2-19	4-4
2N4118	N JFET	2N4118	2-13	4-31	2N4860A	N JFET	2N4860A	2-20	4-4
2N4118A	N JFET	2N4118A	2-13	4-31	2N4860JAN	N JFET	2N4860JAN		
2N4119	N JFET	2N4119	2-13	4-31	2N4860JANTX	N JFET	2N4860JANTX	2-19	4-4
2N4119A	N JFET	2N4119A	2-13	4-31	2N4860JANTXV	N JFET	2N4860JANTXV		
2N4120	P MOS ENH	3N163			2N4861	N JFET	2N4861	2-19	4-4
2N4139	N JFET	2N3822			2N4861A	N JFET	2N4861A	2-20	4-4
2N4220	N JFET	2N4220	2-14	4-27	2N4861JAN	N JFET	2N4861JAN		
2N4220A	N JFET	2N4220A	2-14	4-27	2N4861JANTX	N JFET	2N4861JANTX		
2N4221	N JFET	2N4221	2-14	4-27	2N4861JANTXV	N JFET	2N4861JANTXV		
2N4221A	N JFET	2N4221A	2-14	4-27	2N4867	N JFET	2N4867	2-21	4-31
2N4222	N JFET	2N4222	2-14	4-27	2N4867A	N JFET	2N4867A	2-21	4-29
2N4222A	N JFET	2N4222A	2-14	4-27	2N4868	N JFET	2N4868	2-21	4-29
2N4223	N JFET	2N4223	2-15	4-27	2N4868A	N JFET	2N4868A	2-21	4-29
2N4224	N JFET	2N4224	2-15	4-27	2N4869	N JFET	2N4869	2-21	4-29
2N4267	P MOS ENH	3N163			2N4869A	N JFET	2N4869A	2-21	4-29
2N4302	N JFET	PN4302-18			2N4977	N JFET	2N5432		
2N4303	N JFET	PN4303-18			2N4978	N JFET	2N5433		
2N4304	N JFET	PN4304-18			2N4979	N JFET	2N5434		
2N4338	N JFET	2N4338	2-16	4-22	2N5018	P JFET	2N5018	2-22	4-42
2N4339	N JFET	2N4339	2-16	4-22	2N5019	P JFET	2N5019	2-22	4-42

FET Cross Reference *and* Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5020	P JFET	2N3329			2N5484	N JFET	2N5484	2-29	4-10
2N5021	P JFET	2N2608			2N5485	N JFET	2N5485	2-29	4-10
2N5033	P JFET	2N2608			2N5486	N JFET	2N5486	2-29	4-10
2N5045	D N JFET	2N5045	2-23	4-25	2N5515	D N JFET	2N5515	2-30	4-29, 4-18
2N5046	D N JFET	2N5046	2-23	4-25	2N5516	D N JFET	2N5516	2-30	4-29, 4-18
2N5047	D N JFET	2N5047	2-23	4-25	2N5517	D N JFET	2N5517	2-30	4-29, 4-18
2N5103	N JFET	2N4416			2N5518	D N JFET	2N5518	2-30	4-29, 4-18
2N5104	N JFET	2N4416			2N5519	D N JFET	2N5519	2-30	4-29, 4-18
2N5105	N JFET	2N4416			2N5520	D N JFET	2N5520	2-30	4-29, 4-18
2N5114	P JFET	2N5114	2-24	4-42	2N5521	D N JFET	2N5521	2-30	4-29, 4-18
2N5115	P JFET	2N5115	2-24	4-42	2N5522	D N JFET	2N5522	2-30	4-29, 4-18
2N5116	P JFET	2N5116	2-24	4-42	2N5523	D N JFET	2N5523	2-30	4-29, 4-18
2N5158	N JFET	2N5434			2N5524	D N JFET	2N5524	2-30	4-29, 4-18
2N5159	N JFET	2N5433			2N5545	D N JFET	2N5545	2-31	4-25
2N5196	D N JFET	2N5196	2-25	4-25	2N5546	D N JFET	2N5546	2-31	4-25
2N5197	D N JFET	2N5197	2-25	4-25	2N5547	D N JFET	2N5547	2-31	4-25
2N5198	D N JFET	2N5198	2-25	4-25	2N5549	N JFET	2N4392		
2N5199	D N JFET	2N5199	2-25	4-25	2N5561	D N JFET	U401		
2N5245	N JFET	PN4416			2N5562	D N JFET	U402		
2N5246	N JFET	J305-18			2N5563	D N JFET	U404		
2N5247	N JFE	J304-18			2N5564	D N JFET	2N5564	2-32	4-4
2N5248	N JFET	2N5486			2N5565	D N JFET	2N5565	2-32	4-4
2N5257	N JFET	2N5457			2N5566	D N JFET	2N5566	2-32	4-4
2N5258	N JFET	2N5458			2N5592	N JFET	2N3822		
2N5259	N JFET	2N5459			2N5593	N JFET	2N3822		
2N5265	P JFET	2N2608			2N5594	N JFET	2N3822		
2N5266	P JFET	2N2608			2N5638	N JFET	2N5638	2-33	4-4
2N5267	P JFET	2N2608			2N5639	N JFET	2N5639	2-33	4-4
2N5268	P JFET	2N2608			2N5640	N JFET	2N5640	2-33	4-4
2N5269	P JFET	2N3331			2N5647	N JFET	2N4117A		
2N5270	P JFET	2N3331			2N5648	N JFET	2N4117A		
2N5358	N JFET	2N4340			2N5649	N JFET	2N4117A		
2N5359	N JFET	2N4340			2N5797	P JFET	2N2608		
2N5360	N JFET	2N4339			2N5798	P JFET	2N2608		
2N5361	N JFET	2N4339			2N5799	P JFET	2N2608		
2N5362	N JFET	2N4339			2N5800	P JFET	2N2608		
2N5363	N JFET	2N4222A			2N5801	N JFET	2N4393		
2N5364	N JFET	2N4224			2N5802	N JFET	2N4393		
2N5391	N JFET	2N4867A			2N5803	N JFET	2N4392		
2N5392	N JFET	2N4868A			2N5902	D N JFET	2N5902	2-34	4-23
2N5393	N JFET	2N4869A			2N5903	D N JFET	2N5903	2-34	4-23
2N5394	N JFET	2N4869A			2N5904	D N JFET	2N5904	2-34	4-23
2N5395	N JFET	2N4869A			2N5905	D N JFET	2N5905	2-34	4-23
2N5396	N JFET	2N4869A			2N5906	D N JFET	2N5906	2-34	4-23
2N5397	N JFET	U310			2N5907	D N JFET	2N5907	2-34	4-23
2N5398	N JFET	U312			2N5908	D N JFET	2N5908	2-34	4-23
2N5432	N JFET	2N5432	2-26	4-13	2N5909	D N JFET	2N5909	2-34	4-23
2N5433	N JFET	2N5433	2-26	4-13	2N5911	D N JFET	2N5911	2-35	4-36
2N5434	N JFET	2N5434	2-26	4-13	2N5912	D N JFET	2N5912	2-35	4-36
2N5452	D N JFET	2N5452	2-27	4-25	2N5949	N JFET	PN4416		
2N5453	D N JFET	2N5453	2-27	4-25	2N5950	N JFET	PN4416		
2N5454	D N JFET	2N5454	2-27	4-25	2N5951	N JFET	PN4416		
2N5457	N JFET	2N5457	2-28	4-27	2N5952	N JFET	J305		
2N5458	N JFET	2N5458	2-28	4-27	2N5953	N JFET	J305		
2N5459	N JFET	2N5459	2-28	4-27	2N6451	N JFET	2N4393		
					2N6452	N JFET	2N4393		

FET Cross Reference and Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N6453	N JFET	2N4393			202S	N JFET	2N4392		
2N6454	N JFET	2N4393			203S	N JFET	2N3821		
2N6483	D N JFET	U401			204S	N JFET	2N3821		
2N6484	D N JFET	U402			210U	N JFET	2N4416		
2N6585	D N JFET	U404			231S	D N JFET	2N3954		
2N6568	N JFET	U290			232S	D N JFET	2N3955		
2N6656	V MOS N ENH	2N6656			233S	D N JFET	2N3956		
2N6657	V MOS N ENH	2N6657			234S	D N JFET	2N3957		
2N6658	V MOS N ENH	2N6658			235S	D N JFET	2N3958		
2N6659	V MOS N ENH	2N6659			241U	N JFET	2N4869		
2N6660	V MOS N ENH	2N6660			250U	N JFET	2N4091		
2N6661	V MOS N ENH	2N6661			251U	N JFET	2N4392		
3N145	P MOS ENH	3N163			703U	N JFET	2N4220		
3N146	P MOS ENH	3N163			704U	N JFET	2N4220		
3N155	P MOS ENH	3N163			705U	N JFET	2N4224		
3N155A	P MOS ENH	3N163			707U	N JFET	2N4860		
3N156	P MOS ENH	3N163			714U	N JFET	2N3822		
3N156A	P MOS ENH	3N163			734U	N JFET	2N4416		
3N157	P MOS ENH	3N163			734EU	N JFET	PN4416		
3N157A	P MOS ENH	3N163			751U	N JFET	2N4340		
3N158	P MOS ENH	3N163			752U	N JFET	2N4340		
3N158A	P MOS ENH	3N163			753U	N JFET	2N4341		
3N163	P MOS ENH	3N163	2-36	4-2	754U	N JFET	2N4340		
3N164	P MOS ENH	3N164	2-36	4-2	755U	N JFET	2N4341		
3N174	P MOS ENH	3N163			756U	N JFET	2N4340		
14T	N JFET	2N3819			1277A	N JFET	2N3822		
142T	N JFET	PN4392			1278A	N JFET	2N3821		
158T	N JFET	PN4302			1279A	N JFET	2N3821		
159T	N JFET	PN4416			1280A	N JFET	2N4224		
100S	N JFET	PN4304			1281A	N JFET	2N3822		
100U	N JFET	2N3684			1282A	N JFET	2N4341		
102M	N JFET	2N5486			1283A	N JFET	2N4340		
102S	N JFET	2N4302			1284A	N JFET	2N4222		
103M	N JFET	2N5457			1285A	N JFET	2N3821		
103S	N JFET	2N5459			1286A	N JFET	2N4220		
104M	N JFET	2N5458			1325A	N JFET	2N4222		
105M	N JFET	2N5459			1714A	N JFET	2N4340		
105U	N JFET	2N4222			2000M	N JFET	2N3823		
106M	N JFET	2N5485			2001M	N JFET	2N3823		
107M	N JFET	2N5486			2078A	D N JFET	2N3955		
110U	N JFET	2N4339			2079A	D N JFET	2N3955		
115U	N JFET				2080A	D N JFET	2N5546		
120U	N JFET	2N4340			2081A	D N JFET	2N5546		
125U	N JFET	2N4339			2093M	N JFET	2N3687		
130U	N JFET	2N4341			2094M	N JFET	2N3686		
135U	N JFET	2N4339			2095M	N JFET	2N3686		
155U	N JFET	2N4416			2098A	D NJFET	2N5545		
182S	N JFET	2N4391			2099A	D N JFET	2N5546		
183S	N JFET	2N3823			2130U	D N JFET	2N5452		
197S	N JFET	2N4338			2132U	D N JFET	2N3955		
198S	N JFET	2N4340			2134U	D N JFET	2N3956		
199S	N JFET	2N4341			2136U	D N JFET	2N3957		
200S	N JFET	2N4392			2138U	D N JFET	2N3958		
200U	N JFET	2N3824			2139U	D N JFET	2N3958		
201S	N JFET	2N4391			2147U	D N JFET	2N3958		

FET Cross Reference *and* Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2148U	D N JFET	2N3958			BFW56	N JFET	2N4869		
2149U	D N JFET	2N3958			BFW61	N JFET	2N4224		
A5T3821	N JFET	J305			BSV22	N JFET	2N4416		
A5T3822	N JFET	J305			BSV78	N JFET	2N4856A		
A5T3823	N JFET	PN4416			BSV80	N JFET	2N4858A		
A5T3824	N JFET	J302-18			C413N	N JFET	2N5434		
A192	N JFET	2N4416			C673	N JFET	2N4341		
AD830	D N JFET	U421			C674	N JFET	2N4341		
AD831	D N JFET	U421			C680	N JFET	2N4338		
AD832	D N JFET	U422			C680A	N JFET	2N4338		
AD833	D N JFET	U426			C681	N JFET	2N4338		
AD833A	D N JFET	U423			C681A	N JFET	2N4338		
AD835	D N JFET	2N3921			C682	N JFET	2N4339		
AD836	D N JFET	2N3921			C682A	N JFET	2N4339		
AD837	D N JFET	2N3922			C683	N JFET	2N4339		
AD838	D N JFET	2N4085			C683A	N JFET	2N4339		
AD839	D N JFET	2N4085			C684	N JFET	2N4220		
AD840	D N JFET	2N5196			C684A	N JFET	2N4220		
AD841	D N JFET	2N5197			C685	N JFET	2N4220		
AD842	D N JFET	2N5199			C685A	N JFET	2N4220		
AD3954	D N JFET	2N3954			C6690	N JFET	2N4341		
AD3954A	D N JFET	2N3954A			C6691	N JFET	2N4341		
AD3955	D N JFET	2N3955			C6692	N JFET	2N4340		
AD3956	D N JFET	2N3956			CM600	N JFET	2N4092		
AD3957	D N JFET	2N3957			CM601	N JFET	2N4091		
AD3958	D N JFET	2N3958			CM602	N JFET	2N4091		
BC264	N JFET	PN4304			CM603	N JFET	2N4091		
BC264A	N JFET	PN4302			CM640	N JFET	2N4093		
BC264B	N JFET	PN4304			CM641	N JFET	2N4093		
BC264C	N JFET	PN4304			CM642	N JFET	2N4093		
BC264D	N JFET	PN4416			CM643	N JFET	2N4092		
BF244A/B/C*	N JFET	*Contact factory			CM644	N JFET	2N4092		
BF245A/B/C*	D N JFET	*Contact factory			CM645	N JFET	2N4092		
BFR45	D N JFET	2N4416			CM646	N JFET	2N4092		
BFS21	N JFET	2N5199			CM647	N JFET	2N4091		
BFS21A	D N JFET	2N5199			CM650	N JFET	2N5432		
BFS67	N JFET	2N3821			CM651	N JFET	2N5433		
BFS67P	N JFET	2N4303			CM652	N JFET	2N5432		
BFS68	N JFET	2N3823			CM653	N JFET	2N5433		
BFS68P	N JFET	PN4416			CM697	N JFET	2N5434		
BFS70	N JFET	2N3821			CM800	N JFET	2N5434		
BFS71	N JFET	2N3822			CMX740	N JFET	U290		
BFS72	N JFET	2N3823			CP640	N JFET	U296		
BFS73	N JFET	2N3821			CP643	N JFET	2N5434		
BFS74	N JFET	2N4856			CP650	N JFET	U322		
BFS75	N JFET	2N4857			CP651	N JFET	U320		
BFS76	N JFET	2N4858			CP652	N JFET	U322		
BFS77	N JFET	2N4859			CP653	N JFET	U320		
BFS78	N JFET	2N4860			CR022 Thru CR470 Referenced Under 1N Series				
BFS79	N JFET	2N4861			CRR0240-4300	CL N FET	CRR0240-4300	2-38	
BFS80	N JFET	2N4416A			DN5564-66	D N JFET	DN5564-66	2-40	4-4
BFW10	N JFET	2N3823			DN5567	D N JFET	DN5567	2-41	4-4
BFW11	N JFET	2N3822			DPAD1	D PAD N JFET	DPAD1	2-42	
BFW54	N JFET	2N3822			DPAD2	D PAD N JFET	DPAD2	2-42	
BFW55	N JFET	2N3822			DPAD5	D PAD N JFET	DPAD5	2-42	

FET Cross Reference and Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
DPAD10	D PAD N JFET	DPAD10	2-42		E500	CL N JFET	J500		
DPAD20	D PAD N JFET	DPAD20	2-42		E501	CL N JFET	J501		
DPAD50	D PAD N JFET	DPAD50	2-42		E502	CL N JFET	J502		
DPAD100	D PAD N JFET	DPAD100	2-42		E503	CL N JFET	J503		
DU4339	D N JFET	U235			E504	CL N JFET	J504		
DU4340	D N JFET	U235			E505	CL N JFET	J505		
E100	N JFET	J203-18			E506	CL N JFET	J506		
E101	N JFET	J201-18			E507	CL N JFET	J507		
E102	N JFET	J202-18			EPAD50	DD N JFET	JPAD50		
E103	N JFET	J105-18			EPAD100	DD N JFET	JPAD100		
E105	N JFET	J105-18			EPAD200	DD N JFET	JPAD200		
E106	N JFET	J106-18			EPAD500	DD N JFET	JPAD500		
E107	N JFET	J107-18			FE100	N JFET	2N3821		
E108	N JFET	J108-18			FE100A	N JFET	2N3821		
E109	N JFET	J109-18			FE102	N JFET	2N4119		
E110	N JFET	J110-18			FE102A	N JFET	2N4119		
E111	N JFET	J111-18			FE104	N JFET	2N4118		
E112	N JFET	J112-18			FE104A	N JFET	2N4118		
E113	N JFET	J113-18			FE200	N JFET	2N3821		
E114	N JFET	J114			FE202	N JFET	2N3821		
E174	P JFET	J174-18			FE204	N JFET	2N3821		
E175	P JFET	J175-18			FE300	N JFET	2N3822		
E176	P JFET	J176-18			FE302	N JFET	2N3821		
E177	P JFET	J177-18			FE304	N JFET	2N3821		
E201	N JFET	J201-18			FE0654A	N JFET	2N5486		
E202	N JFET	J202-18			FE0654B	N JFET	2N5485		
E203	N JFET	J203-18			FE3819	N JFET	2N3819		
E204	N JFET	J204-18			FE5457	N JFET	2N5457		
E210	N JFET	J210			FE5458	N JFET	2N5458		
E211	N JFET	J211			FE5459	N JFET	2N5459		
E212	N JFET	J212			FE5484	N JFET	2N5484		
E230	N JFET	J230-18			FE5485	N JFET	2N5485		
E231	N JFET	J231-18			FE5486	N JFET	2N5486		
E232	N JFET	J232-18			FM3954	D N JFET	2N3954		
E270	P JFET	J270-18			FM3954A	D N JFET	2N3954A		
E271	P JFET	J271-18			FM3955	D N JFET	2N3955		
E300	N JFET	J300			FM3955A	D N JFET	2N3955A		
E304	N JFET	J304			FM3956	D N JFET	2N3956		
E305	N JFET	J305			FM3957	D N JFET	2N3957		
E308	N JFET	J308			FM3958	D N JFET	2N3958		
E309	N JFET	J309			FN4117	N J FET	FN4117	2-43	4-31
E310	N JFET	J310			FN4117A	N J FET	FN4117A	2-43	4-31
E400	D N JFET	U410			FN4118	N J FET	FN4118	2-43	4-31
E401	D N JFET	U411			FN4118A	N J FET	FN4118A	2-43	4-31
E402	D N JFET	U410			FN4119	N J FET	FN4119	2-43	4-31
E410	D N JFET	U410			FN4119A	N J FET	FN4119A	2-43	4-31
E411	D N JFET	U411			FN4392	N J FET	FN4392	2-44	4-4
E412	D N JFET	U412			FN4393	N J FET	FN4393	2-44	4-4
E413	D N JFET	U410			FT0654A	N JFET	2N5486		
E414	D N JFET	U411			FT0654B	N JFET	2N5486		
E415	D N JFET	U412			FT0654C	N JFET	2N4221		
E420	D N JFET	U440			FT0654D	N JFET	2N4221		
E421	D N JFET	U441			FT0654D	N JFET	2N4221		
E430	D N JFET	U430			FT704	P MOS ENH	3N163		
E431	D N JFET	U431							

FET Cross Reference *and* Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
GET5457	N JFET	2N5457			J110	N JFET	J110	2-46	4-13
GET5458	N JFET	2N5458			J110-18	N JFET	J110-18	2-46	4-13
GET5459	N JFET	2N5459			J111	N JFET	J111	2-47	4-4
HDIG1030	P MOS ENH	3N163			J111-18	N JFET	J111-18	2-47	4-4
ID100	D PAD N JFET	DPAD1			J112	N JFET	J112	2-47	4-4
ID101	D PAD N JFET	DPAD10			J112-18	N JFET	J112-18	2-47	4-4
IMF3954	D N JFET	2N3954			J113	N JFET	J113	2-47	4-4
IMF3954A	D N JFET	2N3954A			J113-18	N JFET	J113-18	2-47	4-4
IMF3955	D N JFET	2N3955			J174	P JFET	J174	2-48	4-42
IMF3955A	D N JFET	2N3955A							
IMF3956	D N JFET	2N3956			J174-18	P JFET	J174-18	2-48	4-42
IMF3957	D N JFET	2N3957			J175	P JFET	J175	2-48	4-42
IMF3958	D N JFET	2N3958			J175-18	P JFET	J175-18	2-48	4-42
IMF6485	D N JFET	U405			J176	P JFET	J176	2-48	4-42
IT100	P JFET	2N5116			J176-18	P JFET	J176-18	2-48	4-42
IT101	P JFET	2N5114			J177	P JFET	J177	2-48	4-42
IT108	N JFET	2N5486			J177-18	P JFET	J177-18	2-48	4-42
IT109	N JFET	U310			J201	N JFET		2-49	4-23
IT1700	P MOS ENH	3N163			J201-18	N JFET		2-49	4-23
IT1702	P MOSENH	3N163			J202	N JFET		2-49	4-23
ITE500	CL N JFET	J500			J202-18	N JFET		2-49	4-23
ITE501	CL N JFET	J501			J203	N JFET		2-49	4-23
ITE502	CL N JFET	J502			J203-18	N JFET		2-49	4-23
ITE503	CL N JFET	J503			J204	N JFET	J204	2-49	4-23
ITE504	CL N JFET	J504			J204-18	N JFET	J204-18	2-49	4-23
ITE505	CL N JFET	J505			J210	N JFET	J210	2-50	4-36
ITE506	CL N JFET	J506			J211	N JFET	J211	2-50	4-36
ITE507	CL N JFET	J507			J212	N JFET	J212	2-50	4-36
ITE3066	N JFET	J202-18			J230	N JFET	J230	2-51	4-29, 13
ITE3067	N JFET	J201-18			J230-18	N JFET	J230-18	2-51	4-29, 13
ITE3068	N JFET	J201-18			J231	N JFET	J231	2-51	4-29, 13
ITE4117	N JFET	2N4117			J231-18	N JFET	J231-18	2-51	4-29, 13
ITE4118	N JFET	2N4118			J232	N JFET	J232	2-51	4-29, 13
ITE4119	N JFET	2N4119			J232-18	N JFET	J232-18	2-51	4-29, 13
ITE4338	N JFET	J201-18			J270	P JFET	J270	2-52	4-29, 13
ITE4339	N JFET	J201-18			J270-18	P JFET	J270-18	2-52	4-42
ITE4340	N JFET	J202-18			J271	P JFET	J271	2-52	4-42
ITE4341	N JFET	J203-18			J271-18	P JFET	J271-18	2-52	4-42
ITE4391	N JFET	PN4391-18			J300	N JFET	J300	2-53	4-37
ITE4392	N JFET	PN4392-18			J300A/B/C/D	N JFET	J300A/B/C/D	2-53	4-37
ITE4393	N JFET	PN4393-18			J304	N JFET	J304	2-54	4-10
ITE4416	N JFET	PN4416			J305	N JFET	J305	2-54	4-10
ITE4867	N JFET	J230-18			J308	N JFET	J308	2-55	4-34
ITE4868	N JFET	J231-18			J309	N JFET	J309	2-55	4-34
ITE4869	N JFET	J232-18			J310	N JFET	J310	2-55	4-34
J105	N JFET	J105	2-45	4-33	J401	D N JFET	U401		
J105-18	N JFET	J105-18	2-45	4-33	J402	D N JFET	U402		
J106	N JFET	J106	2-45	4-33	J403	D N JFET	U403		
J106-18	N JFET	J106-18	2-45	4-33	J404	D N JFET	U404		
J107	N JFET	J107	2-45	4-33	J405	D N JFET	U405		
J107-18	N JFET	J107-18	2-45	4-33	J406	D N JFET	U406		
J108	N JFET	J108	2-46	4-13	J410	D N JFET	U410		
J108-18	N JFET	J108-18	2-46	4-13	J411	D N JFET	U411		
J109	N JFET	J109	2-46	4-13	J412	D N JFET	U412		
J109-18	N JFET	J109-18	2-46	4-13	J500	CL N JFET	J500	2-56	4-7
					J501	CL N JFET	J501	2-56	4-7

FET Cross Reference *and* Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J502	CL N JFET	J502	2-56	4-7	KE4416	N JFET	PN4416		
J503	CL N JFET	J503	2-56	4-7	KE4856	N JFET	PN4391-18		
J504	CL N JFET	J504	2-56	4-7	KE4857	N JFET	PN4392-18		
J505	CL N JFET	J505	2-56	4-7	KE4858	N JFET	PN4393-18		
J506	CL N JFET	J506	2-57	4-7	KE4859	N JFET	PN4391-18		
J507	CL N JFET	J507	2-57	4-7	KE4860	N JFET	PN4392-18		
J508	CL N JFET	J508	2-57	4-7	KE4861	N JFET	PN4393-18		
J509	CL N JFET	J509	2-57	4-7	KE5103	N JFET	J305		
J510	CL N JFET	J510	2-57	4-7	KE5104	N JFET	J304		
J511	CL N JFET	J511	2-57	4-7	KE5105	N JFET	J306		
J552	CL N JFET	J552	2-58	4-15	KK4416-18	N JFET	PN4416		
J553	CL N JFET	J553	2-59		LDF603	N JFET	2N4221A		
J554	CL N JFET	J554	2-59		LDF604	N JFET	2N4221A		
J555	CL N JFET	J555	2-59		LDF605	N JFET	2N4221A		
J556	CL N JFET	J556	2-59		M163	P MOS ENH	3N163		
J557	CL N JFET	J557	2-59						
JPAD5	PAD N JFET	JPAD5	2-60		M164	P MOS ENH	3N164		
JPAD10	PAD N JFET	JPAD10	2-60		MEM520	P MOS ENH	3N164		
JPAD20	PAD N JFET	JPAD20	2-60		MEM520C	P MOS ENH	3N164		
JPAD50	PAD N JFET	JPAD50	2-60		MEM561	P MOS ENH	3N163		
JPAD100	PAD N JFET	JPAD100	2-60		MEM561C	P MOS ENH	3N163		
JPAD200	PAD NJFET	JPAD200	2-60						
JPAD500	PAD N JFET	JPAD500	2-60		MEM806	P MOS ENH	3N163		
JR135V	CL N JFET	JR135V	2-61		MEM806A	P MOS ENH	3N163		
JR170V	CL N JFET	JR170V	2-61		MFE823	P MOS ENH	MFE823	2-61	4-2
JR200V	CL N JFET	JR200V	2-61		MFE2000	N JFET	2N4416		
JR220V	CL N JFET	JR220V	2-61		MFE2001	N JFET	2N4416		
JR240V	CL N JFET	JR240V	2-61						
J1401	D N JFET	U401			MFE2004	N JFET	2N4093		
J1402	D N JFET	U402			MFE2005	N JFET	2N4092		
J1403	D N JFET	U403			MFE2006	N JFET	2N4091		
J1404	D N JFET	U404			MFE2007	N JFET	2N4860		
J1405	D N JFET	U405			MFE2008	N JFET	2N4859		
J1406	D N JFET	U406							
J9100	CL N JFET	J9100	2-58	4-15	MFE2009	N JFET	2N4859		
K210-18	N JFET	J210			MFE2010	N JFET	2N5434		
K211-18	N JFET	J211			MFE2011	N JFET	2N5433		
K212-18	N JFET	J212			MFE2012	N JFET	2N5432		
K300-18	N JFET	J210			MFE2093	N JFET	2N3687		
K304-18	N JFET	J304							
K305-18	N JFET	J305			MFE2094	N JFET	2N3686		
K308-18	N JFET	J308			MFE2095	N JFET	2N3685		
K309-18	N JFET	J309			MFE4007	P JFET	2N2608		
					MFE4008	P JFET	2N2608		
					MFE4009	P JFET	2N3329		
K310-18	N JFET	J310							
KE3684	N JFET	2N3684			MFE4010	P JFET	2N3330		
KE3685	N JFET	2N3685			MFE4011	P JFET	2N3330		
KE3686	N JFET	2N3686			MFE4012	P JFET	2N3331		
KE3687	N JFET	2N3687			MK10	N JFET	2N4416		
KE3823	N JFET	J304-18			MMF1	D N JFET	2N3921		
KE3970	N JFET	PN4391-18			MMF2	D N JFET	2N3921		
KE3971	N JFET	PN4392-18			MMF3	D N JFET	2N3921		
KE3972	N JFET	PN4393-18			MMF4	D N JFET	2N3921		
KE4091	N JFET	PN4391-18			MMF5	D N JFET	2N3921		
					MMF6	D N JFET	2N3921		
KE4092	N JFET	PN4392-18							
KE4093	N JFET	PN4393-18			MMT3823	N JFET	2N3823		
KE4220	N JFET	2N5457			MPF102	N JFET	MPF102	2-62	4-10
KE4221	N JFET	2N5457			MPF103	N JFET	2N5457		
KE4222	N JFET	2N5459			MPF104	N JFET	2N5458		
					MPF105	N JFET	2N5459		
KE4223	N JFET	J304-18							
KE4224	N JFET	J304-18			MPF106	N JFET	2N5485		
KE4391	N JFET	PN4391-18			MPF107	N JFET	2N5486		
KE4392	N JFET	PN4392-18			MPF108	N JFET	MPF108	2-63	4-10
KE4393	N JFET	PN4393-18			MPF109	N JFET	MPF109	2-64	4-27
					MPF111	N JFET	MPF111	2-65	4-27

FET Cross Reference and Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MPP4391	N JFET	PN4391-18			PN4093	N JFET	PN4093	2-69	4-4
MPP4392	N JFET	PN4392-18			PN4117	N JFET	PN4117	2-70	4-31
MPP4393	N JFET	PN4393-18			PN4117A	N JFET	PN4117A	2-70	4-31
NF500	N JFET	2N4416			PN4118	N JFET	PN4118	2-70	4-31
NF501	N JFET	2N4416			PN4118A	N JFET	PN4118A	2-70	4-31
NF506	N JFET	2N4416			PN4119	N JFET	PN4119	2-70	4-31
NF510	N JFET	2N4393			PN4119A	N JFET	PN4119A	2-70	4-31
NF511	N JFET	2N4393			PN4120	N JFET	PN4120	2-70	4-31
NF520	N JFET	2N4339			PN4120A	N JFET	PN4120A	2-70	4-31
NF521	N JFET	2N4339			PN4302	N JFET	PN4302	2-71	4-22
NF522	N JFET	2N4339			PN4302-18	N JFET	PN4302-18	2-71	4-22
NF523	N JFET	2N4340			PN4303	N JFET	PN4303	2-71	4-22
NF530	N JFET	2N4341			PN4303-18	N JFET	PN4303-18	2-71	4-22
NF531	N JFET	2N4339			PN4304	N JFET	PN4304	2-71	4-22
NF532	N JFET	2N4341			PN4304-18	N JFET	PN4304-18	2-71	4-22
NF533	N JFET	2N4339			PN4391	N JFET	PN4391	2-72	4-4
NF580	N JFET	2N5432			PN4391-18	N JFET	PN4391-18	2-72	4-4
NF581	N JFET	2N5432			PN4392	N JFET	PN4392	2-72	4-4
NF582	N JFET	2N5433			PN4392-18	N JFET	PN4392-18	2-72	4-4
NF583	N JFET	2N5434			PN4393	N JFET	PN4393	2-72	4-4
NF584	N JFET	2N5433			PN4393-18	N JFET	PN4393-18	2-72	4-4
NF585	N JFET	2N4859			PN4416	N JFET	PN4416	2-73	4-11
NF4302	N JFET	2N4302			PN5163	N JFET	PN5163	2-74	
NF4303	N JFET	2N4303			PF510	P JFET	2N5018		
NF4304	N JFET	2N4304			PF511	P JFET	2N5014		
NF4445	N JFET	2N5432			SD210DE	D N JFET	SD210DE	2-76	
NF4446	N JFET	2N5433			SD211DE	D N JFET	SD211DE	2-78	
NF4447	N JFET	2N5432			SD212DE	D N JFET	SD212DE	2-76	
NF4448	N JFET	2N5433			SD213DE	D N JFET	SD213DE	2-78	
NF5163	N JFET	2N5163			SD214DE	D N JFET	SD214DE	2-76	
NF5457	N JFET	2N5457			SD215DE	D N JFET	SD215DE	2-78	
NF5458	N JFET	2N5458			SU2078	D N JFET	U425		
NF5459	N JFET	2N5459			SU2079	D N JFET	U425		
NF5484	N JFET	2N5484			SU2098	D N JFET	2N5197		
NF5485	N JFET	2N5485			SU2098A	D N JFET	2N5197		
NF5486	N JFET	2N5486			SU2098B	D N JFET	2N5196		
NF5555	N JFET	2N5555			SU2099	D N JFET	2N5197		
NF5638	N JFET	2N5638			SU2099A	D N JFET	2N5197		
NF5639	N JFET	2N5639			SU2365	D N JFET	U401		
NF5640	N JFET	2N5640			SU2365A	D N JFET	U401		
NF5653	N JFET	2N5653			SU2366	D N JFET	U402		
NF5654	N JFET	2N5654			SU2366A	D N JFET	U402		
PAD1	PAD N JFET	PAD1	2-68		SU2367	D N JFET	U403		
PAD2	PAD N JFET	PAD2	2-68		SU2367A	D N JFET	U403		
PAD5	PAD N JFET	PAD5	2-68		SU2368	D N JFET	U404		
PAD10	PAD N JFET	PAD10	2-68		SU2368A	D N JFET	U404		
PAD20	PAD N JFET	PAD20	2-68		SU2369	D N JFET	U405		
PAD50	PAD N JFET	PAD50	2-68		SU2369A	D N JFET	U405		
PAD100	PAD N JFET	PAD100	2-68		SU2410	D N JFET	U424		
P1086	P JFET	P1086	2-67	4-42					

FET Cross Reference and Index (Cont'd)

FET Cross Reference and Index



Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
SU2411	D N JFET	U425			U149	P JFET	2N2609		
SU2412	D N JFET	U426			U168	P JFET	2N2609		
TD5902	D N JFET	2N5902			U182	N JFET	2N4857		
TD5902	D N JFET	2N5902			U183	N JFET	2N3824		
TD5902A	D N JFET	2N5902			U197	N JFET	2N4339		
TD5903	D N JFET	2N5903			U198	N JFET	2N4340		
TD5903A	D N JFET	2N5903			U199	N JFET	2N4341		
TD5904	D N JFET	2N5904			U200	N JFET	U200	2-75	4-4
TD5904A	D N JFET	2N5904			U201	N JFET	U201	2-75	4-4
TD5905	D N JFET	2N5905			U202	N JFET	U202	2-75	4-4
TD5905A	D N JFET	2N5905			U221	N JFET	2N4391		
TD5906	D N JFET	2N5906			U222	N JFET	2N4391		
TD5906A	D N JFET	2N5906			U231	D N JFET	U231	2-76	4-22
TD5907	D N JFET	2N5907			U232	D N JFET	U232	2-76	4-22
TD5907A	D N JFET	2N5907			U233	D N JFET	U233	2-76	4-22
TD5908	D N JFET	2N5908			U234	D N JFET	U234	2-76	4-22
TD5908A	D N JFET	2N5908			U235	D N JFET	U235	2-76	4-22
TD5909	D N JFET	2N5909			U240	N JFET	2N5432		
TD5909A	D N JFET	2N5909			U241	N JFET	2N5433		
TD5911	D N JFET	2N5911			U242	N JFET	2N5432		
TD5911A	D N JFET	2N5911			U243	N JFET	2N5433		
TD5912	D N JFET	2N5912			U248	D N JFET	2N5902		
TD5912A	D N JFET	2N5912			U248A	D N JFET	2N5906		
TIS14	N JFET	2N4340			U249	D N JFET	2N5903		
TIS25	D N JFET	U401			U249A	D N JFET	2N5907		
TIS26	D N JFET	U402			U250	D N JFET	2N5904		
TIS27	D N JFET	U404			U250A	D N JFET	2N5908		
TIS41	N JFET	2N4859			U251	D N JFET	2N5905		
TIS58	N JFET	J305-18			U251A	D N JFET	2N5909		
TIS59	D N JFET	U1837			U254	N JFET	2N4859		
TIS73	N JFET	PN4391-18			U255	N JFET	2N4860		
TIS74	N JFET	PN4392-18			U256	N JFET	2N4861		
TIS75	N JFET	PN4393-18			U257	D N JFET	U257	2-77	4-36
TIS88	N JFET	2N5486			U273	N JFET	2N4118A		
TIXS41	N JFET	2N4859			U273A	N JFET	2N4118A		
TIXS42	N JFET	PN4393-18			U274	N JFET	2N4119A		
TN4117	N JFET	2N4117			U274A	N JFET	2N4119A		
TN4117A	N JFET	2N4117A			U275	N JFET	2N4119A		
TN4118	N JFET	2N4118			U275A	N JFET	2N4119A		
TN4118A	N JFET	2N4118A			U280	D N JFET	U231		
TN4119	N JFET	2N4119			U281	D N JFET	U231		
TN4119A	N JFET	2N4119A			U282	D N JFET	U232		
TN4338	N JFET	2N4338			U283	D N JFET	U232		
TN4339	N JFET	2N4339			U284	D N JFET	U233		
TN4340	N JFET	2N4340			U285	D N JFET	U234		
TN4341	N JFET	2N4341			U290	N JFET	U290	2-78	4-33
TP5114	P JFET	2N5114			U291	N JFET	U291	2-78	4-33
TP5115	P JFET	2N5115			U295	N JFET	U295		
TP5116	P JFET	2N5116			U296	N JFET	U296		
U110	P JFET	2N2608			U300	P JFET	2N5114		
U112	P JFET	2N2608			U301	P JFET	2N5115		
U133	P JFET	2N2608			U304	P JFET	U304	2-79	4-42
U146	P JFET	2N2608			U305	P JFET	U305	2-79	4-42
U147	P JFET	2N2608			U306	P JFET	U306	2-79	4-42
U148	P JFET	2N2608			U308	N JFET	U308	2-80	4-34

FET Cross Reference *and* Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U309	N JFET	U309	2-80	4-34	U1421	N JFET	2N3822		
U310	N JFET	U310	2-80	4-34	U1422	N JFET	2N3822		
U311	N JFET	U311	2-81	4-34	U1714	N JFET	2N4340		
U320	N JFET	U290			U1837E	N JFET	U1837		
U321	N JFET	U291			U1897	N JFET	U1897	2-88	4-4
U322	N JFET	U290			U1897-18	N JFET	U1897-18	2-88	4-4
U401	D N JFET	U401	2-82	4-18	U1897E	N JFET	U1897-18		
U402	D N JFET	U402	2-82	4-18	U1898	N JFET	U1898	2-88	4-4
U403	D N JFET	U403	2-82	4-18	U1898-18	N JFET	U1898-18	2-88	4-4
U404	D N JFET	U404	2-82	4-18	U1898E	N JFET	U1898-18	2-88	4-4
U405	D N JFET	U405	2-82	4-18	U1899	N JFET	U1899	2-88	4-4
U406	D N JFET	U406	2-82	4-18	U1899-18	N JFET	U1899-18		
U410	D N JFET	U410	2-83	4-25	U1899E	N JFT	U1899-18		
U411	D N JFET	U411	2-83	4-25	U1994E	N JFET	U1994		
U412	D N JFET	U412	2-83	4-25	U2047E	N JFET	PN4416		
U421	D N JFET	U421	2-84	4-20	U3000	N JFET	2N4341		
U422	D N JFET	U422	2-84	4-20	U3001	N JFET	2N4339		
U423	D N JFET	U423	2-84	4-20	U3002	N JFET	2N4338		
U424	D N JFET	U424	2-84	4-20	U3010	N JFET	2N4341		
U425	D N JFET	U425	2-84	4-20	U3011	N JFET	2N4340		
U426	D N JFET	U426	2-84	4-20	U3012	N JFET	2N4338		
U427	D N JFET	U427	2-85	4-20	UC20	N JFET	2N4341		
U428	D N JFET	U428	2-85	4-20	UC40	P JFET	2N2608		
U430	D N JFET	U430	2-86	4-34	UC41	P JFET	2N2608		
U431	D N JFET	U431	2-86	4-34	UC100	N JFET	2N4339		
U440	D N JFET	U440	2-87	4-36	UC110	N JFET	2N4339		
U441	D N JFET	U441	2-87	4-36	UC115	N JFET	2N4340		
U443	D N JFET	U443	2-87	4-36	UC120	N JFET	2N3686		
U444	D N JFET	U444	2-87	4-36	UC130	N JFET	2N4341		
U508	N JFET	CR030			UC155	N JFET	2N4416		
U1177	N JFET	2N4220A			UC200	N JFET	2N3824		
U1178	N JFET	2N3821			UC201	N JFET	2N3824		
U1179	N JFET	2N3821			UC210	N JFET	2N4416		
U1180	N JFET	2N4221A			UC220	N JFET	2N3822		
U1181	N JFET	2N4220A			UC240	N JFET	2N4869		
U1182	N JFET	2N3821			UC241	N JFET	2N4869		
U1277	N JFET	2N4339			UC250	N JFET	2N4091		
U1278	N JFET	2N4339			UC251	N JFET	2N4392		
U1279	N JFET	2N4340			UC300	P JFET	2N2608		
U1280	N JFET	2N4339			UC310	P JFET	2N2843		
U1281	N JFET	2N3822			UC320	P JFET	2N2843		
U1282	N JFET	2N4341			UC330	P JFET	2N2843		
U1283	N JFET	2N4340			UC340	P JFET	2N2843		
U1284	N JFET	2N4341			UC400	P JFET	2N3331		
U1285	N JFET	2N4220			UC401	P JFET	2N5116		
U1288	N JFET	2N4341			UC410	P JFET	2N3330		
U1287	N JFET	2N4092			UC420	P JFET	2N3329		
U1321	N JFET	2N3966			UC450	P JFET	2N5114		
U1322	N JFET	2N4221A			UC451	P JFET	2N5116		
U1323	N JFET	2N4221A			UC588	N JFET	2N4417		
U1324	N JFET	2N4220A			UC703	N JFET	2N4220		
U1325	N JFET	2N4222			UC704	N JFET	2N4220		
U1420	N JFET	2N3821			UC705	N JFET	2N4224		

FET Cross Reference and Index (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page	Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
UC707	N JFET	2N4860			UC2130	D N JFET	2N5452		
UC714	N JFET	2N3822			UC2132	D N JFET	2N3955		
UC714E	N JFET	J203-18			UC2134	D N JFET	2N3956		
UC734	N JFET	2N4416			UC2136	D N JFET	2N3957		
UC734E	N JFET	PN4416			UC2138	D N JFET	2N3958		
UC751	N JFET	2N4340			UC2139	D N JFET	2N3958		
UC752	N JFET	2N4340			UC2147	D N JFET	2N3958		
UC753	N JFET	2N4341			UC2148	D N JFET	2N3958		
UC754	N JFET	2N4340			UC2149	D N JFET	2N3958		
UC755	N JFET	2N4341			VCR2N	N JFET	VCR2N	2-89	4-4
UC756	N JFET	2N4340			VCR3P	P JFET	VCR3P	2-89	4-41
UC805	P JFET	2N3331			VCR4N	N JFET	VCR4N	2-89	4-23
UC807	N JFET	2N4860			VCR5P	P JFET	VCR5P	2-89	4-39
UC814	P JFET	2N3331			VCR6P	P JFET	2N5116		
UC851	P JFET	2N2608			VCR7N	N JFET	VCR7N	2-89	4-31
UC853	P JFET	2N2608			VCR11N	N JFET	VCR11N	2-91	
UC854	P JFET	2N2608			WK5457	N JFET	2N5457		
UC855	P JFET	2N2609			WK5458	N JFET	2N5458		
UC1700	P MOS ENH	3N163			WK5459	N JFET	2N5459		
UC1764	P MOS ENH	3N163							

Product Information

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

■ **Standard Products** All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.

■ **Examples of Modified Standard Products are:**

Electrical Specials Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

High Reliability Specials Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-STD-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

■ **Custom Products** Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.

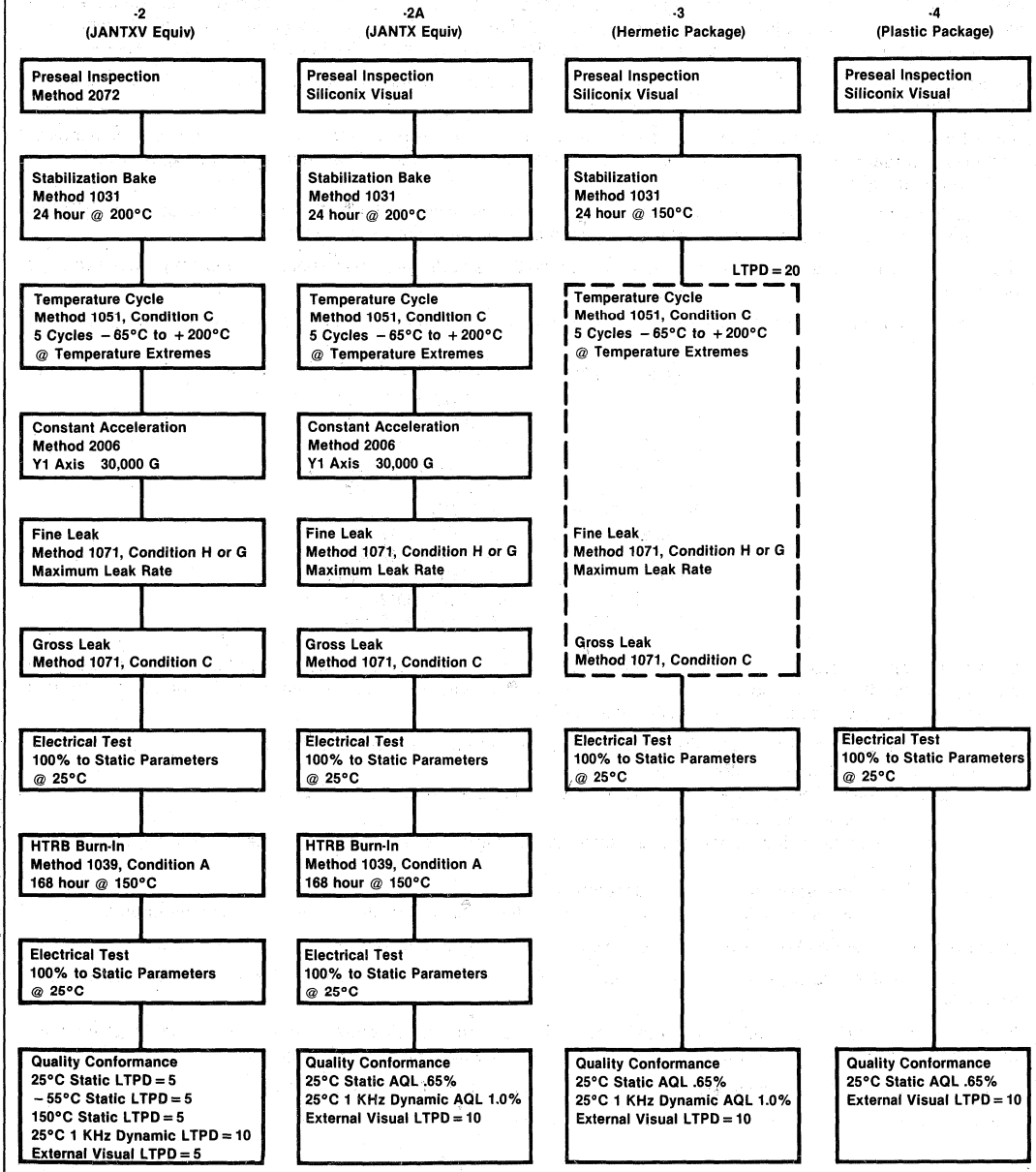
FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
CR CRR	Si Standard N-Channel Current Regulator	Si Standard N-Channel Current Regulator
DPAD DM DN	Si Standard Dual JFET Diode	Special DMOS Special N-Channel Dual FET (Also Standard Offering) Special N-Channel JFET (Also Standard Offering) Special TO-92 Cased FET (Also Standard Offering)
FN	Special N-Channel JFET	
J	Si Standard TO-92 Cased FET	
JPAD	Si Standard TO-92 Cased JFET Diode	
M	Si Standard MOSFET	
MEM	Si Standard MOSFET	
MU	Special MOSFET (Also Standard Offering)	
PAD	Si Standard JFET Diode	
PF	Special P-Channel JFET (Also Standard Offering)	
PN		Si Standard TO-92 Cased FET
SD	Si Standard DMOS	
SU	Special P-Channel JFET (Also Standard Offering)	
U	Si Standard FET	Si Standard FET
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
VMP	VMOS Power FET N-Channel	
VN		VMOS Power FET N-Channel
2N		JEDEC-Registered Device
3N	JEDEC-Registered Device	
Suffix		

-18 Std TO-92 Package with Center Lead Formed Toward Flat of TO-92 Package

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Index or current price list for availability of these devices.

Process Option Flow Chart



NOTES:
Processing and test methods are MIL-STD-750 unless specified otherwise.

Additional Product Options for European Customers

CECC 50 000

CECC 50 000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI, and UK generated specifications are prefixed with the letters BS.

A number of popular standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification
2N3970/1/2	BS CECC 50012-001
2N4091/2/3	BS CECC 50012-002
2N4391/2/3	BS CECC 50012-004
2N4856/7/8	BS CECC 50012-005
2N4859/60/61	BS CECC 50012-005
2N4856A/7A/8A	BS CECC 50012-006
2N4859A/60A/61A	BS CECC 50012-006
2N3821/2	BS CECC 50012-007
2N3824	BS CECC 50012-008
2N4220/1/2	BS CECC 50012-009
2N4220/1A/2A	BS CECC 50012-009

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 0000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)
quality assessment tests, assuring product conforms to electrical specification.
2. Group B sample inspection (lot by lot)
reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C sample inspection (periodic—3 monthly)
long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morrision, Swansea SA6 6NE, South Wales

In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750B and custom screening options.

JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information, enquiries may be directed to the nearest field sales office.

Die Process Information

Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.
- Standard thickness 0.008 ± 0.002 in inches.

Die Screening Criteria

Electrical Probe — Die are 100% probed in wafer form at 25°C to DC criteria and g_{fs} (1KHz) where applicable, LTPD20.

Visual Criteria — Die are supplied with 100% visual sort to the criteria of MIL-STD-750 method 2072.

LTPD — 20% on applicable parameters

Assembly

- Chips supplied in wafer packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C .
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

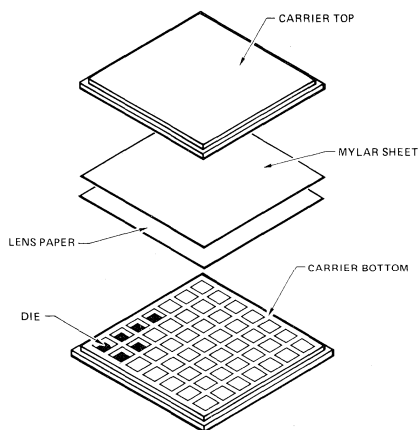
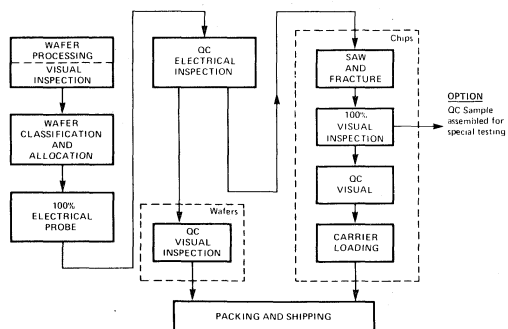
Options

- **SEM** — Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** — sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** — Siliconix has a chip processor/distributor with hot probe capability available.

Chip Packaging

- Chips are packaged as individual die in the flat wafer carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.
- Standard carrier 20 x 20 (400 die)

Chip and Wafer Processing



NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

PC Board Layout and Construction for Low Leakage Applications

In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of Teflon[®] or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85° C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.

Teflon[®] is a registered trademark of DuPont.

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

p-channel JFETs designed for . . .



Performance Curves PC PD
See Section 4

■ General Purpose Amplifiers

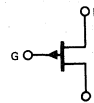
BENEFITS

- JAN Approved Version Available

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3) 30 V
 Gate Current, Forward Biased (Note 1) 50 mA
 Total Device Dissipation (Derate 2 mW/°C) 300 mW
 Storage Temperature Range -65 to +200°C

TO-18
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N2608		2N2609		Unit	Test Conditions		
	Min	Max	Min	Max				
1 S T A T I C I C	IGSS	Gate Reverse Current (Note 2)			nA	VGS = 30 V, VDS = 0 V		
			10		30	μA	VGS = 5 V, VDS = 0, TA = 150°C	
3	BVGS	30		30	V	IG = 1 μA, VDS = 0 V		
4	VGS(off)	1	4	1	4	V	VDS = -5 V, ID = 1 μA	
5	IDSS	-0.90	-4.50	-2	-10	mA	VDS = -5 V, VGS = 0 V	
6 D Y N A M I C	gf _s	1000		2500		μmho	VDS = -5 V, VGS = 0 V	f = 1 kHz
7	Ciss		17		30	pF	VDS = -5 V, VGS = 1 V	f = 140 kHz
8	NF		3		3	dB	VDS = -5 V, VGS = 0, RG = 1M Ω	f = 1 kHz

*JEDEC Registered Data

PC

PD

NOTES:

1. Not JEDEC Registered
2. IGSS is JEDEC Registered at VGS = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

2N2608 2N2609 (JAN)

2

2N3329 2N3330 2N3331 2N3332

p-channel JFETs designed for . . .



**Performance Curves PC
See Section 4**

- **Small-Signal Amplifiers**
- **Analog Multipliers**
- **Modulators**

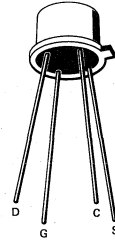
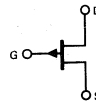
BENEFITS

- **Ease of Amplifier Design**
IDSS & gfs Closely Specified

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain and Gate-Source Voltage (Note 1) 20 V
 Gate Current 10 mA
 Total Device Dissipation at (or below)
 25°C Free-Air Temperature (Note 2) 300 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 230°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3329		2N3330		2N3331		2N3332		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max	Min	Max			
1 2 S T A T I C I C	IGSS	Gate Reverse Current		0.01	0.01	0.01	0.01	0.01	μA	VGS = 10 V, VDS = 0	
				10	10	10	10	10		VGS = 10 V, VDS = 0, TA = 150°C	
3 4 D Y N A M I C	BVGSS	Gate-Source Breakdown Voltage		20	20	20	20	20	V	IG = 10 μA, VDS = 0	
		VGS(off)	Gate-Source Cutoff Voltage		5	6	8	6		6	VDS = -15 V, ID = -10 μA
5 6	IDSS		Saturation Drain Current		-1	-3	-2	-6	-5	mA	VDS = -10 V, VGS = 0
		rDS(on)	Drain-Source ON Resistance		1000	800	600				Ω
7 8	gfs		Common-Source Input Conductance		0.2	0.2	0.2	0.2	μmho	VDS = -10 V	f = 1 kHz
		Common-Source Reverse Transfer Conductance		0.1	0.1	0.1	0.1	0.1			
9 10 11	gfs	Common-Source Output Conductance		20	40	100	20		f = 10 MHz		
		Common-Source Forward Transconductance		1000	2000	1500	3000				
12 13	Ciss	Common-Source Input Capacitance		20	20	20	20	pF	VDS = -10 V, VGS = 1 V	f = 1 MHz	
		Noise Figure		3	3	4	1				dB
14	Noise Figure									VDS = -5 V, ID = -1 mA Rgen = 10 MΩ	

*JEDEC registered data

PC

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2.0 mW/°C

2N3382 2N3384 2N3386

2

p-channel JFETs designed for . . .



Performance Curves PE
See Section 4

- Analog Switches
- Choppers
- Commutators
- Amplifiers

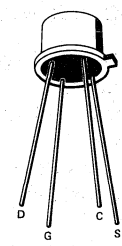
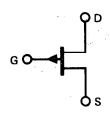
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 150 \Omega$ (2N3386)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain Voltage (Note 1)	30 V
Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Storage Temperature Range	-65 to +200°C
Total Dissipation at 25°C T _A (Note 2)	300 mW

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3382		2N3384		2N3386		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1 I _{GSS} Gate Reverse Current		15		15		15	nA	V _{GS} = 30 V V _{DS} = 0
2 I _{GSS} Gate Reverse Current		15		15		15	μA	V _{GS} = 5 V V _{DS} = 0 T _A = 150°C
3 BV _{GSS} Gate-Source Breakdown Voltage	30		30		30		V	I _G = 1 μA V _{DS} = 0
4 V _{GS(off)} Gate-Source Cutoff Voltage (Note 3)	1.0	5.0	4.0	5.0	4.0	9.5		V _{DS} = -5 V I _D = -1 μA
5 I _{DSS} Saturation Drain Current (Note 3)	-3.0	-30.0	-15.0	-30.0	-15.0	-50.0	mA	V _{DS} = -10 V V _{GS} = 0
6 I _{D(off)} Drain Cutoff Current		-2 (6)		-2 (6)		-2.5 (10)	nA (V)	V _{DS} = -5 V V _{GS} = ()
7 r _{ds(on)} Drain-Source ON Resistance		300		180		150	Ω	V _{GS} = 0 V _{DS} = 0 f = 1 kHz
8 g _{fs} Common-Source Forward Transconductance (Note 3)	4500	12,500	7500	12,500	7500	15,000	μmho	V _{DS} = -10 V V _{GS} = 0
9 C _{sgs} + C _{dgs} Source-Gate Capacitance Plus Drain-Gate Capacitance		6.0		6.0		6.0	pF	V _{DS} = 0 V _{GS} = 10 V f = 140 kHz
10 C _{iss} Common-Source Input Capacitance	16 Typ							

*JEDEC registered data.

PE

NOTE:

1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulswidth = 2 ms, duty cycle ≤ 3%.

n-channel JFET designed for . . .



**Performance Curves NH NRL
See Section 4**

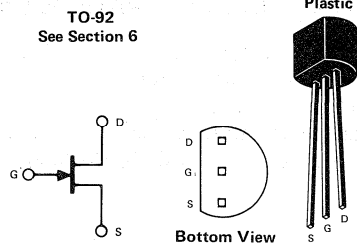
- **General Purpose Amplifiers**
- **Analog Switching**

BENEFITS

- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Gate Voltage	25 V
Drain-Source Voltage	25 V
Reverse Gate-Source Voltage	-25 V
Gate Current	10 mA
Continuous Device Dissipation at (or Below) 25°C Free Air Temperature (Note 1)	200 mW
Storage Temperature Range	-55°C to +150°C
Lead Temperature (1/16" from Case for 10 seconds)	260°C



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Max	Unit	Test Conditions	
S T A T I C	1	BV _{GSS} Gate-Source Breakdown Voltage	-25		V	I _G = -1 μA, V _{DS} = 0	
	2	I _{GSS} Gate Reverse Current		-2	nA	V _{GS} = -15 V, V _{DS} = 0	
	3			-2	μA		T _A = 100°C
D Y N A M I C	4	I _{DSS} Saturation Drain Current	2	20	mA	V _{DS} = 15 V, V _{GS} = 0 (Note 2)	
	5	V _{GS} Gate-Source Voltage	-0.5	-7.5	V	V _{DS} = 15 V, I _D = 200 μA	
	6	V _{GS(off)} Gate-Source Cutoff Voltage		-8	V	V _{DS} = 15 V, I _D = 2 nA	
	7	y _{fs} Common-Source Forward Transfer Admittance	2000	6500	μmho	V _{DS} = 15 V, V _{GS} = 0 (Note 2)	f = 1 kHz
8	y _{os} Common Source Output Admittance		50	μmho			
9 10 11	9	C _{iss} Common Source Input Capacitance		8	pF	V _{DS} = 15 V, V _{GS} = 0	f = 1 MHz
	10	C _{rss} Common Source Reverse Transfer Capacitance		4	pF		
	11	y _{fs} Common Source Forward Transfer Admittance	1600		μmho	V _{DS} = 15 V, V _{GS} = 0	f = 100 MHz

*JEDEC registered data

NH
NRL

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

n-channel JFETs designed for . . .



Performance Curves NRL
See Section 4

- Small-Signal Amplifiers
- Oscillators

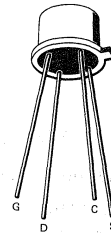
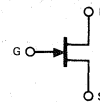
BENEFITS

- Operates from High Supply Voltages
 $BV_{GSS} > 50 \text{ V}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) -50 V
 Gate Current 10 mA
 Total Device Dissipation at (or below) 25°C
 Free-Air Temperature (Note 2) 300 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3821		2N3822		2N3823		Unit	Test Conditions				
	Min	Max	Min	Max	Min	Max						
1 2 3 4 5 6 7 8 9 10 11 12 13	IGSS	Gate Reverse Current		-0.1	-0.1	-0.5	nA	VGS = -30 V, VDS = 0 150°C				
		BVGSS	Gate-Source Breakdown Voltage		-50	-30	-0.5		μA			
5	VGS(loff)	Gate-Source Cutoff Voltage		-4	-6	-8	V	IG = -1 μA, VDS = 0 VDS = 15 V, ID = 0.5 nA VDS = 15 V, ID = 50 μA VDS = 15 V, ID = 200 μA VDS = 15 V, ID = 400 μA				
		VGS	Gate-Source Voltage		-0.5	-2			-1	-4	-1.0	-7.5
6	IDSS	Saturation Drain Current (Note 3)		0.5	2.5	2	10	4	20	mA	VDS = 15 V, VGS = 0	
7	gfS	Common-Source Forward Transconductance (Note 3)		1500	4500	3000	6500	3,500	6,500	μmho	VDS = 15 V, VGS = 0	f = 1 kHz
8	Yfs	Common-Source Forward Transadmittance		1500		3000		3,200				f = 100 MHz
9	gos	Common-Source Output Conductance (Note 3)			10		20		35	pF	VDS = 15 V, VGS = 0	f = 1 kHz
10	Ciss	Common-Source Input Capacitance			6		6		6			f = 1 MHz
11	Crss	Common-Source Reverse Transfer Capacitance			2		2		2			
12	NF	Noise Figure			5		5		6	dB	VDS = 15 V, VGS = 0, Rgen = 1 meg, BW = 5 Hz	f = 10 Hz
13	En	Equivalent Short-Circuit Input Noise Voltage			200		200		200	nV/√Hz	VDS = 15 V, VGS = 0, BW = 5 Hz	

*JEDEC Registered Data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

2N3821 2N3822 2N3823

2

n-channel JFET designed for . . .



Performance Curves NRL
See Section 4

- High Speed Commutators
- Choppers

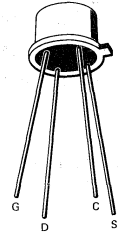
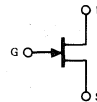
BENEFITS

- Low Insertion Loss
 $r_{ds(on)} < 250 \Omega$
- High Off-Isolation
 $I_{D(off)} < 0.1 \text{ nA}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1)	...	-50 V
Gate Current	...	10 mA
Total Device Dissipation at (or below) 25°C		
Free-Air Temperature (Note 2)	...	300 mW
Storage Temperature Range	...	-65 to +200°C
Lead Temperature	...	300°C
(1/16" from case for 10 seconds)		

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Max	Unit	Test Conditions	
1	S T A T I C	I_{GSS} Gate Reverse Current		-0.1	nA	$V_{GS} = -30 \text{ V}, V_{DS} = 0$	
2				-0.1	μA		150°C
3		BV_{GSS} Gate-Source Breakdown Voltage	-50		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$	
4		$I_{D(off)}$ Drain Cutoff Current		0.1	nA	$V_{DS} = 15 \text{ V}, V_{GS} = -8 \text{ V}$	
					0.1		μA
5	D Y N A M I C	$r_{ds(on)}$ Drain-Source ON Resistance		250	Ω	$V_{GS} = 0 \text{ V}, I_D = 0$	f = 1 kHz
6		C_{iss} Common-Source Input Capacitance		6	pF	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	f = 1 MHz
7		C_{rss} Common-Source Reverse Transfer Capacitance		3	pF	$V_{GS} = -8 \text{ V}, V_{DS} = 0$	

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

dual n-channel JFETs designed for . . .



Performance Curves NNR
See Section 4

■ Differential Amplifiers

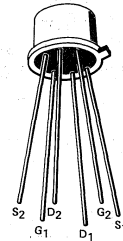
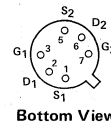
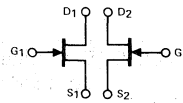
BENEFITS

- Minimum System Error and Calibration
5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
Low Output Conductance

TO-71
See Section 6

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	50 mA
Total Device Dissipation (Derate 1.7 mW/°C to 200°C)	300 mW
Storage Temperature Range	-65 to +200°C



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	IGSS Gate Reverse Current		-1	nA	VGS = -30 V, VDS = 0	100°C
			-1	μA		
	BV DGO Drain-Gate Breakdown Voltage	50			ID = 1 μA, IS = 0	
	VGS(off) Gate-Source Cutoff Voltage		-3	V	VDS = 10 V, ID = 1 nA	
	VGS Gate-Source Voltage	-0.2	-2.7		VDS = 10 V, ID = 100 μA	
7	IG Gate Operating Current		-250	pA	VDG = 10 V, ID = 700 μA	100°C
			-25	nA		
	IDSS Saturation Drain Current (Note 1)	1	10	mA	VDS = 10 V, VGS = 0	
9	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	VDG = 10 V, VGS = 0	f = 1 kHz
10	gos Common-Source Output Conductance		35			
11	Ciss Common-Source Input Capacitance		18	pF		
12	Crss Common-Source Reverse Transfer Capacitance		6			
13	gos Common-Source Forward Transconductance	1500		μmho	VDG = 10 V, ID = 700 μA	f = 1 kHz
14	gos Common-Source Output Conductance		20			
15	NF Spot Noise Figure		2	dB	VDS = 10 V, VGS = 0	f = 1 kHz, RG = 1 meg

2

Characteristic	2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max	Min	Max			
16	VGS1-VGS2		5		5		15		mV	VDG = 10 V, ID = 700 μA	
17	Δ VGS1-VGS2 ΔT		10		25		10		μV/°C		TA = 0°C TB = 100°C
18	gfs1 gfs2		0.95 1.0		0.95 1.0		0.95 1.0		-		f = 1 kHz

*JEDEC registered data.

NOTES:

1. Pulse test duration = 2 ms.
2. Measured at end points, TA and TB.
3. Assumes smaller value in numerator.

NNR

2N3921 2N3922 2N4084 2N4085

2N3954 2N3955 2N3954A 2N3955A
PREFERRED PART 2N5196

matched dual n-channel JFETs designed for . . .



Performance Curves NQP, NP-D
See Section 4

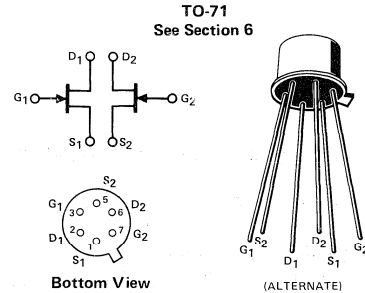
BENEFITS

- High Accuracy & Stability
 Offset Less Than 5 mV (2N3954, 54A)
 Drift Less Than 5 $\mu\text{V}/^\circ\text{C}$ (2N3954A)
- Wide Dynamic Range
 I_G Specified @ $V_{DS} = 20\text{ V}$
- Low Capacitance
 $C_{iss} < 4\text{ pF}$

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

ABSOLUTE MAXIMUM RATINGS (25°C)

Any Case-To-Lead Voltage	$\pm 100\text{ V}$
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	$\pm 100\text{ V}$
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	$-65\text{ to }+200^\circ\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	300°C



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3954		2N3954A		2N3955		2N3955A		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max	Min	Max			
1 IGSS Gate Reverse Current		-100		-100		-100		-100	pA	$V_{GS} = -30\text{ V}$,	$T_A = 125^\circ\text{C}$
2		-500		-500		-500		-500	nA	$V_{DS} = 0$	
3 BVGSS Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	$V_{DS} = 0$,	$I_G = -1\text{ }\mu\text{A}$
4 VGS(off) Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		$V_{DS} = 20\text{ V}$,	
5 VGS(f) Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		$I_D = 1\text{ nA}$	
6 VGS Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		$V_{DS} = 0$,	$I_D = 50\text{ }\mu\text{A}$ $I_D = 200\text{ }\mu\text{A}$
7	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		$V_{DS} = 20\text{ V}$	
8 IG Gate Operating Current		-50		-50		-50		-50	pA	$V_{DS} = 20\text{ V}$,	$T_A = 125^\circ\text{C}$
9		-250		-250		-250		-250	nA	$I_D = 200\text{ }\mu\text{A}$	
10 IDSS Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	$V_{DS} = 20\text{ V}$,	$V_{GS} = 0$
11 gfs Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000		$f = 1\text{ kHz}$	
12 gos Common-Source Output Conductance		35		35		35		35	μmho	$V_{DS} = 20\text{ V}$,	$f = 200\text{ MHz}$ $f = 1\text{ kHz}$
13 Ciss Common-Source Input Capacitance		4.0		4.0		4.0		4.0		$V_{GS} = 0$	
14 Crss Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF		$f = 1\text{ MHz}$
15 Cdgo Drain-Gate Capacitance		1.5		1.5		1.5		1.5		$V_{DG} = 10\text{ V}$,	
16 NF Common Source Spot Noise Figure		0.5		0.5		0.5		0.5	dB	$I_S = 0$	$f = 100\text{ Hz}$
17										$V_{DS} = 20\text{ V}$,	
18 G1-G2 Differential Gate Current		10		10		10		10	nA	$V_{GS} = 0$,	$T = 125^\circ\text{C}$
19 IDSS1/IDSS2 Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	-	$I_D = 200\text{ }\mu\text{A}$,	
20 VGS1-VGS2 Differential Gate-Source Voltage		5.0		5.0		10.0		5.0	mV	$V_{DS} = 20\text{ V}$,	$T = 25^\circ\text{C to }-55^\circ\text{C}$ $T = 25^\circ\text{C to }125^\circ\text{C}$
21 VGS1-VGS2 Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		$I_D = 200\text{ }\mu\text{A}$	
22		1.0		0.5		2.5		1.5			
23 gfs1/gfs2 Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	-		$f = 1\text{ kHz}$

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP, NP-D

matched dual n-channel JFETs designed for . . .



Performance Curves NQP, NP-D
See Section 4

BENEFITS

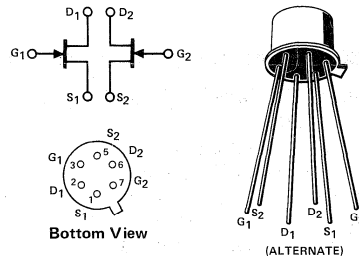
- Wide Dynamic Range
I_G Specified @ V_{DS} = 20 V
- Low Capacitance
C_{iss} < 4 pF

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N3956		2N3957		2N3958		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1 I _{GSS} Gate Reverse Current		-100		-100		-100	pA	V _{GS} = -30 V, V _{DS} = 0 T _A = 150°C
	2	-500		-500		-500	nA	
3 BV _{GSS} Gate-Source Breakdown Voltage	-50		-50		-50			V _{DS} = 0 V, I _G = -1 μA
4 V _{GS(off)} Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	V	V _{DS} = 20 V, I _D = 1 nA
	5	2.0	2.0	2.0	2.0	2.0		V _{DS} = 0 V, I _G = 1 mA
6 V _{GS(f)} Gate-Source Forward Voltage		-4.2		-4.2		-4.2	V	V _{DS} = 20 V, I _D = 50 μA
	7	-0.5	-4.0	-0.5	-4.0	-0.5		-4.0
8 I _G Gate Operating Current		-50		-50		-50	pA	V _{DS} = 20 V, I _D = 200 μA T _A = 125°C
	9	-250	-250	-250	-250	-250		
10 I _{DSS} Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V _{DS} = 20 V, V _{GS} = 0
11 y _{fs1} Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	f = 1 kHz
12	1000	1000	1000	1000	1000	1000		f = 200 MHz
13 g _{os} Common-Source Output Conductance		35		35		35	pF	f = 1 kHz
14 C _{iss} Common-Source Input Capacitance		4.0		4.0		4.0		f = 1 MHz
15 C _{rss} Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2	pF	V _{DS} = 20 V, V _{GS} = 0
16 C _{dgo} Drain-Gate Capacitance		1.5		1.5		1.5		V _{DG} = 10 V, I _S = 0
17 NF Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V _{DS} = 20 V, V _{GS} = 0 V, R _G = 10 MΩ, f = 100 Hz
18 I _{G1} -I _{G2} Differential Gate Reverse Current		10		10		10	nA	V _{DS} = 20 V, I _D = 200 μA, T = 125°C
19 I _{DSS1} /I _{DSS2} Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	-	V _{DS} = 20 V, V _{GS} = 0
20 V _{GS1} -V _{GS2} Differential Gate-Source Voltage		15		20		25	mV	V _{DS} = 20 V, I _D = 200 μA
21 Δ V _{GS1} -V _{GS2} Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0		
22		5.0		7.5		10.0		T = 25°C to 125°C
23 g _{fs1} /g _{fs2} Transconductance Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	-	f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP, NP-D

2N3956 2N3957 2N3958
PREFERRED PART 2N5196

2

n-channel JFET designed for . . .



Performance Curves NH
See Section 4

- Analog Switches
- Choppers
- Commutators

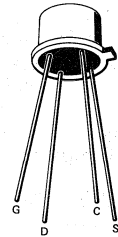
BENEFITS

- Low Insertion Loss, No Offset Voltage
 $r_{DS(on)} < 220 \Omega$
- Short Switching Aperture Times
 $C_{rss} < 1.5 \text{ pF}$
 $t_{(on)} + t_{(off)} < 50 \text{ ns Typical}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage -30 V
 Gate Current 10 mA
 Total Device Dissipation
 (25°C Free-Air Temperature) 300 mW
 Power Derating 1.7 mW/°C
 Storage Temperature Range -55 to +200°C
 Operating Temperature Range -55 to +175°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-72
See Section 6



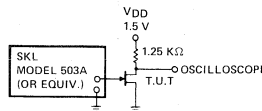
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Typ	Max	Unit	Test Conditions
1	S T A T I C	I_{GSS} Gate Reverse Current			-0.1	nA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$
2		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4		-6.0	V	$V_{DS} = 10 \text{ V}, I_D = 10 \text{ nA}$
3		BV_{GSS} Gate-Source Breakdown Voltage	-30				$I_G = -1 \mu\text{A}, V_{DS} = 0$
4		I_{DSS} Saturation Drain Current (Note 1)	2.0			mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
5		$I_{D(off)}$ Drain Cutoff Current			1.0	nA	$V_{DS} = 10 \text{ V}, V_{GS} = -7 \text{ V}$ $T_A = 150^\circ\text{C}$
6					2.0	μA	
7		$r_{DS(on)}$ Static Drain-Source ON Resistance			220	Ω	$V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0$
8		$V_{DS(on)}$ Drain-Source ON Voltage			0.25	V	$I_D = 1 \text{ mA}, V_{GS} = 0$
9		I_{DGO} Drain Reverse Current			0.1	nA	$V_{DG} = 20 \text{ V}, I_S = 0$ $T_A = 150^\circ\text{C}$
10					0.2	μA	
11	D Y N A M I C	$r_{ds(on)}$ Drain-Source ON Resistance			220	Ω	$V_{GS} = 0, I_D = 0$ $f = 1 \text{ kHz}$
12		C_{iss} Common-Source Input Capacitance		3.1	6.0	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ $f = 1 \text{ MHz}$
13		C_{rss} Common-Source Reverse Transfer Capacitance		0.8	1.5		$V_{DS} = 0, V_{GS} = -7 \text{ V}$
14		$t_{d(on)}$ Turn ON Delay Time		3.0	20	ns	$V_{DD} = 1.5 \text{ V}$ $I_{D(on)} = 1.0 \text{ mA}$ $V_{GS(on)} = 0$ $V_{GS(off)} = -6 \text{ V}$ $R_L = 1.25\text{k} \Omega$ See Circuit Below
15	t_r Rise Time		10.0	100			
16	t_{off} Turn OFF Time		30.0	100			
17	$t_{d(off)}$ Turn OFF Delay Time (Note 2)		10.0				
18	t_f Fall Time (Note 2)		20.0				

* JEDEC registered parameters unless otherwise noted (apply to min/max only).

NOTES:

1. Pulse test duration $\leq 2 \text{ ms}$.
2. Non-JEDEC registered parameters:
 $t_{d(off)} + t_f = t_{off}$.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 ns
PULSE DUTY CYCLE 50%
INPUT RESISTANCE 50 Ω

SAMPLING SCOPE
RISE TIME < 10 ns
INPUT RESISTANCE > 5 M Ω @ < 10 pF

NH

n-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Amplifiers

Performance Curves NC
See Section 4

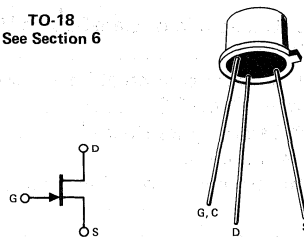
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 30 \Omega$ (2N3970)
- Good Off-Isolation
 $I_{D(off)} < 250 \text{ pA}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage -40 V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Case Temperature
 (Note 1) 1.8 W
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-18
See Section 6



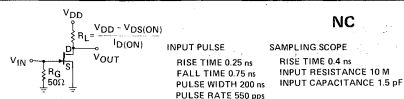
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N3970		2N3971		2N3972		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max			
1 BV _{GSS} Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$	
2 I _{DGO} Drain Reverse Current		250		250		250	pA	$V_{DG} = 20 \text{ V}, I_S = 0$	
3		500		500		500	nA		150°C
4 I _{D(off)} Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20 \text{ V}, V_{GS} = -12 \text{ V}$	
5		500		500		500	nA		150°C
6 V _{GS(off)} Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$	
7 I _{DSS} Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	
8						2		$V_{GS} = 0$	
9 V _{DS(on)} Drain-Source ON Voltage				1.5			V		$I_D = 5 \text{ mA}$
10		1							$I_D = 10 \text{ mA}$
11 r _{DS(on)} Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 1 \text{ mA}$	
12 r _{ds(on)} Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 0$ f = 1 kHz	
13 C _{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ f = 1 MHz	
14 C _{rss} Common-Source Reverse Transfer Capacitance		6		6		6	pF	$V_{DS} = 0, V_{GS} = -12 \text{ V}$	
15 t _{d(on)} Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10 \text{ V}, V_{GS(off)} = 0$ $I_{D(on)} \quad R_L \quad V_{GS(off)}$	
16 t _r Rise Time		10		15		40			2N3970 20 mA 450 Ω -10 V
17 t _{off} Turn-Off Time		30		60		100			2N3971 10 mA 850 Ω -5 V 2N3972 5 mA 1.6K Ω -3 V

*JEDEC registered data.

NOTE:

1. Derate linearly at the rate of 10 mW/°C.



2N3970 2N3971 2N3972

2

n-channel JFETs designed for . . .



Performance Curves NT
See Section 4

- Ultra-High Input Impedance Amplifiers
- Electrometers
- pH Meters
- Smoke Detectors

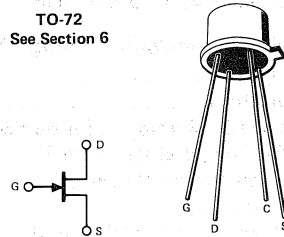
BENEFITS

- Low Power
 $I_{DSS} < 90 \mu A$ (2N4117)
- Minimum Circuit Loading
 $I_{GSS} < 1 pA$ (2N4117A Series)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) -40 V
 Gate-Current 50 mA
 Total Device Dissipation
 (Derate 2 mW/°C to 175°C) 300 mW
 Storage Temperature Range -65 to +175°C
 Lead Temperature
 (1/16" from case for 10 seconds) 255°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Unit	Test Conditions					
	Min	Max	Min	Max	Min	Max							
S T A T I C	1	I _{GSS}	Gate Reverse Current 2N4117 Series Only		-10	-10	-10	pA	V _{GS} = -20 V, V _{DS} = 0	150°C			
			-25	-25	-25								
	3	I _{GSS}	Gate Reverse Current 2N4117A Series Only		-1	-1	-1	pA	V _{GS} = -20 V, V _{DS} = 0	150°C			
-2.5			-2.5	-2.5									
5	BV _{GSS}	Gate-Source Breakdown Voltage		-40	-40	-40	V	I _G = -1 μA, V _{DS} = 0					
	6	V _{GS(off)}	Gate-Source Cutoff Voltage		-0.6	-1.8		-1	-3	-2	-6	V _{DS} = 10 V, I _D = 1 nA	
7	I _{DSS}	Saturation Drain Current (Note 2)		0.03	0.09	0.08	0.24	0.20	0.60	mA	V _{DS} = 10 V, V _{GS} = 0		
D Y N A M I C	8	g _{fs}	Common-Source Forward Transconductance (Note 2)		70	210	80	250	100	330	μmho	V _{DS} = 10 V, V _{GS} = 0	f = 1 kHz
	9	g _{os}	Common-Source Output Conductance			3		5		10			
	10	C _{iss}	Common-Source Input Capacitance			3		3		3	pF	f = 1 MHz	
	11	C _{rss}	Common-Source Reverse Transfer Capacitance			1.5		1.5		1.5			

*JEDEC registered data.

NT

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

2N4117 2N4117A 2N4118 2N4118A 2N4119 2N4119A
 PREFERRED PARTS FN4117 SERIES, PLASTIC EQUIVALENT PN4117 SERIES

2N4220 2N4221 2N4222 2N4221A 2N4222A

n-channel JFETs designed for . . .



**Performance Curves NRL
See Section 4**

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

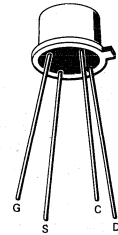
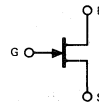
BENEFITS

- High Gain
- Low Receiver Noise Figure

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Drain Current	15 mA
Total Device Dissipation at (or below) 25°C	
Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
	Min	Max	Min	Max	Min	Max			
1 I _{GSS} Gate Reverse Current		-0.1		-0.1		-0.1	nA	V _{GS} = -15 V, V _{DS} = 0	
2 BV _{GSS} Gate-Source Breakdown Voltage		-0.1		-0.1		-0.1	μA		150°C
3 V _{GS(off)} Gate-Source Cutoff Voltage	-30		-30		-30		V	I _G = -10 μA, V _{DS} = 0	
4 V _{GS} Gate-Source Voltage		-4		-6		-8	V	V _{DS} = 15 V, I _D = 0.1 nA	
5 I _{DSS} Saturation Drain Current (Note 3)	-0.5 (50)	-2.5 (50)	-1 (200)	-5 (200)	-2 (500)	-6 (500)	μA	V _{DS} = 15 V, I _D = ()	
7 g _{fs} Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000		V _{DS} = 15 V, V _{GS} = 0	f = 1 kHz
8 y _{fs} Common-Source Forward Transadmittance	750		750		750		μmho		f = 100 MHz
9 g _{os} Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
10 C _{iss} Common-Source Input Capacitance		6		6		6			f = 1 MHz
11 C _{rss} Common-Source Reverse Transfer Capacitance		2		2		2	pF		
12 NF Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V _{DS} = 15 V, V _{GS} = 0 R _{gen} = 1 meg	f = 100 Hz

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs designed for . . .



Performance Curves NRL
See Section 4

■ VHF Amplifiers

■ Mixers

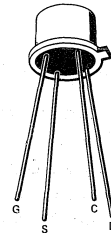
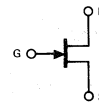
BENEFITS

- Low Noise
NF = 3 dB Typical @ 200 MHz
- Easy Tuning
 $C_{rss} < 2 \text{ pF}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Drain Current	20 mA
Total Device Dissipation at (or below) 25°C	
Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

1	2	3	4	5	6	2N4223		2N4224		Unit	Test Conditions		
						Min	Max	Min	Max				
S T A T I C	1	IGSS	Gate Reverse Current				-0.25		-0.5	nA	V _{GS} = -20 V, V _{DS} = 0		
							-0.25		-0.5	μA		150°C	
S T A T I C	4	BV _{GSS}	Gate-Source Breakdown Voltage	-30		-30				V	I _G = -10 μA, V _{DS} = 0		
				(0.25)	(0.25)	(0.5)	(0.5)	(nA)					
S T A T I C	5	V _{GS}	Gate-Source Cutoff Voltage	-1.0	-7.0	-1.0	-7.5			V	V _{DS} = 15 V, I _D = ()		
				(0.3)	(0.3)	(0.2)	(0.2)	(mA)					
D Y N	7	I _{DSS}	Saturation Drain Current (Note 3)	3	18	2	20			mA	V _{DS} = 15 V, V _{GS} = 0		
D Y N	8	g _{fs}	Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500			μmho	V _{DS} = 15 V, V _{GS} = 0	f = 1 kHz	
D Y N	9	C _{iss}	Common-Source Input Capacitance (Output Shorted)		6		6			pF	V _{DS} = 15 V, V _{GS} = 0	f = 1 MHz	
H I G H	10	C _{rss}	Common-Source Reverse Transfer Capacitance		2		2				V _{DS} = 15 V, V _{GS} = 0		
F R E Q	11	y _{fs}	Common-Source Forward Transmittance	2700		1700				μmho	V _{DS} = 15 V, V _{GS} = 0	f = 200 MHz	
F R E Q	12	g _{iss}	Common-Source Input Conductance (Output Shorted)		800		800				V _{DS} = 15 V, V _{GS} = 0	f = 200 MHz	
F R E Q	13	g _{oss}	Common-Source Output Conductance (Input Shorted)		200		200				V _{DS} = 15 V, V _{GS} = 0	f = 200 MHz	
F R E Q	14	G _{ps}	Small Signal Power Gain	10						dB	V _{DS} = 15 V, V _{GS} = 0, R _{gen} = 1 K		
F R E Q	14	NF	Noise Figure		5						V _{DS} = 15 V, V _{GS} = 0, R _{gen} = 1 K		

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

2N4338 2N4339 2N4340 2N4341

n-channel JFETs designed for . . .



Performance Curves NP
See Section 4

- Small-Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

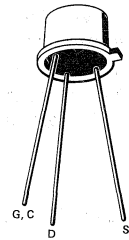
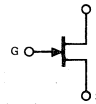
BENEFITS

- Low Noise
NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
 $V_{GS(off)} < 1\text{ V}$ (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
3:1 I_{DSS} , V_p , g_{fs} Ranges
- High Off-Isolation as a Switch
 $I_{D(off)} < 50\text{ pA}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1)	-50 V
Gate Current	50 mA
Total Device Dissipation (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Maximum Operating Temperature	175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)**

Characteristic	2N4338		2N4339		2N4340		2N4341		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max	Min	Max		
1 I_{GSS} Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	$V_{GS} = -30\text{ V}, V_{DS} = 0$ 150°C
2		-0.1		-0.1		-0.1		-0.1	µA	
3 BV_{GSS} Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	$I_G = -1\text{ µA}, V_{DS} = 0$
4 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		
5 $I_{D(off)}$ Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	$V_{DS} = 15\text{ V}$ $V_{GS} = ()$
6 I_{DSS} Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	$V_{DS} = 15\text{ V}, V_{GS} = 0$
7 g_{fs} Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	µmho	$V_{DS} = 15\text{ V}, V_{GS} = 0$ f = 1 kHz
8 g_{os} Common-Source Output Conductance		5		15		30		60		
9 $r_{ds(on)}$ Drain-Source ON Resistance		2500		1700		1500		800		
10 C_{iss} Common-Source Input Capacitance		7		7		7		7	pF	$V_{DS} = 15\text{ V}, V_{GS} = 0$ f = 1 MHz
11 C_{rss} Common-Source Reverse Transfer Capacitance		3		3		3		3		
12 NF Noise Figure		1		1		1		1	dB	$V_{DS} = 15\text{ V}, V_{GS} = 0$ $R_{gen} = 1\text{ meg}, BW = 200\text{ Hz}$ f = 1 kHz

*JEDEC registered data

NP

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d-c power is applied. (Not a JEDEC condition.)

n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Performance Curves NC See Section 4

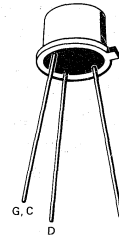
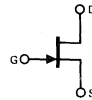
BENEFITS

- Low Insertion Loss, High Accuracy in Test Systems $r_{DS(on)} < 30 \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive
High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100 \text{ pA}$
- High Speed $t_{ON} < 20 \text{ ns}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 6



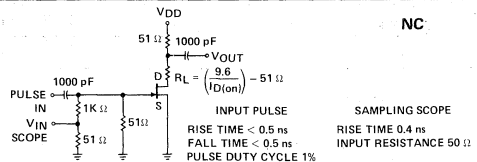
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N4391		2N4392		2N4393		Unit	Test Conditions						
	Min	Max	Min	Max	Min	Max								
1 I_{GSS} Gate Reverse Current		-100		-100		-100	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$	150°C					
2 BV_{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$						
3 $I_{D(off)}$ Drain Cutoff Current						100	pA	$V_{DS} = 20 \text{ V}$	$V_{GS} = -5 \text{ V}$	150°C				
						200	nA							
				100			pA							
				200			nA							
		100					pA							
6 $V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	$I_G = 1 \text{ mA}, V_{DS} = 0$						
7 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ mA}$						
8 I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$						
9 $V_{DS(on)}$ Drain Source ON Voltage				0.4			V	$V_{GS} = 0$	$I_D = 3 \text{ mA}$	150°C				
		0.4					V				$I_D = 6 \text{ mA}$			
							V				$I_D = 12 \text{ mA}$			
10 $r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 1 \text{ mA}$						
11 $r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0, I_D = 0$	f = 1 kHz					
12 C_{iss} Common-Source Input Capacitance		14		14		14	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	f = 1 MHz					
				3.5			pF				$V_{DS} = 0, V_{GS} = -5 \text{ V}$			
				3.5			pF				$V_{GS} = -7 \text{ V}$			
13 C_{rss} Common-Source Reverse Transfer Capacitance		3.5					pF	$V_{DS} = 0, V_{GS} = -12 \text{ V}$						
14 $t_{d(on)}$ Turn-ON Delay Time		15		15		15	ns	$V_{DD} = 10 \text{ V}, V_{GS(on)} = 0$	$I_{D(on)}$	$V_{GS(off)}$	RL			
15 t_r Rise Time		5		5		5	ns					2N4391	12 mA	-12 V
16 $t_{d(off)}$ Turn-OFF Delay Time		20		35		50	ns					2N4392	6	-7
17 t_f Fall Time		15		20		30	ns					2N4393	3	-5

*JEDEC registered data.

NOTE:

- Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$.



2N4391 2N4392 2N4393
PREFERRED PARTS FN4392 SERIES, PLASTIC EQUIVALENT PN4391 SERIES

2

n-channel JFETs designed for . . .



Performance Curves NH
See Section 4

- VHF Amplifiers
- Mixers

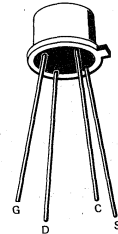
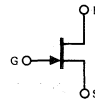
BENEFITS

- Low Noise
NF = 3 dB Typical at 400 MHz
- Wide Band
High g_{fs}/C_{iss} Ratio

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage, 2N4416 -30 V
 Gate-Drain or Gate-Source Voltage, 2N4416A -35 V
 Gate Current 10 mA
 Total Device Dissipation (Derate 1.7 mW/°C) 300 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	1 I _{GSS} Gate Reverse Current		-0.1	nA	V _{GS} = -20 V, V _{DS} = 0 V	150°C
	2		-0.1	μA		
	3 BV _{GSS} Gate-Source Breakdown Voltage	-30		V	I _G = -1 μA, V _{DS} = 0 V	2N4416
4 V _{GS(off)} Gate-Source Cutoff Voltage			-6	V	V _{DS} = 15 V, I _D = 1 nA	2N4416
		-2.5	-6			2N4416A
D Y N A M I C	5 I _{DSS} Saturation Drain Current (Note 1)	5	15	mA	V _{DS} = 15 V, V _{GS} = 0 V	f = 1 kHz
	6 g _{fs} Common-Source Forward Transconductance	4500	7500	μmho		
	7 g _{os} Common-Source Output Conductance		50	μmho		
	8 C _{rss} Common-Source Reverse Transfer Capacitance		0.8	pF		
	9 C _{iss} Common-Source Input Capacitance		4	pF		
	10 C _{oss} Common-Source Output Capacitance		2			

Characteristic		100 MHz		400 MHz		Unit	Test Conditions	
		Min	Max	Min	Max			
H I G H F R E Q U E N C Y	11 g _{iss} Common-Source Input Conductance		100		1000	μmho	V _{DS} = 15 V, V _{GS} = 0 V	
	12 b _{iss} Common-Source Input Susceptance		2500		10,000			
	13 g _{oss} Common-Source Output Conductance		75		100			
	14 b _{oss} Common-Source Output Susceptance		1000		4000			
	15 g _{fs} Common-Source Forward Transconductance			4000				
	16 G _{ps} Common-Source Power Gain	18		10				dB
	17 NF Noise Figure		2		4			

*JEDEC Registered data

NH

NOTES:

1. Pulse test duration = 300 μs.

n-channel JFETs designed for . . .



Performance Curves NC
See Section 4

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

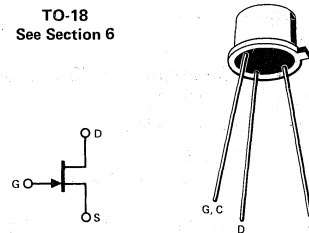
BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
 $r_{DS(on)} < 25 \Omega$ (2N4856, 59)
- High Off-Isolation
 $I_{D(off)} < 250 \text{ pA}$
- High Speed
 $t_{ON} < 9 \text{ ns}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856-58	-40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61	-30 V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 6



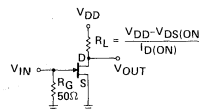
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N4856 2N4859		2N4857 2N4860		2N4858 2N4861		Unit	Test Conditions		
	Min	Max	Min	Max	Min	Max				
1 BV _{GSS} Gate-Source Breakdown Voltage	2N4856-58	-40	2N4859-61	-30	2N4856-58	-40	V	$I_G = -1 \mu\text{A}, V_{DS} = 0$		
3 I _{GSS} Gate Reverse Current	2N4856-58	-250	2N4859-61	-500	2N4856-58	-250	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$		
4		-500		-500		-500	nA	150°C		
5		-250		-250		-250	pA	$V_{GS} = -15 \text{ V}, V_{DS} = 0$		
6		-500		-500		-500	nA	150°C		
7 I _{D(off)} Drain Cutoff Current		250		250		250	pA	$V_{DS} = 15 \text{ V}, V_{GS} = -10 \text{ V}$		
8		500		500		500	nA	150°C		
9 V _{GS(off)} Gate-Source Cutoff Voltage		-4		-10		-2	V	$V_{DS} = 15 \text{ V}, I_D = 0.5 \text{ nA}$		
10 I _{DSS} Saturation Drain Current (Note 1)		50		20		100	80	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	
11 V _{DS(on)} Drain-Source ON Voltage		0.75 (20)		0.50 (10)		0.50 (5)	0.50 (5)	V (mA)	$V_{GS} = 0, I_D = ()$	
12 r _{ds(on)} Drain-Source ON Resistance		25		40		60	Ω	$V_{GS} = 0, I_D = 0$	f = 1 kHz	
13 C _{iss} Common-Source Input Capacitance		18		18		18	pF	$V_{DS} = 0, V_{GS} = -10 \text{ V}$	f = 1 MHz	
14 C _{rss} Common-Source Reverse Transfer Capacitance		8		8		8	pF			
15 t _{d(on)} Turn-ON Delay Time		6 (20) [-10]		6 (10) [-6]		10 (5) [-4]	ns (mA) [V]			
16 t _r Rise Time		3 (20) [-10]		4 (10) [-6]		10 (5) [-4]	ns (mA) [V]		$V_{DD} = 10 \text{ V}, V_{GS(on)} = 0, I_D(on) = (), V_{GS(off)} = []$	$R_L = \begin{cases} 464 \Omega, 2N4856, 59 \\ 953 \Omega, 2N4857, 60 \\ 1910 \Omega, 2N4858, 61 \end{cases}$
17 t _{off} Turn-OFF Time		25 (20) [-10]		50 (10) [-6]		100 (5) [-4]	ns (mA) [V]			

*JEDEC registered data.

NOTE:

1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

NC

2N4856A 2N4857A 2N4858A
2N4859A 2N4860A 2N4861A

n-channel JFETs designed for . . .



Performance Curves NC
See Section 4

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

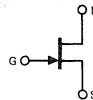
BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
 $r_{DS(on)} < 25 \Omega$ (2N4856A, 59A)
- High Off-Isolation
 $I_{D(off)} < 250 \text{ pA}$
- Short Sample and Hold Aperture Time
 $C_{rss} < 4 \text{ pF}$
- High Speed
 $t_{ON} < 8 \text{ ns}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856A-58A.	-40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859A-61A.	-30 V
Gate Current.	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N4856A 2N4859A		2N4857A 2N4860A		2N4858A 2N4861A		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max			
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	BV _{GSS}	Gate-Source Breakdown Voltage		2N4856A-58A	2N4859A-61A	-40	-30	V	$I_G = -1 \mu\text{A}, V_{DS} = 0$
		2N4856A-58A	2N4859A-61A	-40	-30				
I _{GSS}	Gate Reverse Current	2N4856A-58A	2N4859A-61A	-250	-500	-250	-500	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$
		2N4856A-58A	2N4859A-61A	-250	-500	-250	-500	nA	$V_{GS} = -15 \text{ V}, V_{DS} = 0$
I _{D(off)}	Drain Cutoff Current	2N4856A-58A	2N4859A-61A	250	500	250	500	nA	$V_{DS} = 15 \text{ V}, V_{GS} = -10 \text{ V}$
		2N4856A-58A	2N4859A-61A	250	500	250	500	nA	$V_{DS} = 15 \text{ V}, V_{GS} = -10 \text{ V}$
V _{GS(off)}	Gate-Source Cutoff Voltage	-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15 \text{ V}, I_D = 0.5 \text{ mA}$
I _{DSS}	Saturation Drain Current (Note 1)	50	20	100	8	80	80	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
V _{DS(on)}	Drain-Source ON Voltage		0.75 (20)	0.50 (10)	0.50 (5)			V (mA)	$V_{GS} = 0, I_D = ()$
r _{ds(on)}	Drain-Source ON Resistance		25	40	60			Ω	$V_{GS} = 0, I_D = 0$
C _{iss}	Common-Source Input Capacitance		10	10	10			pF	$V_{DS} = 0, V_{GS} = -10 \text{ V}$
C _{rss}	Common-Source Reverse Transfer Capacitance		4	3.5	3.5			pF	$V_{DS} = 0, V_{GS} = -10 \text{ V}$
t _{d(on)}	Turn-ON Delay Time		5 (20) [-10]	6 (10) [-6]	8 (5) [-4]			ns (mA) [V]	$V_{DD} = 10 \text{ V}, V_{GS(on)} = 0, I_{D(on)} = (), V_{GS(off)} = (-)$
t _r	Rise Time		3 (20) [-10]	4 (10) [-6]	8 (5) [-4]			ns (mA) [V]	
t _{off}	Turn-OFF Time		20 (20) [-10]	40 (10) [-6]	80 (5) [-4]			ns (mA) [V]	

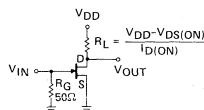
$$R_L = \begin{cases} 464 \Omega, 2N4856A, 59A \\ 953 \Omega, 2N4857A, 60A \\ 1910 \Omega, 2N4858A, 61A \end{cases}$$

NC

*JEDEC registered data.

NOTE:

- Pulse test required, pulsewidth = 100 μs , duty cycle $\leq 10\%$.



INPUT PULSE

- RISE TIME 0.25 ns
- FALL TIME 0.75 ns
- PULSE WIDTH 100 ns
- PULSE DUTY CYCLE < 10%

SAMPLING SCOPE

- RISE TIME 0.75 ns
- INPUT RESISTANCE 1 M
- INPUT CAPACITANCE 2.5 pF

n-channel JFETs designed for . . .



Performance Curves NS
See Section 4

■ Audio and Sub-Audio Amplifiers

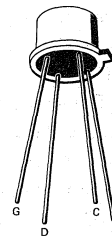
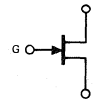
BENEFITS

- Ultra Low Noise
 $\bar{e}_n = 8 \text{ nV}/\sqrt{\text{Hz}}$ Typical at 10 Hz
 $\bar{e}_n = 2 \text{ nV}/\sqrt{\text{Hz}}$ Typical at 1 kHz

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) -40 V
 Gate Current or Drain Current 50 mA
 Total Device Dissipation
 (Derate 1.7 mW/°C) 300 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-72
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	Characteristic			Unit	Test Conditions	
														Min	Max	Min		Max	Min
S T A T I C	1	IGSS	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V _{GS} = -30 V, V _{DS} = 0								
					-0.25		-0.25		-0.25	µA									
	3	BV _{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I _G = -1 µA, V _{DS} = 0								
	4	V _{GS(off)}	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5	V	V _{DS} = 20 V, I _D = 1 µA								
5	I _{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V _{DS} = 20 V, V _{GS} = 0									
D Y N A M I C	6	g _{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	µmho	V _{DS} = 20 V, V _{GS} = 0								f = 1 kHz
	7	g _{os}	Common-Source Output Conductance		1.5		4		10	µmho	V _{DS} = 20 V, V _{GS} = 0								f = 1 kHz
	8	C _{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF	V _{DS} = 20 V, V _{GS} = 0								f = 1 MHz
9	C _{iss}	Common-Source Input Capacitance		25		25		25	pF	V _{DS} = 20 V, V _{GS} = 0								f = 1 MHz	
10	11	ē _n	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	V _{DS} = 10 V, V _{GS} = 0							f = 10 Hz	
12	13	ē _n	Short Circuit Equivalent Input Noise Voltage		10		10		10	nV/√Hz	V _{DS} = 10 V, V _{GS} = 0							f = 1 kHz	
13	14	NF	Spot Noise Figure		5		5		5	dB	V _{DS} = 10 V, V _{GS} = 0							f = 1 kHz	
														R _{gen} = 20 K, 2N4867 Series					
														5 K, 2N4867A Series					

*JEDEC registered data.

NS

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

2N4867 2N4867A 2N4868 2N4868A 2N4869 2N4869A

2

p-channel JFETs designed for . . .



**Performance Curves PS
See Section 4**

- Analog Switches
- Commutators
- Choppers

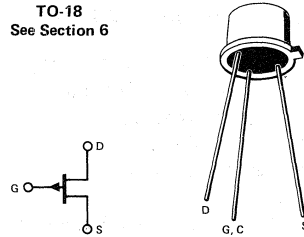
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 75 \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 6



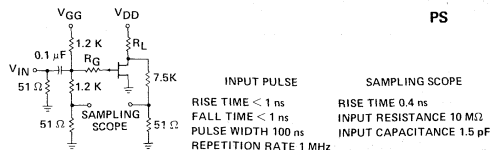
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N5018		2N5019		Unit	Test Conditions
	Min	Max	Min	Max		
1 BV _{GSS} Gate-Source Breakdown Voltage	30		30		V	I _G = 1 μA, V _{DS} = 0
2 I _{GSS} Gate Reverse Current		2		2	nA	V _{GS} = 15 V, V _{DS} = 0
3 I _{D(off)} Drain Cutoff Current		-10		-10	nA	V _{DS} = -15 V, V _{GS} = 12 V (2N5018)
4 I _{DGO} Drain Reverse Current		-10		-10	μA	V _{GS} = 7 V (2N5019)
5 I _{DGO} Drain Reverse Current		-2		-2	nA	V _{DG} = -15 V, I _S = 0
		-3		-3	μA	
7 V _{GS(off)} Gate-Source Cutoff Voltage		10		5	V	V _{DS} = -15 V, I _D = -1 μA
8 I _{DSS} Saturation Drain Current	-10		-5		mA	V _{DS} = -20 V, V _{GS} = 0
9 V _{DS(on)} Drain-Source ON Voltage		-0.5		-0.5	V	V _{GS} = 0, I _D = -6 mA (2N5018), I _D = -3 mA (2N5019)
10 r _{DS(on)} Static Drain-Source ON Resistance		75		150	Ω	I _D = -1 mA, V _{GS} = 0
11 r _{ds(on)} Drain-Source ON Resistance		75		150	Ω	I _D = 0, V _{GS} = 0
12 C _{iss} Common-Source Input Capacitance		45		45	pF	V _{DS} = -15 V, V _{GS} = 0
		10		10		V _{DS} = 0, V _{GS} = 12 V (2N5018), V _{GS} = 7 V (2N5019)
13 C _{rss} Common-Source Reverse Transfer Capacitance		10		10		f = 1 MHz
14 t _{d(on)} Turn-ON Delay Time		15		15	ns	V _{DD} = -6 V, V _{GS(on)} = 0 V _{GS(off)} I _{D(on)} R _L 2N5018 12 V -6 mA 910 Ω 2N5019 7 V -3 mA 1.8K Ω
15 t _r Rise Time		20		75		
16 t _{d(off)} Turn-OFF Delay Time		15		25		
17 t _f Fall Time		50		100		

*JEDEC registered data.

NOTE:

- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



monolithic dual n-channel JFETs designed for . . .



2N5045 2N5046 2N5047

High Gain Differential Amplifiers

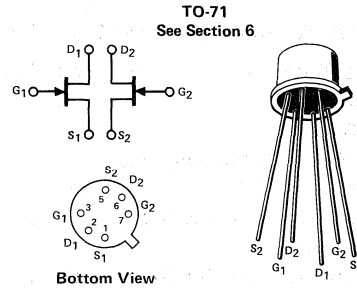
Performance Curves NQP
See Section 4

BENEFITS

- Minimum System Error and Calibration
5 mV Offset Maximum (2N5045)
- Low Drift
5 mV Drift Maximum (2N5045)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Forward Gate Current	30 mA
Total Dissipation (25°C Free Air Temp.)	400 mW
Power Derating (to 175°C)	2.67 mW/°C
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions				
		Min	Max	Min	Max	Min	Max						
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	S T A T I C	IGSS	Gate Reverse Current			-1	-1	μA	VGS = -50 V, VDS = 0 V				
					-0.25	-0.25	-0.25						
		VGS(off)	Gate-Source Cutoff Voltage						nA	VGS = -30 V, VDS = 0 V T = 150°C			
					-250	-250	-250						
IDSS	Drain Saturation Current		0.5	8.0	0.5	8.0	0.5	8.0	mA				
gfs	Common-Source Forward Transconductance		1.5	6.0	1.5	6.0	1.5	6.0	mmho	f = 1 kHz			
yfs	Common-Source Forward Admittance		1.5		1.5		1.5			f = 100 MHz			
gos	Common-Source Output Conductance			25		25		25	μmho	f = 1 kHz			
Ciss	Common-Source Input Capacitance			8.0		8.0		8.0	pF	f = 1 MHz			
Crss	Common-Source Reverse Transfer Capacitance			4.0		4.0		4.0		f = 10 Hz, RG = 1 MΩ			
NF	Spot Noise Figure			5.0		5.0			dB	f = 10 Hz			
en	Equivalent Short-Circuit Input Noise Voltage			200		200		nV/√Hz		f = 10 Hz			
M A T C H I N G	Δ	IGS1-IGS2		Differential Gate Current			10	10	10	nA	VGS = -15 V, VDS = 0 V TA = 100°C		
		IDS1/IDS2		Drain Current Ratio (Note 2)		0.95	1.0	0.9	1.0	0.8	1.0	—	VGS = 0 V, VDS = 15 V
		VGS1-VGS2		Differential Gate-Source Voltage			5	10	15	15	mV	VDS = 15 V ID = 50 μA ID = 200 μA	
		Δ VGS1-VGS2		Gate-Source Voltage Differential Drift (Note 3)			5	10	15	15		VDS = 15 V, ID = 200 μA TA = 25°C TB = -25°C TB = 100°C	
		gfs1/gfs2		Transconductance Ratio (Note 2)		0.95	1.0	0.9	1.0	0.8	1.0	—	VDS = 15 V, ID = 200 μA
gos1-gos2		Diff. Output Conductance			1.0	2.0	3.0	3.0	μmho		VDS = 15 V, ID = 200 μA f = 1 kHz		

*JEDEC registered data.

NOTES:

1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements.
2. Assumes smaller value in numerator.
3. Measured at end points, TA and TB.

NQP

2

p-channel JFETs designed for . . .



Performance Curves PS
See Section 4

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

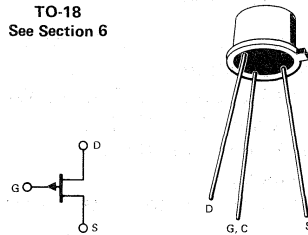
BENEFITS

- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $r_{DS(on)} < 75 \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7 \text{ pF}$
- High Off-Isolation $I_{D(off)} < 500 \text{ pA}$

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	.50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 6



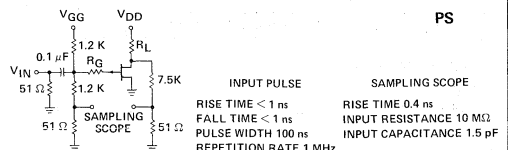
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N5114		2N5115		2N5116		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1 BV _{GSS} Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1 \mu\text{A}, V_{DS} = 0$
2 I _{GSS} Gate Reverse Current		500		500		500	pA	$V_{GS} = 20 \text{ V}, V_{DS} = 0$
3 I _{D(off)} Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15 \text{ V}, V_{GS} = 12 \text{ V}$ (2N5114)
4 I _{D(off)} Drain Cutoff Current		-1.0		-1.0		-1.0	μA	$V_{GS} = 7 \text{ V}$ (2N5115), $V_{GS} = 5 \text{ V}$ (2N5116)
5 V _{GS(off)} Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	$V_{DS} = -15 \text{ V}, I_D = -1 \text{ nA}$
6 I _{DSS} Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0, V_{DS} = -18 \text{ V}$ (2N5114) $V_{DS} = -15 \text{ V}$ (2N5115, 2N5116)
7 V _{GS(f)} Forward Gate-Source Voltage		-1		-1		-1	V	$I_G = -1 \text{ mA}, V_{DS} = 0$
8 V _{DS(on)} Drain-Source ON Voltage		-1.3		-0.8		-0.6	V	$V_{GS} = 0, I_D = -15 \text{ mA}$ (2N5114) $I_D = -7 \text{ mA}$ (2N5115), $I_D = -3 \text{ mA}$ (2N5116)
9 r _{DS(on)} Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0, I_D = -1 \text{ mA}$
10 r _{ds(on)} Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0, I_D = 0$
11 C _{iss} Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = -15 \text{ V}, V_{GS} = 0$
12 C _{rss} Common-Source Reverse Transfer Capacitance		7		7		7	pF	$V_{DS} = 0, V_{GS} = 12 \text{ V}$ (2N5114) $V_{GS} = 7 \text{ V}$ (2N5115), $V_{GS} = 5 \text{ V}$ (2N5116)
13 t _{d(on)} Turn-ON Delay Time		6		10		12	ns	$V_{DD} = -10 \text{ V}, -6 \text{ V}, -6 \text{ V}$
14 t _r Rise Time		10		20		30	ns	$V_{GS(off)} = 12 \text{ V}, 7 \text{ V}, 5 \text{ V}$
15 t _{d(off)} Turn-OFF Delay Time		6		8		10	ns	$R_L = 580 \Omega, /43 \Omega, 1800 \Omega$
16 t _f Fall Time		15		30		50	ns	$V_{GS(on)} = 0, 0, 0$ $I_{D(on)} = -15 \text{ mA}, -7 \text{ mA}, -3 \text{ mA}$

*JEDEC registered data.

NOTES:

- Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
- Pulse Test PW 300 μs , duty cycle $\leq 3\%$.



monolithic dual n-channel JFETs designed for . . .



- Differential Amplifiers
- FET Input Op Amps

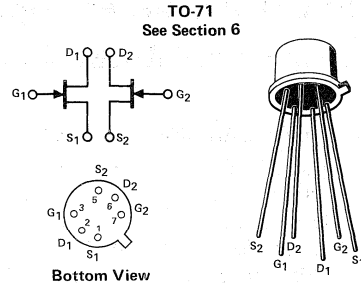
Performance Curves NQP See Section 4

BENEFITS

- Minimum System Error and Calibration
5 mV Maximum Offset (2N5196, 97)
- Low Drift
5 $\mu\text{V}/^\circ\text{C}$ Maximum (2N5196)
- Simplifies Amplifier Design
Low Output Conductance

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$ (Derate 2.56 mW/ $^\circ\text{C}$)	250 mW
Total Device Dissipation, $T_A = 85^\circ\text{C}$ (Derate 4.3 mW/ $^\circ\text{C}$)	500 mW
Storage Temperature Range	-65 to +200°C



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	1 I_{GSS} Gate Reverse Current		-25	pA	$V_{GS} = -30\text{ V}, V_{DS} = 0$	150°C
	2		-50	nA		
	3 BV_{GSS} Gate-Source Breakdown Voltage	-50			$I_G = -1\ \mu\text{A}, V_{DS} = 0$	
	4 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.7	-4	V		
	5 V_{GS} Gate-Source Voltage	-0.2	-3.8		$V_{DS} = 20\text{ V}, I_D = 1\ \text{nA}$	
D Y N A M I C	6 I_G Gate Operating Current		-15	pA	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$	125°C
	7 I_{DSS} Saturation Drain Current	0.7	7	mA		
	8 g_{fs} Common-Source Forward Transconductance	1000	4000	μmho	$V_{DS} = 20\text{ V}, V_{GS} = 0$	f = 1 kHz
	9 g_{fs} Common-Source Forward Transconductance	700	1600		$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$	
	10 g_{os} Common-Source Output Conductance		50		$V_{DS} = 20\text{ V}, V_{GS} = 0$	
11 g_{os} Common-Source Output Conductance		4		$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$		
12 C_{iss} Common-Source Input Capacitance		6	pF	$V_{DS} = 20\text{ V}, V_{GS} = 0$	f = 1 MHz	
13 C_{rss} Common-Source Reverse Transfer Capacitance		2			f = 100 Hz, $R_G = 10\ \text{M}\Omega$	
14 NF Spot Noise Figure		0.5	dB		f = 1 kHz	
15 \bar{e}_n Equivalent Short-Circuit Input Noise Voltage		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$		f = 1 kHz	

Characteristic	2N5196		2N5197		2N5198		2N5199		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max	Min	Max			
16 $ I_{G1} - I_{G2} $ Differential Gate Current		5		5		5		5	nA	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$ 125°C	
17 $\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	-	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	
18 $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	-	f = 1 kHz	
19 $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		5		10		15	mV	$V_{DG} = 20\text{ V}, I_D = 200\ \mu\text{A}$	
20 $\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$ Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	$\mu\text{V}/^\circ\text{C}$		$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$
21		5		10		20		40			$T_A = -55^\circ\text{C}$ $T_B = 25^\circ\text{C}$
22 $ g_{os1} - g_{os2} $ Differential Output Conductance		1		1		1		1	μmho	f = 1 kHz	

*JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.

2. Measured at end points, T_A and T_B .

NQP

2N5196 2N5197 2N5198 2N5199

2

n-channel JFETs designed for . . .



Performance Curves NIP
See Section 4

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

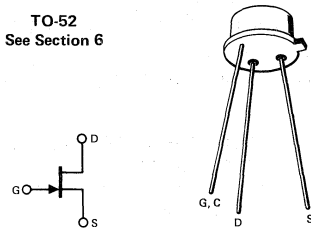
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 5 \Omega$ (2N5432)
- Small Error in Measurement Systems
 $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation
 $I_{D(off)} < 200$ pA
- High Speed
 $t_d(on) < 4$ ns
- Low Noise Audio-Frequency Amplification
 $e_n < 2$ nV/ $\sqrt{\text{Hz}}$ at 1 kHz Typical

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage -25 V
 Gate Current 100 mA
 Drain Current 400 mA
 Total Device Dissipation at 25°C
 Free-Air Temperature (Note 1) 300 mW
 Storage Temperature Range -65 to +150°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-52
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

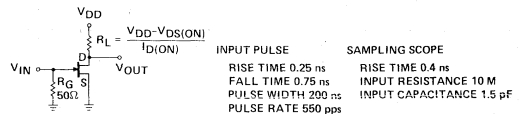
Characteristic	2N5432		2N5433		2N5434		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max			
1 I _{GSS} Gate Reverse Current		-200		-200		-200	pA	V _{GS} = -15 V, V _{DS} = 0	150°C
2		-200		-200		-200	nA		
3 BV _{GSS} Gate Source Breakdown Voltage	-25		-25		-25		V	I _G = -1 μA, V _{DS} = 0	
4 S I _{D(off)} Drain Cutoff Current		200		200		200	pA	V _{DS} = 5 V, V _{GS} = -10 V	150°C
	5 T		200		200		nA		
6 C V _{GS(off)} Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V _{DS} = 5 V, I _D = 3 nA	
7 I _{DSS} Saturation Drain Current (Note 2)	150		100		30		mA	V _{DS} = 15 V, V _{GS} = 0	
8 r _{DS(on)} Static Drain-Source ON Resistance	2	5		7		10	ohm	V _{GS} = 0, I _D = 10 mA	
9 V _{DS(on)} Drain-Source ON Voltage		50		70		100	mV		
10 r _{ds(on)} Drain-Source ON Resistance		5		7		10	ohm	V _{GS} = 0, I _D = 0	f = 1 kHz
11 D C _{iss} Common-Source Input Capacitance		30		30		30	pF	V _{DS} = 0, V _{GS} = -10 V	f = 1 MHz
12 Y C _{rss} Common-Source Reverse Transfer Capacitance		15		15		15			
13 S t _{d(on)} Turn-ON Delay Time		4		4		4	ns	V _{DD} = 1.5 V, 145 Ω (2N5432) V _{GS(on)} = 0, 143 Ω (2N5433) V _{GS(off)} = -12 V, 140 Ω (2N5434) I _{D(on)} = 10 mA	
14 W t _r Rise Time		1		1		1			
15 t _{d(off)} Turn-OFF Delay Time		6		6		6			
16 t _f Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:

- Derate linearly at the rate of 2.3 mW/°C.
- Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



matched dual n-channel JFETs designed for . . .



Performance Curves NQP
See Section 4

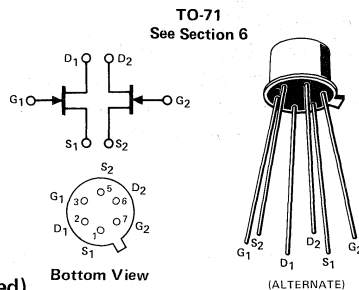
Low and Medium Frequency Differential Amplifiers

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

BENEFITS

- Minimum System Error and Calibration
5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
Output Conductance Less than
1 μ mho



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N5452		2N5453		2N5454		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max			
1 I _{GSS} Gate Reverse Current							pA	V _{GS} = -30 V, V _{DS} = 0 V T _A = 150°C	
		-100		-200		-100	nA		
2 BV _{GSS} Gate-Source Breakdown Voltage	-50		-50		-50			V _{DS} = 0 V, I _G = -1 μ A	
3 V _{GS(off)} Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5		V _{DS} = 20 V, I _D = 1 nA	
4 V _{GS} Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V _{DS} = 20 V, I _D = 50 μ A	
5 V _{GS(f)} Gate-Source Forward Voltage		2		2		2		V _{DS} = 0 V, I _G = 1 mA	
6 I _{DSS} Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0		V _{DS} = 20 V, V _{GS} = 0 V	
7 g _{fs} Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000		f = 1 kHz	
	1000		1000		1000		μ mho	f = 100 MHz	
8 g _{os} Common-Source Output Conductance		3.0		3.0		3.0		f = 1 kHz	
		1.0		1.0		1.0		V _{DS} = 20 V, I _D = 200 μ A	
9 C _{iss} Common-Source Input Capacitance		4.0		4.0		4.0		V _{DS} = 20 V, V _{GS} = 0 V	
10 C _{rss} Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		f = 1 MHz	
11 C _{dgo} Drain-Gate Capacitance		1.5		1.5		1.5		V _{DG} = 10 V, I _S = 0 V	
12 \bar{e}_n Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V _{DS} = 20 V, V _{GS} = 0 V f = 1 kHz	
13 NF Common-Source Spot Noise Figure		0.5		0.5		0.5		V _{DS} = 20 V, V _{GS} = 0 V, R _G = 10 M Ω f = 100 Hz	
14 I _{DSS1} /I _{DSS2} Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0		V _{DS} = 20 V, V _{GS} = 0 V	
15 V _{GS1} -V _{GS2} Differential Gate-Source Voltage		5.0		10.0		15.0		V _{DS} = 20 V, I _D = 200 μ A	
16 Δ V _{GS1} -V _{GS2} Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
17 g _{fs1} /g _{fs2} Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0			T = 25°C to +125°C
18 g _{os1} -g _{os2} Differential Output Conductance		0.25		0.25		0.25	μ mhos		f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NQP

2N5452 2N5453 2N5454
PREFERRED PARTS 2N5196 SERIES

2

n-channel JFETs designed for . . .



Performance Curves NRL, NP
See Section 4

- General Purpose Amplifiers
- Switches

BENEFITS

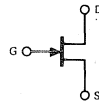
- Low Cost
- Automated Insertion Package

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	-65 to +150°C

TO-92
See Section 6

Plastic



Bottom View

Source & Drain
Interchangeable

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

1	S	Characteristic	2N5457			2N5458			2N5459			Unit	Test Conditions
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
2	T	I _{GSS} Gate Reverse Current		-0.01	-1.0		-0.01	-1.0		-0.01	-1.0	nA	V _{GS} = -15 V, V _{DS} = 0 T _A = +100°C
3	A	BV _{GSS} Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I _G = -10 μA, V _{DS} = 0
4	T	V _{GS(off)} Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V _{DS} = 15 V, I _D = 10 nA
5	C	I _{DSS} Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V _{DS} = 15 V, V _{GS} = 0 (Note 1)
6	D	g _{fs} Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	μmho	V _{DS} = 15 V, V _{GS} = 0
7	Y	g _{os} Common-Source Output Conductance		10	50		15	50		20	50	pF	
8	N	C _{iss} Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF	f = 1 MHz
9	M	C _{rss} Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0		
10	C	NF Noise Figure		0.04	3.0		0.04	3.0		0.04	3.0	dB	V _{DS} = 15 V, V _{GS} = 0 R _G = 1 MΩ NBW = 1 Hz f = 1 kHz

*JEDEC registered data

NOTE:

1. Pulse test pulsewidth = 2 ms.

NRL, NP

n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Mixers
- Oscillators
- Analog Switches

***ABSOLUTE MAXIMUM RATINGS (25°C)**

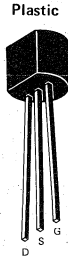
Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	360 mW
Derate above 25°C	3.27 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	240°C

Performance Curves NH
See Section 4

BENEFITS

- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
Very Little Charge Coupling
 $C_{rss} < 1.0$ pF

TO-92
See Section 6



Bottom View
Source & Drain
Interchangeable

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic	2N5484		2N5485		2N5486		Unit	Test Conditions		
	Min	Max	Min	Max	Min	Max				
1 S 2 T 3 A 4 I 5 C	IGSS Gate Reverse Current		-1.0	-1.0	-1.0	-1.0	nA	VGS = -20 V, VDS = 0 TA = +100°C		
	BVGSS Gate-Source Breakdown Voltage		-25	-25	-25	-25	V			
	VGS(off) Gate-Source Cutoff Voltage		-0.3	-3.0	-0.5	-4.0	-2.0	-6.0	VDS = 15 V, ID = 10 nA	
	IDSS Saturation Drain Current		1.0	5.0	4.0	10	8.0	20	VDS = 15 V, VGS = 0 (Note 1)	
6	9fs	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	VDS = 15 V, VGS = 0	
7	9os	Common-Source Output Conductance		50		60		75		f = 1 kHz
8		Re(Vfs) Common-Source Forward Transconductance	2,500							f = 100 MHz
9		Re(Vos) Common-Source Output Conductance		75		3,000		3,500		f = 400 MHz
10		Re(Vis) Common-Source Input Conductance		100		100		100		f = 100 MHz
11						1,000		1,000		f = 400 MHz
12		Ciss Common-Source Input Capacitance		5.0		5.0		5.0		
13		Crss Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0		f = 1 MHz
14		Coss Common-Source Output Capacitance		2.0		2.0		2.0		
15				2.5		2.5		2.5		VDS = 15 V, VGS = 0, RG = 1 MΩ f = 1 kHz
16		NF Noise Figure		3.0					VDS = 15 V, ID = 1 mA, RG = 1 kΩ f = 100 MHz	
17						2.0		2.0	VDS = 15 V, ID = 4 mA, RG = 1 kΩ f = 400 MHz	
18						4.0		4.0		
19		Gps Common-Source Power Gain	16	25					VDS = 15 V, ID = 1 mA f = 100 MHz	
20					18	30	18	30	VDS = 15 V, ID = 4 mA f = 400 MHz	
21					10	20	10	20		
22										
23										

* JEDEC registered data

NH

NOTE:

1 Pulse Test PW 300 μs, duty cycle ≤ 3%

2

2N5515 2N5516 2N5517 2N5518 2N5519
 2N5520 2N5521 2N5522 2N5523 2N5524

matched dual n-channel JFETs designed for . . .

■ Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$ (Derate 2.0 mW/°C)	250 mW
Total Device Dissipation, $T_A = 85^\circ\text{C}$ (Derate 3.0 mW/°C)	375 mW
Storage Temperature Range	-65 to + 200°C
Lead Temperature (1/16" from case for 30 seconds)	300°C

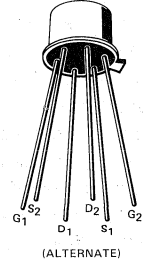
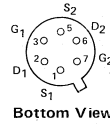
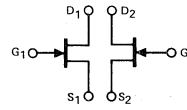


Performance Curves NQP/NS-D See Section 4

BENEFITS

- Ultra-Low Noise
 $\bar{e}_n = 8 \text{ nV}/\sqrt{\text{Hz}}$ at 10 Hz (Typical)
 $\bar{e}_n = 2 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz (Typical)
- Minimum System Error and Calibration
 5 mV Offset Maximum
 CMRR > 100 dB

TO-71
See Section 6



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions									
S T A T I C	1 I_{GSS} Gate Reverse Current		-250	pA	$V_{GS} = -30 \text{ V}, V_{DS} = 0$									
	3 BV_{GSS} Gate-Source Breakdown Voltage	-40	-250	nA	$I_G = -1 \mu\text{A}, V_{DS} = 0$									
	4 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.7	-4	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$									
	5 V_{GS} Gate Source Voltage	-0.2	-3.8											
	6 I_G Gate Operating Current		-100	pA	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$									
D Y N A M I C	7 I_{DSS} Saturation Drain Current (Note 1)	0.5	7.5	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$									
	8 g_{fs} Common-Source Forward Transconductance (Note 1)	1000	4000		$V_{DS} = 20 \text{ V}, V_{GS} = 0$									
	9 g_{fs} Common-Source Forward Transconductance (Note 1)	500	1000	μmho	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$									
	10 g_{os} Common-Source Output Conductance		10		$V_{DS} = 20 \text{ V}, V_{GS} = 0$									
	11 g_{os} Common-Source Output Conductance		1		$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$									
	12 C_{iss} Common-Source Input Capacitance		25	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$									
	13 C_{rss} Common-Source Reverse Transfer Capacitance		5	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$									
	14 \bar{e}_n Equivalent Short Circuit Input Noise Voltage	2N5515-19		30	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$								
		2N5520-24		15		$f = 10 \text{ Hz}$								
		2N5515-24		10		$f = 1 \text{ kHz}$								
Characteristic	2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		Unit	Test Conditions		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
M A T C H I N G	15 $ I_{G1} - I_{G2} $ Differential Gate Current		10		10		10		10		nA	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	125°C	
	16 I_{DSS1} Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	-	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	
	17 $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		5		10		15		15	mV	$V_{DG} = 20 \text{ V}, I_D = 200 \mu\text{A}$	
	18 $\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 3)		5		10		20		40		80	$\mu\text{V}/^\circ\text{C}$		$T_A = 25^\circ\text{C}$ $T_B = 125^\circ\text{C}$
				5		10		20		40		80		$\mu\text{V}/^\circ\text{C}$
19 $ g_{os1} - g_{os2} $ Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho	$f = 1 \text{ kHz}$		
20 $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Notes 1 and 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	-			
21 CMRR Common Mode Rejection Ratio (Note 4)	100		100		90						dB	$V_{DD} = 10 \text{ to } 20 \text{ V}, I_D = 200 \mu\text{A}$		

* JEDEC registered data.

NOTES:

1. Pulse test required, pulsewidth = 300 μs , duty cycle $\leq 3\%$.
2. Assumes smaller value in numerator.

3. Measured at end points, T_A and T_B .

4. $\text{CMRR} = 20 \log_{10} \left(\frac{\Delta V_{DD}}{\Delta|V_{GS1} - V_{GS2}|} \right), \Delta V_{DD} = 10 \text{ V}.$

NQP
NS-D

monolithic dual n-channel JFETs designed for . . .



Performance Curves NQP
See Section 4

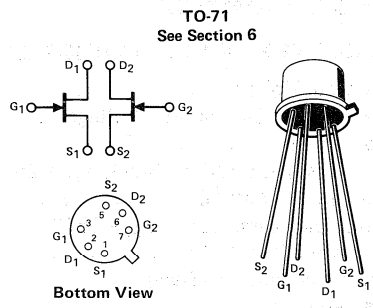
BENEFITS

- High Input Impedance
 $I_G < 50 \text{ pA}$
- Minimum System Error and Calibration
5 mV Offset Maximum (2N5545)

■ **General Purpose
Differential Amplifiers**

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	30 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate 1.67 mW/°C)	250 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate 2.67 mW/°C)	400 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 30 seconds)	300°C



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	I_{GSS} Gate Reverse Current		-100	pA	$V_{GS} = -30 \text{ V}, V_{DS} = 0$	$T_A = 150^\circ$
	BV_{GSS} Gate-Source Breakdown Voltage	-50		V		
	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5	-4.5		$I_G = -1 \mu\text{A}, V_{DS} = 0$	
	I_G Gate Operating Current		-50	pA	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	
	I_{DSS} Saturation Drain Current	0.5	8	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	
D Y N A M I C	g_{fs} Common-Source Forward Transconductance	1500	6000	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	f = 1 kHz
	g_{os} Common-Source Output Conductance		25			
	C_{iss} Common-Source Input Capacitance		6	pF		f = 1 MHz
	C_{rss} Common-Source Reverse Transfer Capacitance		2			
	NF Spot Noise Figure		3.5	dB	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	2N5545 f = 10 Hz, 2N5546 $R_G = 1 \text{ M}\Omega$
\bar{e}_n Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{\text{Hz}}}$	2N5545 f = 10 Hz 2N5546		

	Characteristic	2N5545		2N5546		2N5547		Unit	Test Conditions		
		Min	Max	Min	Max	Min	Max				
13	$ I_{G1} - I_{G2} $ Differential Gate Current		5		5		5	nA	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	$T_A = 125^\circ\text{C}$	
14	$\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	-	$V_{DS} = 15 \text{ V}, V_{GS} = 0$		
15	$ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		10		15	mV	$V_{DG} = 15 \text{ V}$	$I_D = 50 \mu\text{A}$	
			5		10		15			$I_D = 200 \mu\text{A}$	
16	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 2)		10		20		40	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$	$T_A = 25^\circ\text{C}$	
			10		20		40			$T_B = 125^\circ\text{C}$	
17	$\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	-			$T_A = -55^\circ\text{C}$
											$T_B = 25^\circ\text{C}$
18	$ g_{os1} - g_{os2} $ Differential Output Conductance		1		2		3	μmho		f = 1 kHz	

*JEDEC registered data.

NQP

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B .



matched dual n-channel JFETs designed for . . .



Performance Curves NC
See Section 4

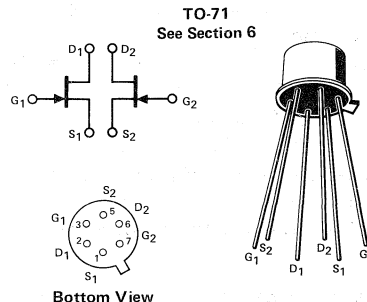
- **Wideband Differential Amplifiers**
- **Commutators**

BENEFITS

- High Gain
7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

Characteristic		Min	Max	Unit	Test Conditions				
S T A T I C	1 I_{GSS} Gate-Reverse Current		-100	pA	$V_{GS} = -20\text{ V}, V_{DS} = 0$ 150°C				
	2 BV_{GSS} Gate-Source Breakdown Voltage	-40	-200	nA					
	3 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5	-3	V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$				
	4 $V_{GS(f)}$ Gate-Source Voltage		1.0	V	$V_{DS} = 15\text{ V}, I_D = 1\ \text{nA}$				
	5 I_{DSS} Saturation Drain Current (Note 1)	5	30	mA	$V_{DS} = 0\text{ V}, I_G = 2\ \text{mA}$				
	6 $r_{DS(on)}$ Static Drain Source ON Resistance		100	Ω	$V_{DS} = 15\text{ V}, V_{GS} = 0$				
	7 $r_{DS(on)}$ Static Drain Source ON Resistance		100	Ω	$I_D = 1\ \text{mA}, V_{GS} = 0$				
D Y N A M I C	8 g_{fs} Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	$V_{DG} = 15\text{ V}, I_D = 2\ \text{mA}$				
	9 g_{os} Common-Source Output Conductance		45			$f = 1\ \text{kHz}$			
	10 C_{rss} Common-Source Reverse Transfer Capacitance		3	$f = 100\ \text{MHz}$					
	11 C_{iss} Common-Source Input Capacitance		12	$f = 1\ \text{kHz}$					
	12 NF Spot Noise Figure		1.0	$f = 1\ \text{MHz}$					
	13 \bar{e}_n Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		$f = 10\ \text{Hz}, R_g = 1\text{ M}$ $f = 10\ \text{Hz}$			
Characteristics		2N5564		2N5565		2N5566		Unit	Test Conditions
M A T C H I N G	14 I_{DSS1} I_{DSS2} Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	—	$V_{DS} = 15\text{ V}, V_{GS} = 0$
	15 $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		10		20	mV	$V_{DS} = 15\text{ V}, I_D = 2\ \text{mA}$
	16 $\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 3)		10		25		50	$\mu\text{V}/^\circ\text{C}$	
	17 $\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	—	

*JEDEC registered data.

NOTES:

1. Pulse test required, pulse width 300 μs , duty cycle $\leq 3\%$.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B .

NC

n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers

Performance Curves NC See Section 4

BENEFITS

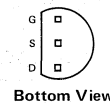
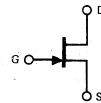
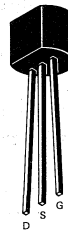
- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
 $t_{rise} < 5 \text{ ns}$ (2N5638)
- Low Insertion Loss
 $r_{DS(on)} < 30 \Omega$ (2N5638)
- Short Sample and Hold Aperture Time
 $C_{rss} < 4 \text{ pF}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at $T_{LEAD} = 25^\circ\text{C}$	625 mW
Derate above 25°C	5.68 mW/ $^\circ\text{C}$
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6

Plastic



Bottom View
Source & Drain Interchangeable

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

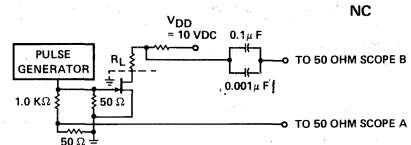
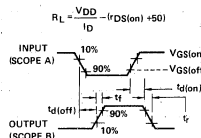
Characteristic	2N5638		2N5639		2N5640		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max		
1 BV_{GSS} Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = -10 \mu\text{A}, V_{DS} = 0$
2 I_{GSS} Gate Reverse Current		-1.0		-1.0		-1.0	nA	$V_{GS} = -15 \text{ V}, V_{DS} = 0$ $T_A = +100^\circ\text{C}$
3 $I_{D(off)}$ Drain Cutoff Current		-1.0		-1.0		-1.0	μA	
4 $I_{D(on)}$ Saturation Drain Current		1.0		1.0		1.0	nA	$V_{DS} = 15 \text{ V}, V_{GS} = -12 \text{ V}$ (2N5638)
5 I_{DSS} Saturation Drain Current		1.0		1.0		1.0	μA	$V_{GS} = -8 \text{ V}$ (2N5639), $V_{GS} = -6 \text{ V}$ (2N5640) $T_A = +100^\circ\text{C}$
6 $V_{DS(on)}$ Drain-Source ON Voltage	50		25		5.0		mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$ (Note 1)
7 $r_{DS(on)}$ Static Drain-Source ON Resistance		0.5		0.5		0.5	V	$V_{GS} = 0, I_D = 12 \text{ mA}$ (2N5638), $I_D = 6 \text{ mA}$ (2N5639), $I_D = 3 \text{ mA}$ (2N5640)
8 $r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	$I_D = 1 \text{ mA}, V_{GS} = 0$
9 C_{iss} Common-Source Input Capacitance		10		10		10	pF	$V_{GS} = -12 \text{ V}, V_{DS} = 0$ $f = 1 \text{ MHz}$
10 C_{rss} Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0	pF	
11 $t_{d(on)}$ Turn-On Delay Time		4.0		6.0		8.0	nsec	$V_{DD} = 10 \text{ V}$ $I_{D(on)} = 12 \text{ mA}$ (2N5638) $R_L = 800 \Omega$ (2N5638)
12 t_r Rise Time		5.0		8.0		10		$V_{GS(on)} = 0$ $I_{D(on)} = 6 \text{ mA}$ (2N5639) $R_L = 1.6 \text{ k}\Omega$ (2N5639)
13 $t_{d(off)}$ Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)} = -10 \text{ V}$ $I_{D(on)} = 3 \text{ mA}$ (2N5640) $R_L = 3.2 \text{ k}\Omega$ (2N5640)
14 t_f Fall Time		10		20		30		

2

* JEDEC registered data

NOTE:

1 Pulse test $PW \leq 300 \mu\text{sec}$, duty cycle $\leq 3.0\%$



SCOPE
TEKTRONIX 567A
OR EQUIVALENT

2N5638 2N5639 2N5640

2N5902 2N5903 2N5904 2N5905
2N5906 2N5907 2N5908 2N5909

matched dual n-channel JFETs designed for . . .



Performance Curves NT
See Section 4

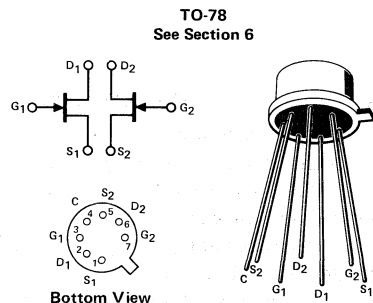
- Differential Amplifiers
- High Input Impedance Amplifiers

BENEFITS

- Matching Characteristics Specified
- High Input Impedance
 $I_G = 1 \text{ pA Max (2N5906-9)}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate 3 mW/°C)	367 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +200°C



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	2N5902-5		2N5906-9		Unit	Test Conditions	
	Min	Max	Min	Max			
1 I _{GSS} Gate Reverse Current		-5		-2	pA	V _{GS} = -20 V, V _{DS} = 0	125°C
2 BV _{GSS} Gate-Source Breakdown Voltage	-40		-40		nA	I _G = -1 μA, V _{DS} = 0	
3 V _{GS(off)} Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5	V	V _{DS} = 10 V, I _D = 1 nA	
4 V _{GS} Gate Source Voltage		-4		-4			
5 I _G Gate Operating Current		-3		-1	pA	V _{DS} = 10 V, I _D = 30 μA	
6 I _{DSS} Saturation Drain Current	30	500	30	500	μA		125°C
7 g _{fs} Common-Source Forward Transconductance	70	250	70	250	μmho	V _{DS} = 10 V, V _{GS} = 0	f = 1 kHz
8 g _{os} Common-Source Output Conductance		5		5			
9 C _{iss} Common-Source Input Capacitance		3		3	pF		f = 1 MHz
10 C _{rss} Common-Source Reverse Transfer Capacitance		1.5		1.5			
11 g _{fs} Common-Source Forward Transconductance	50	150	50	150	μmho	V _{DS} = 10 V, I _D = 30 μA	
12 g _{os} Common-Source Output Conductance		1		1			f = 1 kHz
13 e _n Equivalent Short Circuit Input Noise Voltage		0.2		0.1	μV/√Hz	V _{DS} = 10 V, V _{GS} = 0	f = 100 Hz, R _G = 10 M
14 NF Spot Noise Figure		3		1	dB		

Characteristic	2N5902, 6		2N5903, 7		2N5904, 8		2N5905, 9		Unit	Test Conditions	
	Min	Max	Min	Max	Min	Max	Min	Max			
17 I _{G1} - I _{G2} Differential Gate Current	2.0		2.0		2.0		2.0		nA	V _{DS} = 10 V, I _D = 30 μA, T _A = 125°C	2N5902-5 2N5906-9
18 I _{DSS1} / I _{DSS2} Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	-	V _{DS} = 10 V, V _{GS} = 0	
19 g _{fs1} / g _{fs2} Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	-		f = 1 kHz
20 V _{GS1} - V _{GS2} Differential Gate-Source Voltage		5		5		10		15	mV		
21 ΔV _{GS1} - V _{GS2} / ΔT Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	μV/°C	V _{DS} = 10 V, I _D = 30 μA	T _A = 25°C T _B = 125°C
22 g _{os1} - g _{os2} Differential Output Conductance		5		10		20		40			T _A = -55°C T _B = 25°C
23 g _{os1} - g _{os2} Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

* JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NT

matched dual n-channel JFETs designed for . . .



Performance Curves NZF-D
See Section 4

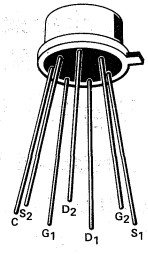
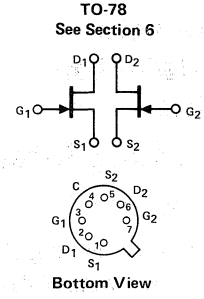
■ Wideband Differential Amplifiers

BENEFITS

- High Gain through 100 MHz
 $g_{fs} > 5000 \mu\text{mho}$
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



***ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)**

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	1 I _{GSS} Gate Reverse Current		-100	pA	V _{GS} = -15 V, V _{DS} = 0	T _A = 150°C
	2 BV _{GSS} Gate-Source Breakdown Voltage		-250	nA		
	3 V _{GS(off)} Gate-Source Cutoff Voltage	-25		V	I _G = -1 μA, V _{DS} = 0	
	4 V _{GS} Gate-Source Voltage	-1	-5		V _{DS} = 10 V, I _D = 1 nA	
	5 V _{GS} Gate-Source Voltage	-0.3	-4			
6 I _G Gate Operating Current			-100	pA	V _{DG} = 10 V, I _D = 5 mA	T _A = 125°C
			-100	nA		
7 I _{DSS} Saturation Drain Current (Note 1)		7	40	mA	V _{DS} = 10 V, V _{GS} = 0 V	
D Y N A M I C	8 g _{fs} Common-Source Forward Transconductance	5000	10,000	μmho	V _{DG} = 10 V, I _D = 5 mA	f = 1 kHz
	9 g _{fs} Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
	10 g _{os} Common-Source Output Conductance		100			f = 1 kHz
	11 g _{os} Common-Source Output Conductance		150			f = 100 MHz
	12 C _{iss} Common-Source Input Capacitance		5	pF		f = 1 MHz
	13 C _{rss} Common-Source Reverse Transfer Capacitance		1.2			
	14 ē _n Equivalent Short Circuit Input Noise Voltage		20	nV/√Hz		f = 10 kHz
	15 NF Spot Noise Figure		1	dB		f = 10 kHz R _G = 100K

Characteristic	2N5911		2N5912		Unit	Test Conditions	
	Min	Max	Min	Max			
16 G ₁ -G ₂ Differential Gate Current		20	20		nA	V _{DG} = 10 V, I _D = 5 mA T _A = 125°C	
17 I _{DSS1} / I _{DSS2} Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	-	V _{DS} = 10 V, V _{GS} = 0	
18 V _{GS1} -V _{GS2} Differential Gate-Source Voltage		10	15		mV	V _{DG} = 10 V, I _D = 5 mA	
19 Δ V _{GS1} -V _{GS2} / ΔT Gate-Source Voltage Differential Drift (Note 3)		20	40		μV/°C		T _A = 25°C T _B = 125°C
20 Δ V _{GS1} -V _{GS2} / ΔT Gate-Source Voltage Differential Drift (Note 3)		20	40		μV/°C		T _A = -55°C T _B = 25°C
21 g _{fs1} / g _{fs2} Transconductance Ratio (Note 2)	0.95	1	0.95	1	-	f = 1 kHz	

*JEDEC registered data.

NZF-D

NOTES:

1. Pulswidth ≤ 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.



enhancement-type p-channel MOSFETs designed for . . .



Performance Curves MRA
See Section 4

■ Ultra-High Input Impedance Amplifiers

**Electrometers
Smoke Detectors
pH Meters**

■ Digital Switching Interfaces

■ Analog Switching

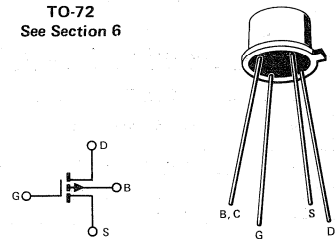
*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source or Gate-Source Voltage 3N163	-40 V
Drain-Source or Gate-Source Voltage 3N164	-30 V
Transient Gate-Source Voltage (Note 1)	±150 V
Drain Current	-50 mA
Storage Temperature	-65 to +200°C
Operating Junction Temperature	-55 to +150°C
Total Device Dissipation (Derate 3.0 mW/°C to 150°C)	375 mW
Lead Temperature 1/16" From Case For 10 Seconds	265°C

BENEFITS

- Rugged MOS Gate Minimizes Handling Problems
±150 V Transient Capability
- Low Gate-Leakage
Typically 0.02 pA
- High Off-Isolation as a Switch
 $I_{DSS} < 200 \mu A$

TO-72
See Section 6



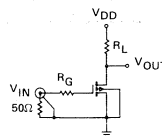
*ELECTRICAL CHARACTERISTICS (25°C and $V_{BS} = 0$ unless otherwise noted)

Characteristic	3N163		3N164		Unit	Test Conditions
	Min	Max	Min	Max		
1 2 3 4 I_{GSS} Gate-Body Leakage Current		-10			pA	$V_{GS} = -40 V, V_{DS} = 0$ $T_A = 125^\circ C$
		-25				
				-10		$V_{GS} = -30 V, V_{DS} = 0$ $T_A = 125^\circ C$
				-25		
5 6 7 8 9 10 11 12 S T A I C BV_{DSS} Drain-Source Breakdown Voltage	-40	-30			V	$I_D = -10 \mu A, V_{GS} = 0$ $I_S = -10 \mu A, V_{GD} = V_{BD} = 0$
	BV_{SDS} Source-Drain Breakdown Voltage	-40	-30			
V_{GS} Gate-Source Voltage	-3	-6.5	-2.5	-6.5	V	$V_{DS} = -15 V, I_D = -0.5 mA$ $V_{DS} = V_{GS}, I_D = -10 \mu A$
$V_{GS(th)}$ Gate-Source Threshold Voltage	-2	-5	-2	-5		
I_{DSS} Drain Cutoff Current		-200		-400	pA	$V_{DS} = -15 V, V_{GS} = 0$ $V_{SD} = -20 V, V_{GD} = 0, V_{DB} = 0$
I_{SDS} Source Cutoff Current		-400		-800		
$I_{D(on)}$ ON Drain Current	-5	-30	-3	-30	mA	$V_{DS} = -15 V, V_{GS} = -10 V$ $V_{GS} = -20 V, I_D = -100 \mu A$
$r_{DS(on)}$ Drain-Source ON Resistance		250		300		
13 14 15 16 17 18 19 20 D Y N A M I C S W g_{fs} Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	μmho	$V_{DS} = -15 V,$ $I_D = -10 mA$ $f = 1 kHz$
	g_{os} Common-Source Output Conductance		250			
C_{iss} Common-Source Input Capacitance		2.5		2.5	pF	$V_{DS} = -15 V, I_D = -10 mA$ $f = 1 MHz$
C_{rss} Common-Source Reverse Transfer Capacitance		0.7		0.7		
C_{oss} Common-Source Output Capacitance		3		3		
$t_{d(on)}$ Turn-ON Delay Time		12		12	ns	$V_{DD} = -15 V$ $I_{D(on)} = -10 mA$ $R_G = R_L = 1.5 k\Omega$
t_r Rise Time		24		24		
t_{off} Turn-OFF Time		50		50		

*JEDEC registered data

NOTE:

1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE
RISE TIME $\leq 2 ns$
PULSE WIDTH $\geq 200 ns$

SAMPLING SCOPE
 $t_r \leq 0.2 ns$
 $C_{IN} \leq 2 pF$
 $R_{IN} \geq 10 M\Omega$

MRA

current regulator diodes designed for . . .



Performance Curves
NKL NKM NKO See Section 4

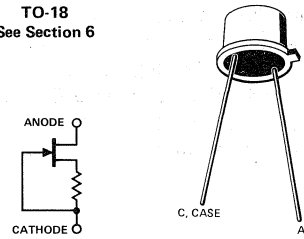
- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

- BENEFITS**
- Simple Two Lead Current Source
 - Current Insensitive to Temperature Changes
Temperature Coefficient Better Than 1500 ppm/°C On All Devices
 - TO-18 Package for Improved Current Control
 - Simplifies Floating Current Sources
No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage 100 V
 Forward Current 20 mA
 Reverse Current 50 mA
 Thermal Resistance θ_{JC} 100°C/W
 Power Dissipation at $T_C = 25^\circ\text{C}$ 1.25 W
 Operating Junction Temperature -55 to +150°C
 Storage Temperature -55 to +200°C

TO-18
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol Parameter	I _{F1}		Z _d		Z _k		V _L		POV		θ_1			G E O M				
	Regulator Current		Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage		Temperature Coefficient							
	V _F = 25 V (Note 1)		V _F = 25 V (Note 2)		V _F = 6 V		I _F = 0.8 I _{F1} (Min) (Note 3)		I _F = 1.1 I _{F1} (Max) (Note 4)		V _F = 25 V -55°C ≤ T _A ≤ 25°C				V _F = 25 V 0°C ≤ T _A ≤ 50°C			V _F = 25 V 25°C ≤ T _A ≤ 125°C
Test Conditions	mA		MΩ		MΩ		Volts		Volts		ppm/°C							
	Nom	Max	Min	Typ	Min	Typ	Max	Typ	Min	Max	Typ	Typ	Typ	Typ				
Units	mA		MΩ		MΩ		Volts		Volts		ppm/°C							
CR022	0.22	0.198	0.242	13.0	16.0	2.75	3.5	1.0	0.40	100	+1350	+1050	+750	N K L				
CR024	0.24	0.216	0.264	10.0	14.0	2.35	3.0	1.0	0.45	100	+1200	+900	+600					
CR027	0.27	0.243	0.297	9.0	13.0	1.95	2.8	1.0	0.50	100	+1000	+700	+400					
CR030	0.30	0.270	0.330	8.0	12.0	1.60	2.5	1.0	0.55	100	+800	+500	+200					
CR033	0.33	0.297	0.363	6.6	11.0	1.35	2.2	1.0	0.60	100	+600	+300	-50					
CR039	0.39	0.351	0.429	4.10	9.5	1.00	1.90	1.05	0.70	100	+300	+50	-300					
CR043	0.43	0.387	0.473	3.30	8.6	0.87	1.65	1.05	0.78	100	+150	-150	-450					
CR047	0.47	0.423	0.517	2.70	8.0	0.75	1.50	1.10	0.85	100	-50	-300	-600					
CR056	0.56	0.504	0.616	1.90	6.5	0.56	1.25	1.20	0.98	100	-300	-600	-900					
CR062	0.62	0.558	0.682	1.55	6.2	0.47	1.15	1.30	1.10	100	-500	-800	-1100					
CR068	0.68	0.612	0.748	1.35	8.5	0.400	1.70	1.15	0.70	100	+850	+400	-50	N K M				
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	+650	+200	-250					
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	+450	+50	-450					
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	+300	-150	-600					
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	+150	-300	-750					
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	+50	-450	-900					
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	-150	-600	-1050					
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	-300	-750	-1200					
CR140	1.40	1.26	1.54	0.54	2.5	0.115	0.52	1.55	1.30	100	-400	-850	-1300					
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	-500	-950	-1400					
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	+650	+350	+50	N K O				
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	+500	+200	-100					
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	+350	+50	-250					
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	+200	-100	-350					
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	+50	-200	-450					
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	-100	-300	-550					
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	-250	-450	-700					
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	-400	-600	-800					
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	-550	-750	-900					
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	-700	-850	-1000					
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	-850	-950	-1100					
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	-1000	-1100	-1200					

NOTES:

- Pulse test — steady state currents may vary.
- Pulse test — steady state impedances may vary.
- Min V_F required to insure I_F > 0.8 I_{F1}(min).
- Max V_F where I_F < 1.1 I_{F1}(max) is guaranteed.

NKL, NKM, NKO

current regulator diodes designed for . . .



- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

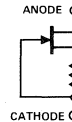
BENEFITS

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at $T_C = 25^\circ\text{C}$	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C

TO-18
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	POV	I_{F1}			Z_d		V_L	
Parameter	Peak Operating Voltage	Regulator Current			Dynamic Impedance		Limiting Voltage	
Test Conditions	$I_F = 1.1 I_{F1}(\text{Max})$ (Note 1)	$V_F = 25 \text{ V}$ (Note 2)			$V_F = 25 \text{ V}$ (Note 3)		$I_F = 0.8 I_{F1}(\text{Min})$ (Note 4)	
Units	Maximum Volts	Nom	(mA) Min	Max	Min	(m Ω) Typ	Max	(V) Typ
CRR0240	100	0.240	0.180	0.300	8	13	1.0	0.5
CRR0360	100	0.360	0.270	0.450	3.3	9.5	1.05	0.7
CRR0560	100	0.560	0.420	0.700	1.5	6	1.30	1.1
CRR0800	100	0.800	0.600	1.000	0.8	5.2	1.35	0.85
CRR1250	100	1.250	0.937	1.560	0.5	2.5	1.60	1.3
CRR1950	100	1.950	1.460	2.440	0.37	0.8	1.95	0.65
CRR2900	100	2.900	2.160	3.600	0.28	0.56	2.35	0.9
CRR4300	100	4.300	3.240	5.400	0.22	0.35	3.00	1.45

NOTES:

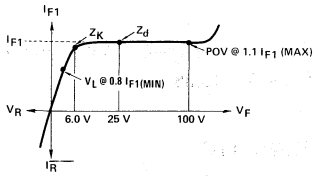
1. Max V_F where $I_F < 1.1 I_{F1}(\text{max})$ is guaranteed.
2. Pulse test — steady state current may vary.
3. Pulse test — steady state impedances may vary.
4. Min V_F required to insure $I_F > 0.8 I_{F1}(\text{min})$.

CRR0240-560 — NKL
CRR0800-1250 — NKM
CRR1950-4300 — NKO

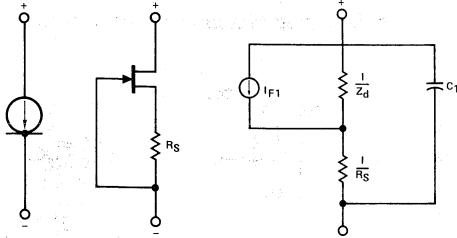
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

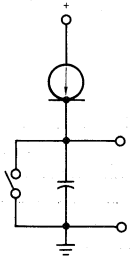
Current-Limiter Diode V-I Characteristic



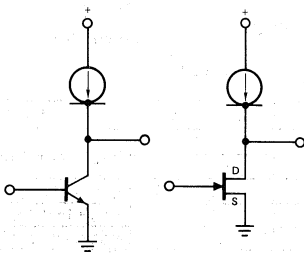
EQUIVALENT CIRCUIT



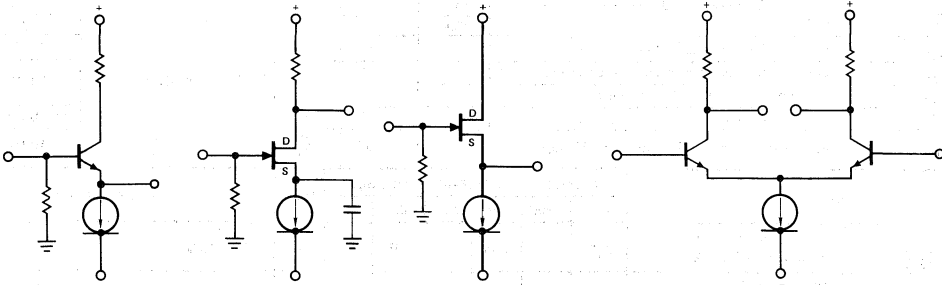
Constant-Current Timing Circuits



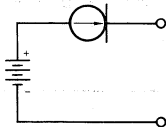
Collector or Drain Hi-Z Load Resistors



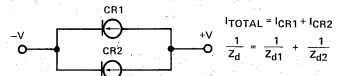
Emitter or Source Biasing



Constant-Current Supply or Current-Limiting Element



Parallel Operation

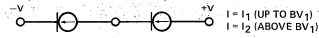


$$I_{TOTAL} = I_{CR1} + I_{CR2}$$

$$\frac{1}{Z_d} = \frac{1}{Z_{d1}} + \frac{1}{Z_{d2}}$$

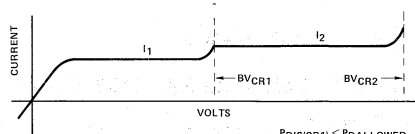
Series Operation

(When $I_1 < I_2$, that is $I_2 - I_1 < 0.2 I_1$)



$$I = I_1 \text{ (UP TO BV}_1\text{)}$$

$$I = I_2 \text{ (ABOVE BV}_1\text{)}$$



$$P_{DIS(CR1)} < P_{DALLOWED}$$

$$BV \text{ (FOR SERIES DEVICES)}$$

$$= BV_1 + BV_2$$

SYMBOLS AND DEFINITIONS

- A Anode (Drain)
- C Cathode (Source and Gate Shorted)
- I_F Forward Current (Anode Positive)
- I_{F1} Current at a specified Test Voltage, V_F
- POV Peak Operating Voltage
- θ_1 Current Temperature Coefficient
- θ_{JC} Thermal Resistance Junction to Case
- θ_{JA} Thermal Resistance Junction to Ambient
- Z_K Knee AC Impedance at specified V_F . Z_K should be as high as possible and is specified as a minimum.
- Z_d Dynamic Impedance at specified V_F . Z_d is specified as a minimum.

matched dual n-channel JFETs designed for . . .



Performance Curves NC-D
See Section 4

- **Wideband Differential Amplifiers**
- **Commutators**

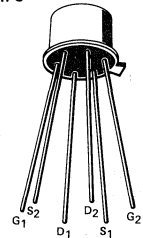
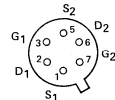
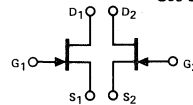
BENEFITS

- High Gain
7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions					
S T A T I C	I_{GSS} Gate-Reverse Current		-100	μA	$V_{GS} = -20\text{ V}, V_{DS} = 0$	150°C				
	BV_{GSS} Gate-Source Breakdown Voltage	-40	-200	nA						
	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5	-3	V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$					
	$V_{GS(f)}$ Gate-Source Voltage		2		$V_{DS} = 15\text{ V}, I_D = 1\ \text{nA}$					
	I_{DSS} Saturation Drain Current (Note 1)	5	50	mA	$V_{DS} = 0\text{ V}, I_G = 2\ \text{mA}$					
	$r_{DS(on)}$ Static Drain Source ON Resistance		100	Ω	$V_{DS} = 15\text{ V}, V_{GS} = 0$					
	g_{fs} Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	$V_{DG} = 15\text{ V}, I_D = 2\ \text{mA}$	f = 1 kHz				
g_{os} Common-Source Output Conductance	7000	65		f = 100 MHz						
C_{rss} Common-Source Reverse Transfer Capacitance		3	pF	f = 1 kHz						
C_{iss} Common-Source Input Capacitance		12		f = 1 MHz						
NF Spot Noise Figure		1.0	dB	f = 10 Hz, $R_g = 1\text{ M}$						
\bar{e}_n Equivalent Short Circuit Input Noise Voltage		50	$\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$	f = 10 Hz						
Characteristics		DN5564		DN5565		DN5566		Unit	Test Conditions	
M A T C H I N G	I_{DSS1} I_{DSS2} Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	—	$V_{DS} = 15\text{ V}, V_{GS} = 0$	
	$ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		10		20	mV	$V_{DS} = 15\text{ V}, I_D = 2\ \text{mA}$	
	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 3)		10		25		50	$\frac{\mu\text{V}}{^\circ\text{C}}$		
	g_{fs1} g_{fs2} Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	—		

NOTES:

1. Pulse test required, pulse width 300 μs , duty cycle $\leq 3\%$.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B .

NC-D



matched dual n-channel JFETs designed for...

Performance Curves NC-D
See Section 4

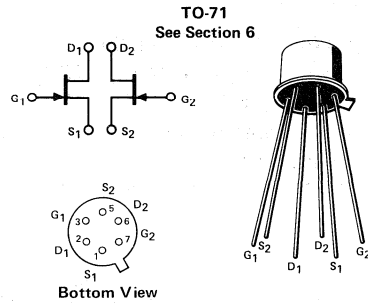
■ Dual FET

BENEFITS

- High Density
- Matched Switch Resistance
- Constant $r_{DS(on)}$ with Signal

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	-65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Max	Unit	Test Conditions	
S T A T I C	C	I_{GSS} Gate-Reverse Current		-100	pA	$V_{GS} = -20\text{ V}, V_{DS} = 0$	150°C
				-200	nA		
		BV_{GSS} Gate-Source Breakdown Voltage	-40			$I_G = 1\ \mu\text{A}, V_{DS} = 0$	
		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5	-3	V	$V_{DS} = 15\text{ V}, I_D = 1\ \text{nA}$	
		$V_{GS(f)}$ Gate-Source Voltage		2.0		$V_{DS} = 0\text{ V}, I_G = 2\ \text{mA}$	
D Y N	M A T C H	I_{DSS} Saturation Drain Current (Note 1)	5	60	mA	$V_{DS} = 15\text{ V}, V_{GS} = 0$	
		$r_{DS(on)}$ Static Drain Source ON Resistance		100	Ω	$I_D = 1\ \text{mA}, V_{GS} = 0$	
		C_{gd} Drain-Gate Capacitance		7	pF	$V_{GS} = -10\text{ V}$	f = 1 MHz
C_{gs} Gate-Source Capacitance		7		$V_{DS} = 10\text{ V}$			
		I_{DSS1} I_{DSS2} Saturation Drain Current Ratio (Notes 1 and 2)	0.9	1	-	$V_{DS} = 15\text{ V}, V_{GS} = 0$	
		$ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		20	mV		
		g_{fs1} g_{fs2} Transconductance Ratio (Notes 1 and 2)	0.9	1	-	f = 1 kHz	

NOTES:

NC

1. Pulse test required, pulse width 300 μs , duty cycle $\leq 3\%$.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B .

dual pico ampere diodes designed for . . .



- Clipping Circuits
- Diode Switching
- High Impedance Protection Circuits

BENEFITS

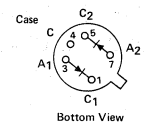
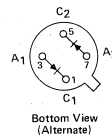
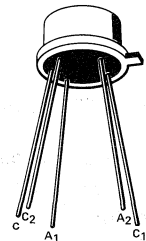
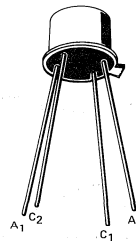
- Very High Off-Isolation
1 pA Max (DPAD1)
- High Isolation Between Diodes
20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Gate Current, Each Side 50 mA
 Total Device Dissipation @ T_A = 25°C
 Derate 4.0 mW/°C to 125°C 400 mW
 Storage Temperature Range -55 to +125°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-71
 (Pins 2 and 6 Removed)
 See Section 6

TO-78
 (DPAD1 Only)
 See Section 6



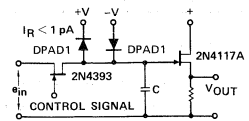
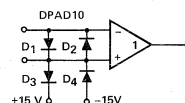
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION
1	S T A T I C I _R Reverse Current			-1	pA	V _R = -20 V
2				-2		
3				-5		
4				-10		
5				-20		
6				-50		
7				-100		
8	B V R Reverse Breakdown Voltage	-45		-120	V	I _R = -1 μA
9			-35			
10	V _F Forward Voltage Drop		0.8	1.5		I _F = 1 mA
11	D Y N C R Capacitance			0.8	pF	V _R = -5 V, f = 1 MHz
12				2.0		
13	M A T C _{R1} - C _{R2} Differential Capacitance		0.1	0.2	pF	V _{R1} = V _{R2} = -5 V, f = 1 MHz

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D₁ and D₂ Common mode input voltage limited by DPADS D₃ and D₄ to ±15 V.

Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



n-channel JFETs designed for . . .



Performance Curves NT
See Section 4

- **Ultra-High Input Impedance Amplifiers**
- Electrometers**
- pH Meters**
- Smoke Detectors**

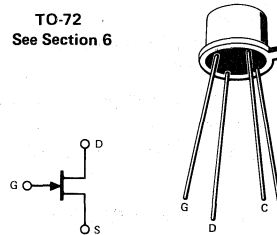
BENEFITS

- Low Power
 $I_{DSS} < 0.2 \text{ mA}$ (FN4117)
- Minimum Circuit Loading
 $I_{GSS} < 1 \text{ pA}$ (FN4117A Series)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) -40 V
 Gate-Current 50 mA
 Total Device Dissipation
 (Derate 2 mW/°C to 175°C) 300 mW
 Storage Temperature Range -65 to +175°C
 Lead Temperature
 (1/16" from case for 10 seconds) 255°C

TO-72
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

1	2	3	4	5	6	7	8	9	10	11	Characteristic	FN4117		FN4118		FN4119		Unit	Test Conditions	
												FN4117A		FN4118A		FN4119A				
												Min	Max	Min	Max	Min	Max			
S	T	A	T	I	GSS	Gate Reverse Current FN4117 Series Only		-10	-10	-10	pA	V _{GS} = -20 V, V _{DS} = 0	150°C							
								-25	-25	-25	nA									
S	T	A	T	I	GSS	Gate Reverse Current FN4117A Series Only		-5	-5	-5	pA	V _{GS} = -20 V, V _{DS} = 0	150°C							
								-2.5	-2.5	-2.5	nA									
S	T	A	T	I	V _{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40	V	I _G = -1 μA, V _{DS} = 0							
S	T	A	T	I	V _{GS(off)}	Gate-Source Cutoff Voltage	-0.6	2.0	-1	-3	-2	-6	V	V _{DS} = 10 V, I _D = 1 nA						
S	T	A	T	I	DSS	Saturation Drain Current (Note 2)	0.03	0.2	0.08	0.4	0.20	1.2	mA	V _{DS} = 10 V, V _{GS} = 0						
D	Y	N	A	M	I	C	g _{fs}	Common-Source Forward Transconductance (Note 2)		70	210	80	250	100	330	μmho	V _{DS} = 10 V, V _{GS} = 0	f = 1 kHz		
D	Y	N	A	M	I	C	g _{os}	Common-Source Output Conductance			3		5		10	pF	f = 1 MHz			
D	Y	N	A	M	I	C	C _{iss}	Common-Source Input Capacitance			3		3		3	pF	f = 1 MHz			
D	Y	N	A	M	I	C	C _{rss}	Common-Source Reverse Transfer Capacitance			1.5		1.5		1.5	pF	f = 1 MHz			

*JEDEC registered data.

NT

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

FN4117 FN4117A FN4118 FN4118A FN4119 FN4119A
SEE ALSO 2N4177 SERIES

2

n-channel JFETs designed for . . .



- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC See Section 4

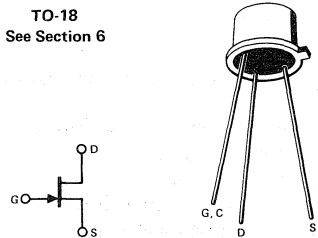
BENEFITS

- Low Insertion Loss, High Accuracy in Test Systems r_{ON}
- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive
High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100 \text{ pA}$
- High Speed $t_{ON} < 20 \text{ ns}$

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage -40 V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Case Temperature
 (Derate 10 mW/°C) 1.8 W
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-18
See Section 6

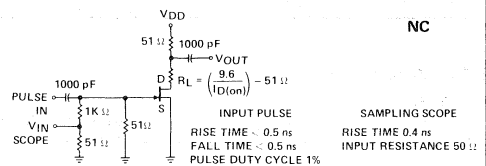


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	FN4392		FN4393		Unit	Test Conditions	
	Min	Max	Min	Max			
1 I_{GSS} Gate Reverse Current		-100		-100	pA	$V_{GS} = -20 \text{ V}, V_{DS} = 0$	
2 BV_{GSS} Gate-Source Breakdown Voltage	-40		-40		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$	150°C
3 $I_{D(off)}$ Drain Cutoff Current				100	pA	$V_{DS} = 20 \text{ V}$	$V_{GS} = -5 \text{ V}$
				200	nA		
		100			pA		
4 $I_{D(off)}$ Drain Cutoff Current		200			nA		
8 $V_{GS(f)}$ Gate-Source Forward Voltage		1		1	V	$I_G = 1 \text{ mA}, V_{DS} = 0$	
9 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-2	-5	-0.5	-3	V	$V_{DS} = 20 \text{ V}, I_D = 1 \text{ nA}$	
10 I_{DSS} Saturation Drain Current (Note 1)	25	100	5	60	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	
12 $V_{DS(on)}$ Drain Source ON Voltage				0.4	V	$V_{GS} = 0$	$I_D = 3 \text{ mA}$
		0.4					$I_D = 6 \text{ mA}$
							$I_D = 12 \text{ mA}$
14 $r_{DS(on)}$ Static Drain-Source ON Resistance		60		100	Ω	$V_{GS} = 0, I_D = 1 \text{ mA}$	
15 $r_{ds(on)}$ Drain-Source ON Resistance		60		100	Ω	$V_{GS} = 0, I_D = 0$	$f = 1 \text{ kHz}$
16 C_{iss} Common-Source Input Capacitance		14		14	pF	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	
18 C_{rss} Common-Source Reverse Transfer Capacitance				3.5	pF	$V_{DS} = 0$	$V_{GS} = -5 \text{ V}$
		3.5					$V_{GS} = -7 \text{ V}$
							$V_{GS} = -12 \text{ V}$
20 $t_{d(on)}$ Turn-ON Delay Time		15		15	ns	$V_{DD} = 10 \text{ V}, V_{GS(on)} = 0$	
21 t_r Rise Time		5		5	ns	$I_{D(on)} \quad V_{GS(off)} \quad R_L$	
22 $t_{d(off)}$ Turn-OFF Delay Time		35		50	ns	FN4392 6 -7 1.6K Ω	
23 t_f Fall Time		20		30	ns	FN4393 3 -5 3.2K Ω	

NOTE:

1. Pulse test required, pulse width = 300 μs , duty cycle $\leq 3\%$.



n-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Commutators

Performance Curves NVA
See Section 4

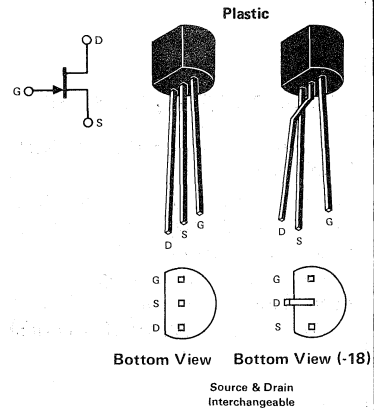
BENEFITS

- Very Low Insertion Loss
 $r_{DS(on)} < 3 \Omega$ (J105)
- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive
High Isolation Resistance from Driver

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage - 25 V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J105			J106			J107			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 I _{GSS} Gate Reverse Current (Note 1)			-3			-3			-3	nA	V _{DS} = 0 V, V _{GS} = -15 V
2 V _{GS(off)} Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V _{DS} = 5 V, I _D = 1 μA
3 BV _{GSS} Gate-Source Breakdown Voltage	-25			-25							V _{DS} = 0 V, I _G = -1 μA
4 I _{DSS} Drain Saturation Current (Note 2)	500		200			100				mA	V _{DS} = 15 V, V _{GS} = 0 V
5 I _{D(off)} Drain Cutoff Current (Note 1)			3			3			3	nA	V _{DS} = 5 V, V _{GS} = -10 V
6 r _{DS(on)} Drain Source ON Resistance			3			6			8	Ω	V _{DS} ≤ 0.1 V, V _{GS} = 0 V
7 C _{dg(off)} Drain Gate OFF Capacitance			35			35			35	pF	V _{DS} = 0 V, V _{GS} = -10 V f = 1 MHz
8 C _{sg(off)} Source Gate OFF Capacitance			35			35			35		
9 C _{dg(on)} + C _{sg(on)} Drain Gate plus Source Gate ON Capacitance			160			160			160		
10 t _{d(on)} Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions V _{DD} 1.5 V 1.5 V 1.5 V V _{GS(off)} -12 V -7 V -5 V R _L 50 Ω 50 Ω 50 Ω
11 t _r Rise Time		20			20			20			
12 t _{d(off)} Turn Off Delay Time		15			15			15			
13 t _f Fall Time		20			20			20			

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NVA

J105 J106 J107
J105-18 J106-18 J107-18

2

J108 J109 J110
J109-18 J110-18
J108-18

n-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Commutators
- Low Noise Audio Amplifiers

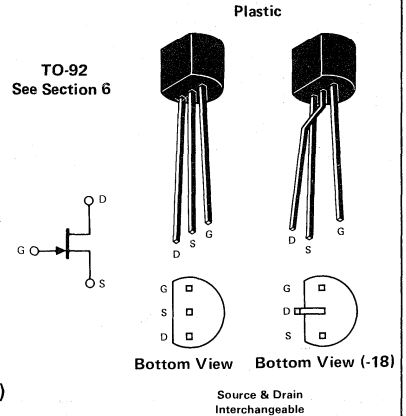
Performance Curves NIP
See Section 4

BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
 $r_{DS(on)} < 8 \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
Purely Resistive
High Isolation Resistance from Driver
- Fast Switching
 $t_{d(on)} + t_r = 5 \text{ ns Typical}$
- Low Noise
 $\bar{e}_n = 6 \text{ nV}/\sqrt{\text{Hz}}$ at 10 Hz, Typ (J110)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage-25V
Gate Current 50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C) 360 mW
Operating Temperature Range-55 to 135°C
Storage Temperature Range-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J108			J109			J110			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 S I_{GSS} Gate Reverse Current (Note 1)			-3			-3			-3	nA	$V_{DS} = 0 \text{ V}, V_{GS} = -15 \text{ V}$
2 T $V_{GS(off)}$ Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	V	$V_{DS} = 5 \text{ V}, I_D = 1 \mu\text{A}$
3 A BV_{GSS} Gate-Source Breakdown Voltage	-25			-25					-25	V	$V_{DS} = 0 \text{ V}, I_G = -1 \mu\text{A}$
4 J I_{DSS} Drain Saturation Current (Note 2)	80			40					10	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$
5 C $I_{D(off)}$ Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5 \text{ V}, V_{GS} = -10 \text{ V}$
6 $r_{DS(on)}$ Drain-Source ON Resistance			8			12			18	Ω	$V_{DS} \leq 0.1 \text{ V}, V_{GS} = 0 \text{ V}$
7 $C_{dg(off)}$ Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0 \text{ V}, V_{GS} = -10 \text{ V}$ $V_{DS} = V_{GS} = 0$
8 $C_{sg(off)}$ Source-Gate OFF Capacitance			15			15			15		
9 D $C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		
10 M $t_{d(on)}$ Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions J108 J109 J110 $V_{DD} \quad 1.5 \text{ V} \quad 1.5 \text{ V} \quad 1.5 \text{ V}$ $V_{GS(off)} \quad -12 \text{ V} \quad -7 \text{ V} \quad -5 \text{ V}$ $R_L \quad 150 \Omega \quad 150 \Omega \quad 150 \Omega$
11 t_r Rise Time		1		1		1		1			
12 C $t_{d(off)}$ Turn OFF Delay Time		6		6		6		6			
13 t_f Fall Time		30		30		30		30			

NOTES:
1. Approximately doubles for every 10°C increase in T_A .
2. Pulse Test duration 300 μs ; duty cycle $\leq 3\%$.

NIP

n-channel FETs designed for . . .



- Analog Switches
- Choppers
- Commutators

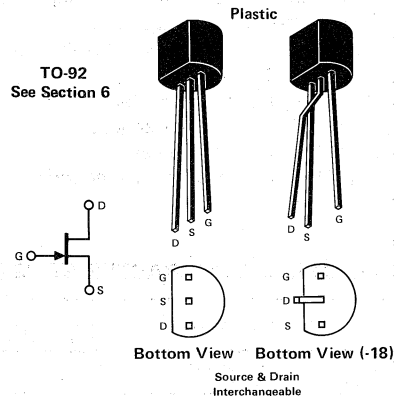
Performance Curves NC See Section 4

BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
 - $r_{DS(on)} < 30 \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
 - Purely Resistive
 - High Isolation Resistance from Driver
- Fast Switching
 - $t_{d(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
 - $C_{gd(off)} < 5$ pF
 - $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-35V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J111			J112			J113			UNIT	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 I _{GSS} Gate Reverse Current (Note 1)			-1			-1			-1	nA	V _{DS} = 0 V, V _{GS} = -15 V
2 V _{GS(off)} Gate Source Cutoff Voltage	-3		-10	-1		-5		-0.5		V	V _{DS} = 5 V, I _D = 1 μA
3 BV _{GSS} Gate Source Breakdown Voltage	35		35					-35			V _{DS} = 0 V, I _G = -1 μA
4 I _{DSS} Drain Saturation Current (Note 2)	20		5					2		mA	V _{DS} = 15 V, V _{GS} = 0 V
5 I _{D(off)} Drain Cutoff Current (Note 1)			-1			-1			-1	nA	V _{DS} = 5 V, V _{GS} = -10 V
6 r _{DS(on)} Drain Source ON Resistance			30			50			100	Ω	V _{DS} = 0.1 V, V _{GS} = 0 V
7 C _{dg(off)} Drain Gate OFF Capacitance			5			5			5	pF	V _{DS} = 0 V, V _{GS} = -10 V f = 1 MHz
8 C _{sg(off)} Source Gate OFF Capacitance			5			5			5		
9 C _{dg(on)} Drain Gate Plus Source Gate ON Capacitance			28			28			28		
10 t _{d(on)} Turn On Delay Time		7			7				7		Switching Time Test Conditions J111 J112 J113 V _{DD} 10 V 10 V 10 V V _{GS(off)} -12 V -7 V -5 V R _L 800 Ω 1,600 Ω 3,200 Ω
11 t _r Rise Time		6			6				6		
12 t _{d(off)} Turn Off Delay Time		20			20				20		
13 t _f Fall Time		15			15				15		

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

NC

J111 J112 J113
J111-18 J112-18 J113-18

2

p-channel JFETs designed for . . .



Performance Curves PS
 See Section 4

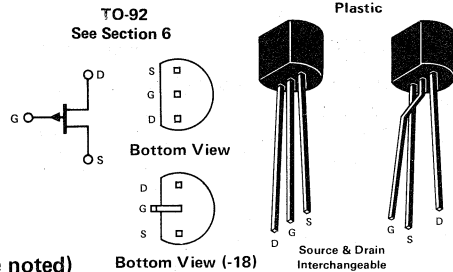
- Analog Switches
- Choppers
- Commutators

BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when Combined with J113, its N-Channel Complement
- Low Insertion Loss
 $r_{DS(on)} < 85 \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
 Purely Resistive
 High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
 $C_{sg(off)} < 5.5 \text{ pF}$
 $C_{dg(off)} < 5.5 \text{ pF}$
- Fast Switching
 $t_{d(on)} + t_r = 7 \text{ ns Typical}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristics	J174			J175			J176			J177			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 IGSS Gate Reverse Current (Note 2)			1			1			1			1	nA	$V_{DS} = 0, V_{GS} = 20 \text{ V}$
2 VGS(off) Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	$V_{DS} = -15 \text{ V}, I_D = -10 \text{ nA}$
3 BVGSS Gate-Source Breakdown Voltage	30			30					30			30		$V_{DS} = 0, I_G = 1 \mu\text{A}$
4 IDSS Saturation Drain Current (Note 3)	-20		-125	-7		-70	-2		-35	-1.5		-20	mA	$V_{DS} = -15 \text{ V}, V_{GS} = 0$
5 ID(off) Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	$V_{DS} = -15 \text{ V}, V_{GS} = 10 \text{ V}$
6 rDS(on) Drain-Source ON Resistance			85			125			250			300	Ω	$V_{GS} = 0, V_{DS} = -0.1 \text{ V}$
7 Cdg(off) Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	$V_{DS} = 0, V_{GS} = 10 \text{ V}$
8 Csg(off) Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5			
9 Cdg(on) + Csg(on) Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32			$V_{DS} = V_{GS} = 0$
10 td(on) Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions J174 J175 J176 J177 $V_{DD} -10 \text{ V} -6 \text{ V} -6 \text{ V} -6 \text{ V}$ $V_{GS(off)} 12 \text{ V} 8 \text{ V} 6 \text{ V} 3 \text{ V}$ $R_L 560 \Omega 1.2 \text{ K}\Omega 5.6 \text{ K}\Omega 10 \text{ K}\Omega$ $V_{GS(on)} 0 \text{ V} 0 \text{ V} 0 \text{ V} 0 \text{ V}$
11 tr Rise Time		5			10			20			25			
12 td(off) Turn Off Delay Time		5			10			15			20			
13 tf Fall Time		10			20			20			25			

NOTES:
 1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
 2. Approximately doubles for every 10°C increase in T_A . PS
 3. Pulse test duration = 300 μs ; duty cycle $\leq 3\%$.

n-channel JFETs designed for . . .



Performance Curves NP See Section 4

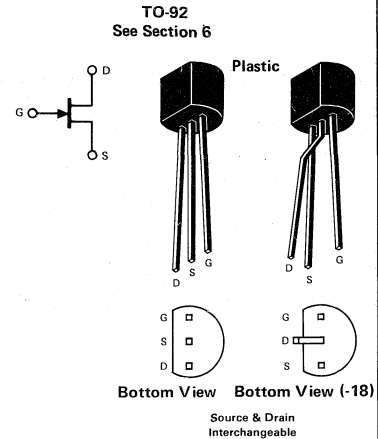
■ General Purpose Amplifiers

BENEFITS

- High Input Impedance
 $I_G = 35 \mu\text{A Typical}$
- Good for Low Power Supply Operation
 $V_{GS(off)} < 1.5 \text{ V (J201)}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-40 V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J201			J202			J203			J204			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 I_{GSS} Gate Reverse Current (Note 2)			-100			-100			-100			-100	pA	$V_{DS} = 0, V_{GS} = -20 \text{ V}$
2 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	-0.3		-2.0	V	$V_{DS} = 20 \text{ V}, I_D = 10 \text{ nA}$
3 BV_{GSS} Gate-Source Breakdown Voltage	-40			-40			-40			-25				$V_{DS} = 0, I_G = -1 \mu\text{A}$
4 I_{DSS} Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	0.2	1.2	3	mA	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
5 I_G Gate Current (Note 2)		-35			-35			-35			-35		pA	$V_{DG} = 20 \text{ V}, I_D = I_{DSS(min)}$
6 g_{fs} Common-Source Forward Transconductance (Note 3)	500			1,000			1,500			500	1500		μmho	$V_{DS} = 20 \text{ V}, V_{GS} = 0$
7 g_{os} Common-Source Output Conductance		1			3.5			10			2.5			
8 C_{iss} Common-Source Input Capacitance		4			4			4			4		pF	$f = 1 \text{ MHz}$
9 C_{rss} Common-Source Reverse Transfer Capacitance		1			1			1			1			
10 e_n Equivalent Short-Circuit Input Noise Voltage		5			5			5			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ kHz}$

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A .
3. Pulse test duration = 2 ms.

NP

J201 J202 J203 J204
J201-18 J202-18 J203-18 J204-18

2

n-channel JFETs designed for . . .



**Performance Curves NZF
See Section 4**

■ General Purpose Amplifiers

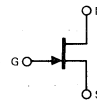
BENEFITS

- High Gain
 $g_{fs} = 7000 \mu\text{mho}$ Minimum
(J211, J212)
- High Input Impedance
 $I_{GSS} = 100 \text{ pA}$ Maximum
 $C_{iss} = 5 \text{ pF}$ Typical

TO-92
See Section 6

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C



Plastic



Bottom View

Source & Drain
Interchangeable

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J210			J211			J212			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 S I_{GSS} Gate Reverse Current (Note 1)			-100			-100			-100	pA	$V_{DS} = 0, V_{GS} = -15 \text{ V}$
2 T $V_{GS(off)}$ Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$
3 A BV_{GSS} Gate-Source Breakdown Voltage	-25			-25			-25				$V_{DS} = 0, I_G = -1 \mu\text{A}$
4 I I_{DSS} Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
5 C I_G Gate Current (Note 1)		-10			-10			-10		pA	$V_{DG} = 10 \text{ V}, I_D = 1 \text{ mA}$
6 g_{fs} Common-Source Forward Transconductance (Note 2)	4,000		12,000	6,000		12,000	7,000		12,000	μmho	$V_{DS} = 15 \text{ V}, V_{GS} = 0$
7 D g_{os} Common-Source Output Conductance			150			200			200		
8 N C_{iss} Common-Source Input Capacitance		4			4			4		pF	f = 1 MHz
9 A C_{rss} Common-Source Reverse Transfer Capacitance		1			1			1			
10 I \bar{e}_n Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{\text{Hz}}}$	f = 1 kHz

NOTES:

1. Approximately doubles for every 10°C increase in T_A .
2. Pulse test duration = 2 ms.

NZF

n-channel JFETs designed for . . .



**Performance Curves NP/NS
See Section 4**

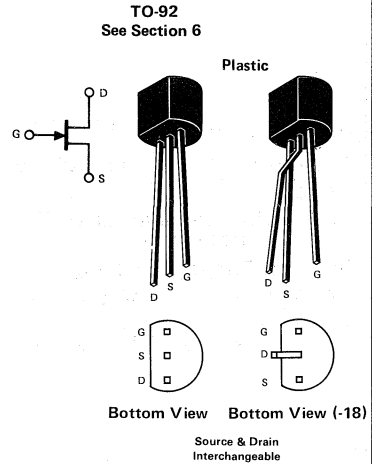
■ Audio and Sub-Audio Amplifiers

BENEFITS

- Ultra Low Noise
 $\bar{e}_n = 8 \text{ nV}/\sqrt{\text{Hz}}$ Typical at 10 Hz
 $\bar{e}_n = 2 \text{ nV}/\sqrt{\text{Hz}}$ Typical at 1 kHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) -40V
Gate Current 50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C) 360 mW
Operating Temperature Range -55 to 135°C
Storage Temperature Range -55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J230			J231			J232			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 IGSS Gate Reverse Current (Note 2)			-250			-250			-250	pA	V _{DS} = 0, V _{GS} = -30 V
2 VGS(off) Gate-Source Cutoff Voltage	-1		-3	-2		-5	-4		-6	V	V _{DS} = 20 V, I _D = 1 μA
3 BVGSS Gate-Source Breakdown Voltage	-40			-40			-40				V _{DS} = 0, I _G = -1 μA
4 IDSS Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	V _{DS} = 20 V, V _{GS} = 0
5 IG Gate Current (Note 2)		-10			-10			-10		pA	V _{DG} = 10 V, I _D = 0.5 mA
6 gfs Common-Source Forward Transconductance (Note 3)	1,000		2,500	1,500		3,000	2,500		4,000	μmho	V _{DS} = 20 V, V _{GS} = 0 f = 1 kHz
7 gos Common-Source Output Conductance		1.5			3			5			
8 Ciss Common-Source Input Capacitance		12			12			12		pF	f = 1 MHz
9 Crss Common-Source Reverse Transfer Capacitance		2			2			2			
10 \bar{e}_n Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	nV/√Hz	V _{DS} = 10 V, V _{GS} = 0 f = 10 Hz
11 \bar{e}_n Equivalent Short Circuit Input Noise Voltage		2			2			2			f = 1 kHz

NOTES:

1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

NP
NS

J230 J231 J232
J230-18 J231-18 J232-18

2

p-channel JFETs designed for . . .



Performance Curves PS
See Section 4

■ General Purpose Amplifiers

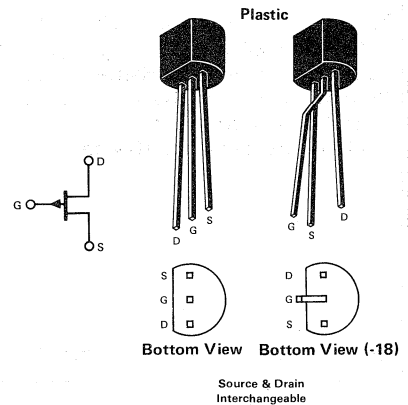
BENEFITS

- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers
 $g_{fs} = 14,000 \mu\text{mho}$ Typical (J271)
- Low Noise
 $\bar{e}_n = 6 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage (Note 1)	30 V
Gate Current	-50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	Characteristic	J270			J271			Unit	Test Conditions	
		Min	Typ	Max	Min	Typ	Max			
1	S I _{GSS} Gate Reverse Current (Note 2)			200			200	pA	V _{DS} = 0, V _{GS} = 20 V	
2	T V _{GS(off)} Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V _{DS} = -15 V, I _D = -1 nA	
3	A B _{VGS} Gate-Source Breakdown Voltage	30			30				V _{DS} = 0, I _G = 1 μA	
4	I I _{DSS} Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V _{DS} = -15 V, V _{GS} = 0	
5	C I _G Gate Current (Note 2)		15			60		pA	V _{DG} = -15 V, I _D = I _{DSS(min)}	
6	D Y N A M I C	g _{fs} Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V _{DS} = -15 V, V _{GS} = 0
7		g _{os} Common-Source Output Conductance			200			500		
8		C _{iss} Common-Source Input Capacitance		32			32		pF	f = 1 MHz
9		C _{rss} Common-Source Reverse Transfer Capacitance		4			4			
10	e _n Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	V _{DS} = -10 V, I _D = I _{DSS(min)} f = 1 kHz	

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

PS

n-channel JFETs designed for . . .



**J300
PREFERRED PART J210 SERIES**

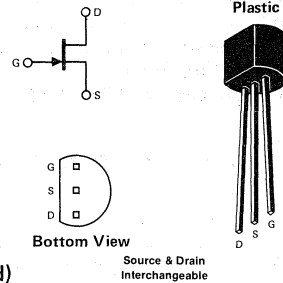
- VHF/UHF Amplifiers
- Oscillators
- Mixers

**Performance Curves NZF
See Section 4**

BENEFITS

- High Power Gain
20–23 dB Typical at 100 MHz,
Common-Source
17.5–20.5 dB Typical at 100 MHz,
Common-Gate
- Low Noise Figure
1.3 dB Typical at 100 MHz
- High Dynamic Range
Greater than 100 dB

TO-92
See Section 6



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C).	360 mW
Operating Temperature Range.	-55 to 135°C
Storage Temperature Range.	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

Characteristic		Min	Max	Unit	Test Conditions
1	I _{GSS} Gate Reverse Current		-0.5	nA	V _{GS} = -15 V, V _{DS} = 0 T _A = 125°C
			-0.1	μA	
3	BV _{GSS} Gate-Source Breakdown Voltage	-25		V	I _G = -1 μA, V _{DS} = 0
4	V _{GS(off)} Gate-Source Cutoff Voltage (Note 1)	-1.5	-7.0		
5	I _{DSS} Saturation Drain Current (Note 1, 2)	4	45		
6	g _{fs} Common-Source Forward Transconductance (Note 1)	4500	9000	μmho	V _{DS} = 10 V, I _D = 5 mA, f = 1 kHz
7	g _{os} Common-Source Output Conductance		200		
8	C _{rss} Common-Source Reverse Transfer Capacitance		1.7	pF	V _{DG} = 10 V, I _D = 5 mA, f = 1 MHz
9	C _{iss} Common-Source Input Capacitance		5.5		

Characteristic	J300A		J300B		J300C		J300D		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max	Min	Max		
I _{DSS} (Note 2) Saturation Drain Current	4	9	7	15	12	25	21	45	mA	V _{DS} = 10V V _{GS} = 0V
V _{GS(off)} Gate Source Cutoff Voltage	-1.5	-3.0	-2.0	-4.0	-2.5	-5.0	-3.5	-7.0	V	V _{DS} = 10V I _D = 1 nA

NOTES:

1. I_{DSS} and V_{GS(off)} are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NZF

2

n-channel JFETs designed for . . .



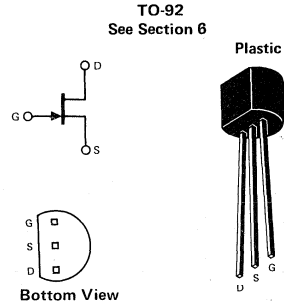
- VHF/UHF Amplifiers
- Oscillators
- Mixers

Performance Curves NH
See Section 4

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
NF = 1.7 dB Typical at 100 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)
 Gate-Drain or Gate-Source Voltage -30 V
 Gate Current 10 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J304			J305			Unit	Test Conditions	
	Min	Typ	Max	Min	Typ	Max			
1 S I_{GSS} Gate Reverse Current (Note 1)			-100			-100	pA	$V_{DS} = 0, V_{GS} = -20 V$	
2 T $V_{GS(off)}$ Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	$V_{DS} = 15 V, I_D = 1 nA$	
3 A BV_{GSS} Gate Source Breakdown Voltage	-30			-30				$V_{DS} = 0, I_G = -1 \mu A$	
4 T I_{DSS} Saturation Drain Current (Note 2)	5		15	1		8	mA	$V_{DS} = 15 V, V_{GS} = 0$	
5 D g_{fs} Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	$V_{DS} = 15 V, V_{GS} = 0$	
6 N g_{os} Common-Source Output Transconductance			50			50			$f = 1 kHz$
7 A C_{iss} Common-Source Input Capacitance		3.5			3.5				$f = 1 MHz$
8 M C_{rss} Common-Source Reverse Transfer Capacitance		0.85			0.85		pF		
9 I C_{oss} Common-Source Output Capacitance		1.0			1.0				
10 H g_{fs} Common-Source Forward Transconductance					3,000		μmho	$V_{DS} = 15 V, V_{GS} = 0$	
11 I g_{oss} Common-Source Output Conductance		4,200							$f = 100 MHz$
12 G b_{oss} Common-Source Output Susceptance		60			60				$f = 400 MHz$
13 R g_{iss} Common-Source Input Conductance		80							$f = 100 MHz$
14 E b_{iss} Common-Source Input Susceptance		800			800				$f = 400 MHz$
15 Q g_{ps} Common-Source Power Gain		3,600							$f = 100 MHz$
16 U g_{iss} Common-Source Input Conductance		80			80				$f = 400 MHz$
17 E b_{iss} Common-Source Input Susceptance		800							$f = 100 MHz$
18 N b_{iss} Common-Source Input Susceptance		2,000			2,000				$f = 400 MHz$
19 C C_{ps} Common-Source Power Gain		7,500							$f = 100 MHz$
20 I C_{ps} Common-Source Power Gain		20						$f = 400 MHz$	
21 N NF Noise Figure (Single Sideband)		11					dB	$V_{DS} = 15 V, I_D = 5 mA$	
22 F NF Noise Figure (Single Sideband)		1.7						$V_{DS} = 15 V, I_D = 5 mA,$	
23 I NF Noise Figure (Single Sideband)		3.8						$R_G = 1 K\Omega, f = 400 MHz$	

NOTES:
 1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration = 2 ms.

NH

n-channel JFETs designed for . . .



- VHF/UHF Amplifiers
- Oscillators
- Mixers

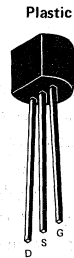
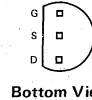
Performance Curves NZA
See Section 4
BENEFITS

- Industry Standard Part
In Low Cost Plastic Package
- High Power Gain
11 dB Typical at 450 MHz
Common-Gate
- Low Noise
2.7 dB Typical at 450 MHz
- Wide Dynamic Range
Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	J308			J309			J310			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 BV _{GSS} Gate-Source Breakdown Voltage	-25			-25			-25			V	I _G = -1 μA, V _{DS} = 0
2 I _{GSS} Gate Reverse Current			-1.0			-1.0			-1.0	nA	V _{GS} = -15 V, V _{DS} = 0
3 I _{GSS} Gate Reverse Current			-1.0			-1.0			-1.0	μA	T = +125°C
4 V _{GS(off)} Gate-Source Cutoff Voltage	-1.0		-6.5	-1.0		-4.0	-2.0		-6.5	V	V _{DS} = 10 V, I _D = 1 nA
5 I _{DSS} Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V _{DS} = 10 V, V _{GS} = 0
6 V _{GS(f)} Gate-Source Forward Voltage			1.0			1.0			1.0	V	V _{DS} = 0, I _G = 1 mA
7 g _{fs} Common-Source Forward Transconductance	8,000	17,000		10,000	17,000		8,000	17,000		μmhos	V _{DS} = 10 V, I _D = 10 mA f = 1 kHz
8 g _{os} Common-Source Output Conductance			250			250			250		
9 g _{fg} Common-Gate Forward Transconductance		13,000			13,000			12,000			
10 g _{og} Common-Gate Output Conductance		150			100			150		pF	V _{DS} = 0, V _{GS} = -10 V f = 1 MHz
11 C _{gd} Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5		
12 C _{gs} Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0		
13 e _n Equivalent Short-Circuit Input Noise Voltage		10			10			10		nV/√Hz	V _{DS} = 10 V, I _D = 10 mA f = 100 Hz
14 Re(y _{fs}) Common-Source Forward Transconductance		12			12			12		mmho	V _{DS} = 10 V, I _D = 10 mA f = 105 MHz
15 Re(y _{ig}) Common-Gate Input Conductance		14			14			14			
16 Re(y _{is}) Common-Source Input Conductance		0.4			0.4			0.4			
17 Re(y _{os}) Common-Source Output Conductance		0.15			0.15			0.15		dB	f = 450 MHz
18 G _{pg} Common-Gate Power Gain at Noise Match		16			16			16			
19 NF Noise Figure		1.5			1.5			1.5			
20 G _{pg} Common-Gate Power Gain at Noise Match		11			11			11			
21 NF Noise Figure		2.7			2.7			2.7			

NOTE:
1. Pulse test PW 300 μs, duty cycle ≤ 3%.

NZA

J308 J309 J310

2

n-channel JFETs current regulator diodes designed for . . .



- **Current Regulation**
- **Current Limiting**
- **Biassing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL
See Section 4

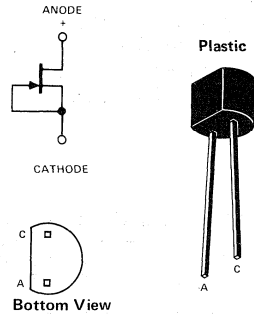
BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
No Power Supplies Required
- Good Operating Current Tolerance
±20%

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

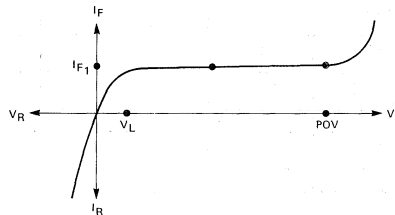
Characteristic		J500	J501	J502	J503	J504	J505	Unit	Test Conditions	
1 S T A T I C	F _I Forward Current (Note 1)	Min	0.192	0.264	0.344	0.448	0.600	0.800	mA	V _F = 25 V
		Nominal	0.240	0.330	0.430	0.560	0.750	1.000		
		Max	0.288	0.396	0.516	0.672	0.900	1.200		
4 P O V	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	F _I = 1.1 F _I (Max)
		Max	1.2	1.3	1.5	1.7	1.9	2.1		
		T _{yp}	0.8	0.9	1.1	1.2	1.4	1.5		
5 V L	Limiting Voltage (Note 3)	Max	1.2	1.3	1.5	1.7	1.9	2.1	V	F _I = 0.9 F _I (Min)
		T _{yp}	0.8	0.9	1.1	1.2	1.4	1.5		
7 D Y N	Z _{F_I} Small-Signal Dynamic Impedance (Note 1)	Min	5.0	3.0	2.0	1.4	1.0	0.6	MΩ	V _F = 25 V, f = 1 kHz
		T _{yp}	8.0	6.0	4.4	3.4	2.5	1.9		
9	C _F Anode-Cathode Capacitance	T _{yp}	2	2	2	2	2	2	pF	V _F = 25 V, f = 1 MHz

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where |F_I < 1.1 |F_I(Max) is guaranteed.
3. Minimum V_F required to insure |F_I > 0.9 |F_I(Min).

NCL

**Current-Limiter Diode
V-I Characteristic**



n-channel JFETs current regulator diodes designed for . . .



J506 J507 J508 J509 J510 J511

- Current Regulation
- Current Limiting
- Biasing
- Linear Ramp and Staircase Generator

Performance Curves NCL
See Section 4

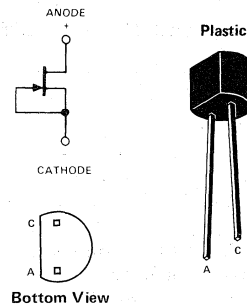
BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
No Power Supplies Required
- Good Operating Current Tolerance
±20%

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	
	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

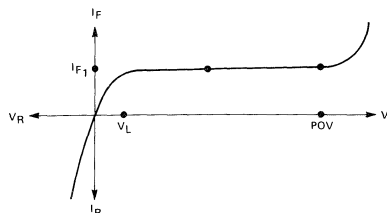
Characteristic		J506	J507	J508	J509	J510	J511	Unit	Test Conditions
1 S T A T I C	I _{F1} Forward Current (Note 1)	Min	1.120	1.440	1.9	2.4	2.9	3.8	mA V _F = 25 V
		Nominal	1.400	1.800	2.4	3.0	3.6	4.7	
		Max	1.680	2.160	2.9	3.6	4.3	5.6	
4 D Y N	POV Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V I _F = 1.1 I _{F1} (Max) I _F = 0.9 I _{F1} (Min)
		Max	2.5	2.8	3.1	3.5	3.9	4.2	
6	V _L Limiting Voltage (Note 3)	Typ	1.8	2.0	2.2	2.5	2.8	3.0	MΩ V _F = 25 V, f = 1 kHz
		Typ	1.4	1.0	0.70	0.60	0.50	0.30	
7 D Y N	Z _{F1} Small-Signal Dynamic Impedance (Note 1)	Min	0.4	0.25	0.25	0.20	0.20	0.15	pF V _F = 25 V, f = 1 MHz
		Typ	2	2	2	2	2	2	
9	C _F Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where I_F < 1.1 I_{F1}(Max) is guaranteed.
3. Minimum V_F required to insure I_F > 0.9 I_{F1}(Min).

NCL

Current-Limiter Diode
V-I Characteristic



n-channel JFETs current regulator diodes designed for . . .



Performance Curves NKL
See Section 4

BENEFITS

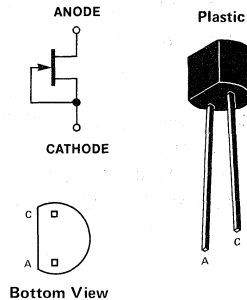
- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
No Power Supplies Required

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation (25°C Free Air Temperature)	350 mW
Power Derating (to +125°C)	3.27 mW/°C
Storage Temperature Range	-55 to 135°C
Operating Temperature Range	-55 to 135°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typical	Max	Unit	Test Conditions
1 2 3	S T A	I _{F1} Forward Current (Note 1)			770	μA	V _F = 100 V
			250		700		V _F = 25 V
			200		—		V _F = 1.0 V
4 5 6	T I C	POV Peak Operating Voltage (Notes 1 and 2)	100			V	I _F = 1.1 I _{F1} (Max)
		V _L Limiting Voltage (Note 3)		1.1	1.5		I _F = 0.9 I _{F1} (Min)
7 8	D Y N	Z _{F1} Small-Signal Dynamic Impedance (Note 1)	2.0	4.4		MΩ	V _F = 25 V, f = 1 kHz
		C _F Anode-Cathode Capacitance		2			pF

NOTES:

1. Pulse test duration = 2 ms.
2. Maximum V_F where I_F < 1.1 I_{F1}(Max) is guaranteed.
3. Minimum V_F required to insure I_F > 0.9 I_{F1}(Min).

NKL

current regulator diodes designed for . . .



- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Performance Curves NCL
See Section 4

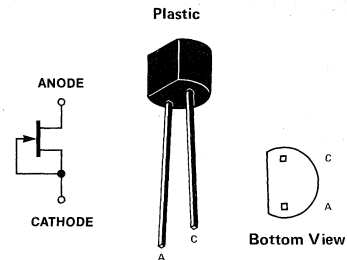
BENEFITS

- Simple Two Lead Current Source
- In Low Cost Plastic Package
- Simplifies Floating Current Sources
No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage.	50 V
Forward Current.	20 mA
Reverse Current.	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C).	360 mW
Operating Temperature Range.	-55 to 135°C
Storage Temperature Range.	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PART NUMBER	Regulator Current			Limiting Voltage		Peak op Volt	Dynamic Impedance	Knee Impedance
	I_F NOM	I_F MIN	I_F MAX	V_L	V_L	V_{OP}	'ZD	'ZK
	$V_F=25V$			$I_F=0.8 I_{F1(min)} I_{F1} 1.1$				
	Nominal mA	Min mA	Max mA	Max Volts	Typical	I_{F1} (Max) Min Volts	Typical Megohms	Typical Megohms
J553	0.5	0.18	0.75	1.3	0.75	50	10	2
J554	1.0	0.6	1.6	1.75	0.55	50	1	1
J555	2.0	1.4	2.6	2.15	0.75	50	.88	0.25
J556	3.0	2.4	3.8	2.6	0.75	50	.6	0.14
J557	4.5	3.6	5.3	3.0	1.5	50	.48	0.09

NOTES:

1. Pulse test—steady state currents may vary.
2. Pulse test—steady state impedance may vary.
3. Min V_F required to insure $I_F > 0.8 I_{F1}$ (min).
4. Max V_F where $I_F < 1.1 I_{F1}$ (max) is guaranteed.

NCL

J553 J554 J555 J556 J557

2

JPAD5 JPAD10 JPAD20 JPAD50
 JPAD5 JPAD10 JPAD20 JPAD50
 JPAD100 JPAD200 JPAD500



low-leakage pico-amp diodes designed for . . .

- High Impedance Diode Switching
- High Dynamic Range Log Amps
- High Isolation Protection Circuits

BENEFITS
 • Low Cost

TO-92
 See Section 6

ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current 10 mA
 Total Device Dissipation 360 mW
 Storage Temperature Range. -65°C to +135°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C



Bottom View

ELECTRICAL CHARACTERISTICS (25°C)

Characteristic		Min	Typ	Max	Unit	Test Conditions
1	S T A T I C I_R Reverse Current (Note 1)	JPAD5		-5	pA	$V_R = -20$ V
		JPAD10		-10		
		JPAD20		-20		
		JPAD50		-50		
		JPAD100		-100		
		JPAD200		-200		
		JPAD500		-500		
2	BV_R Breakdown Voltage (Reverse)	-35	-80		V	$I_R = -1$ μ A
3	V_F Forward Voltage Drop		0.8	1.5	V	$I_F = 5$ mA
4	D Y N C_R Capacitance		1.5	2.0	pF	$V_R = -5$ V, $f = 1$ MHz

NOTE:

1. The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.



JR135V JR170V JR200V JR220V JR240V

2

high voltage protection diode designed for. . .

- High Impedance Diode Switching
- High Dynamic Range Log Amps
- High Isolation Protection Circuits

Performance Curves VRMA
See Section 4

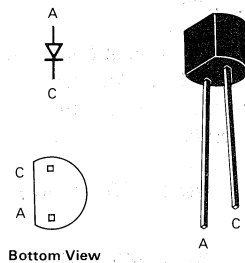
BENEFITS

- Offers High Voltage Protection
- Broad Current Range

ABSOLUTE MAXIMUM RATINGS (25°C)

Anode to Cathode Voltage	
JR135V	135V
JR170V	170V
JR200V	200V
JR220V	220V
JR240V	240V
Forward Diode Current I_F	20mA
Reverse Diode Current I_R	50mA
Power Dissipation P_D	360mW
(Derate 3.27mW/°C)	
Storage Temperature T_{STG}	-55°C to 150°C
Operating Temperature T_{OP}	-55°C to 135°C

Plastic TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C)

Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	POV	Peak Operating Voltage ¹	JR135V	135		V	$I_F = 1mA$
			JR170V	170			
			JR200V	200			
			JR220V	220			
			JR240V	240			
2	I_F^1 I_F^2	Forward Current		200		μA	$V_F = 2V$
				200	770		$V_F = 100V$
3	V_L	Limiting Current			0.9	V	$I = 0.8 I_F^1$
4	Z_D	Dynamic Impedance		2		MΩ	$V_F = 25V$
5	$\Delta I_F / \Delta T$	I_F Temp Coefficient		+0.6		%/°C	$V_F = 2-100V$
							$T_A = -20 \text{ to } +85^\circ C$

NOTE:

1. Pulse test duration 2 ms.

VRMA

enhancement-type p-channel MOSFET designed for . . .



Performance Curves MRA
See Section 4

■ **High-Input
Impedance Amplifiers**

**Smoke Detectors
Electrometers
pH Meters**

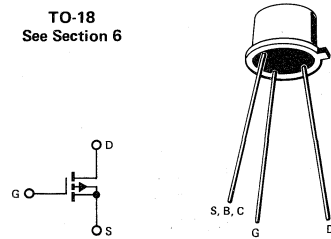
BENEFITS

- High Input Impedance
 $I_{GSS} = 30$ Femto Amp Typical
- High Gain
 $g_{fs} = 1000 \mu\text{mho}$ Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage25 V
Gate-Source Voltage ± 10 V
Drain Current30 mA
Total Device Dissipation at (Or Below) $T_A = 25^\circ\text{C}$ (Derate 3 mW/°C to +150°C)375 mW
Operating Junction Temperature -55 to $+150^\circ\text{C}$
Storage Temperature -65 to $+200^\circ\text{C}$
Lead Temperature (1/16" from case for 10 seconds) 265°C

TO-18
See Section 6



ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic	Min	Max	Unit	Test Conditions
1	S T A T I C	I_{GSS} Gate-Source Leakage Current		-1.0	pA	$V_{GS} = -10$ V, $V_{DS} = 0$
2		BV_{DSS} Drain-Source Breakdown Voltage	-25		V	$I_D = -10 \mu\text{A}$, $V_{GS} = 0$
3		V_{GS} Gate-Source Voltage	-2.0	-6.0	V	$V_{DS} = -10$ V, $i_D = -10 \mu\text{A}$
4		I_{DSS} Drain Cutoff Current		-20	nA	$V_{DS} = -10$ V, $V_{GS} = 0$
5		$I_{D(on)}$ ON Drain Current	-3.0		mA	$V_{DS} = -10$ V, $V_{GS} = -10$ V
6	D Y N A M I C	g_{fs} Common-Source Forward Transconductance	1000		μmhos	$V_{DS} = -10$ V, $I_D = -2$ mA, $f = 1$ kHz
7		C_{iss} Common-Source Input Capacitance		6.0	pF	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $f = 1$ MHz
8		C_{rss} Common-Source Reverse Transfer Capacitance		1.5		

MRA

n-channel JFET designed for . . .



Performance Curves NH
See Section 4

- VHF/UHF Amplifiers
- Mixers
- Oscillators

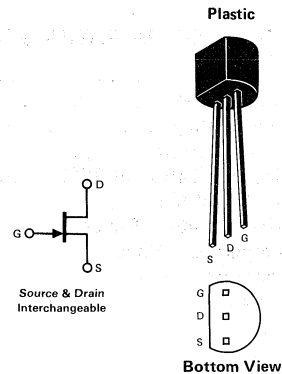
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions	
1	I _{GSS} Gate Reverse Current		-2.0	nA	V _{GS} = -15 V, V _{DS} = 0	T _A = +100°C
			-2.0	μA		
3	BV _{GSS} Gate-Source Breakdown Voltage	-25		V	I _G = -10 μA, V _{DS} = 0	
4	V _{GS(off)} Gate-Source Cutoff Voltage		-8.0		V _{DS} = 15 V, I _D = 2 nA	
5	I _{DSS} Saturation Drain Current	2.0	20	mA	V _{DS} = 15 V, V _{GS} = 0 (Note 1)	
6	V _{GS} Gate-Source Voltage	-0.5	-7.5	V	V _{DS} = 15 V, I _D = 200 μA	
7	g _{fs} Common-Source Forward Transconductance	2000	7500	μmhos	V _{DS} = 15 V, V _{GS} = 0	f = 1 kHz
	Re(y _{fs}) Common-Source Forward Transconductance	1600				f = 100 MHz
	Re(y _{os}) Common-Source Output Conductance		200			
	Re(y _{is}) Common-Source Input Conductance		800			
11	C _{iss} Common-Source Input Capacitance		7.0	pF		f = 1 MHz
12	C _{rss} Common-Source Reverse Transfer Capacitance		3.0			

NOTE:

1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

2

n-channel JFET designed for . . .



- VHF/UHF Amplifiers
- Mixers
- Oscillators

Performance Curves NH
See Section 4

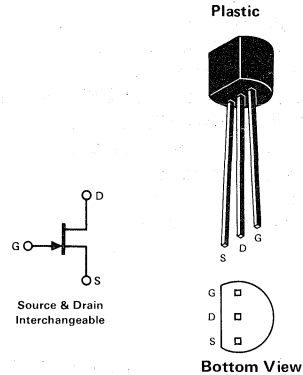
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions		
1 2 3 4 5 6 7 8 9 10 11 12	S T A T I C	I_{GSS} Gate Reverse Current		-1.0	nA	$V_{GS} = -15 V, V_{DS} = 0$	$T_A = +100^\circ C$
				-1.0	μA		
		BV_{GSS} Gate-Source Breakdown Voltage	-25		V	$I_G = -10 \mu A, V_{DS} = 0$	
	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5	-8.0		$V_{DS} = 15 V, I_D = 10 \mu A$		
	I_{DSS} Saturation Drain Current	1.5	24	mA	$V_{DS} = 15 V, V_{GS} = 0$ (Note 1)		
	g_{fs} Common-Source Forward Transconductance	2000	7500	$\mu mhos$	$V_{DS} = 15 V, V_{GS} = 0$	f = 1 kHz	
	g_{os} Common-Source Output Conductance		75				
	$Re(y_{fs})$ Common-Source Forward Transconductance	1600					
	$Re(y_{os})$ Common-Source Output Conductance		200				
	$Re(y_{is})$ Common-Source Input Conductance		800			f = 100 MHz	
	C_{iss} Common-Source Input Capacitance		6.5	pF		f = 1 MHz	
	C_{rss} Common-Source Reverse Transfer Capacitance		2.5				
	NF Noise Figure		2.5	dB	$V_{DS} = 15 V, V_{GS} = 0, R_G = 1M \Omega$	f = 1 kHz	
			3.0		$V_{DS} = 15 V, V_{GS} = 0, R_G = 1K \Omega$	f = 100 MHz	

NOTE:

1. Pulse test, pulse width = 300 μs , duty cycle \leq 3%.

NH



n-channel JFET designed for . . .

- General Purpose Amplifiers
- Analog Switches

Performance Curves NRL, NP
See Section 4

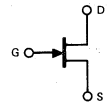
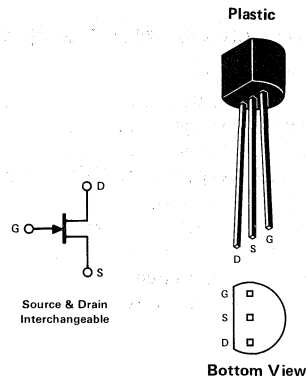
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



Source & Drain Interchangeable

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typ	Max	Unit	Test Conditions
S T A T I C	1	I _{GSS} Gate Reverse Current		-0.01	-1.0	nA	V _{GS} = -15 V, V _{DS} = 0
	2	BV _{GSS} Gate-Source Breakdown Voltage	-25	-60		V	I _G = -10 μA, V _{DS} = 0
	3	V _{GS(off)} Gate-Source Cutoff Voltage	-0.2		-8.0		V _{DS} = 15 V, I _D = 10 μA
	4	I _{DSS} Saturation Drain Current	0.5		24	mA	V _{DS} = 15 V, V _{GS} = 0 (Note 1)
D Y N A M I C	5	g _{fs} Common-Source Forward Transconductance	800		6000	μmho	V _{DS} = 15 V, V _{GS} = 0
	6	g _{os} Common-Source Output Conductance		10	75		
	7	C _{iSS} Common-Source Input Capacitance		4.5	7.0	pF	f = 1 MHz
	8	C _{rSS} Common-Source Reverse Transfer Capacitance		1.0	3.0		
	9	NF Noise Figure		0.04	2.5	dB	V _{DS} = 15 V, V _{GS} = 0, R _G = 1M Ω, f = 1 kHz

NOTE:

1. Pulse test PW ≤ 630 ms, duty cycle ≤ 10%.

NRL, NP

n-channel JFET designed for . . .



Performance Curves NRL, NP
See Section 4

- General Purpose Amplifiers
- Analog Switches

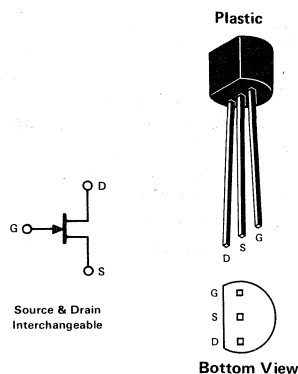
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	20V
Source-Gate Voltage	20V
Drain-Source Voltage	20V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit	Test Conditions	
S T A T I C	I_{GSS} Gate-Reverse Current		-0.1	-100	nA	$V_{GS} = -10\text{ V}, V_{DS} = 0$	
	BV_{GSS} Gate-Source Breakdown Voltage	-20			V	$I_G = -10\ \mu\text{A}, V_{DS} = 0$	
	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.5		-10.0		$V_{DS} = 10\text{ V}, I_D = 1\ \mu\text{A}$	
	I_{DSS} Saturation Drain Current	0.5		20	mA	$V_{DS} = 10\text{ V}, V_{GS} = 0$ (Note 1)	
D Y N A M I C	g_{fs} Common-Source Forward Transconductance	500			μmho	$V_{DS} = 10\text{ V}, V_{GS} = 0$	$f = 1\text{ kHz}$
	g_{os} Common-Source Output Conductance		10				
	C_{iss} Common-Source Input Capacitance		4.5		pF		$f = 1\text{ MHz}$
	C_{rss} Common-Source Reverse Transfer Capacitance		1.0				

NRL, NP

NOTE:

1. Pulse test $PW \leq 630\text{ msec}$, duty cycle $\leq 10\%$.

n-channel JFET designed for . . .



Performance Curves NH
See Section 4

- VHF/UHF Amplifiers
- Mixers
- Oscillators

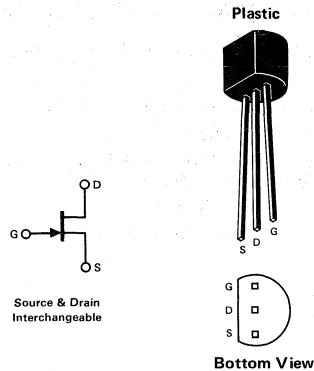
BENEFITS

- Low Cost
- Automatic Insertion Package

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Typ	Max	Unit	Test Conditions
S T A T I C	1	I _{GSS} Gate Reverse Current		-0.01	-100	nA	V _{GS} = -10 V, V _{DS} = 0
	2	BV _{GS} Gate-Source Breakdown Voltage	-25			V	I _G = -10 μA, V _{DS} = 0
	3	V _{GS(off)} Gate-Source Cutoff Voltage	-0.5		-10.0		V _{DS} = 10 V, I _D = 1 μA
	4	I _{DSS} Saturation Drain Current	1		25	mA	V _{DS} = 10 V, V _{GS} = 0, (Note 1)
D Y N	5	g _{fs} Common-Source Forward Transconductance	1000		7500	μmho	f = 1 kHz
	6	Re _(Y_{fs}) Common-Source Forward Transconductance	800				f = 100 MHz
	7	C _{iss} Common-Source Input Capacitance		3.5		pF	V _{DS} = 10 V, V _{GS} = 0
8	C _{rss} Common-Source Reverse Transfer Capacitance		0.85		f = 1 MHz		

NOTE:

1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

NH

p-channel JFETs designed for . . .



**Performance Curves PS
 See Section 4**

- **Analog Switches**
- **Choppers**
- **Commutators**

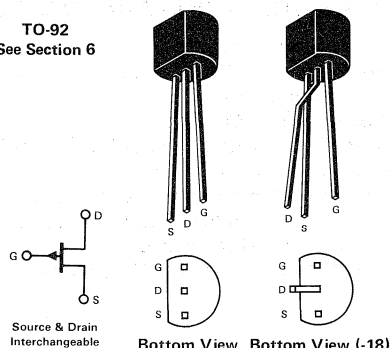
BENEFITS

- **Low Insertion Loss**
 $r_{DS(on)} = 75 \Omega$ Maximum (P1086)
- **No Offset or Error Voltages Generated by Closed Switch**
 Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C

TO-92
 See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	P1086		P1087		Unit	Test Conditions
	Min	Max	Min	Max		
1 BV _{GSS} Gate-Source Breakdown Voltage	30		30		V	I _G = 1 μA, V _{DS} = 0
2 IGSS Gate Reverse Current		2		2	nA	V _{GS} = 15 V, V _{DS} = 0
3 ID(off) Drain Cutoff Current		-10		-10	μA	V _{DS} = -15 V, V _{GS} = 12 V (P1086) V _{GS} = 7 V (P1087)
4 IDGO Drain Reverse Current		-0.5		-0.5	μA	V _{DG} = -15 V, I _S = 0 T _A = 85°C
5 IDGO Drain Reverse Current		2		2	nA	
6 VGS(off) Gate-Source Cutoff Voltage		0.1		0.1	μA	T _A = 85°C
7 VGS(off) Gate-Source Cutoff Voltage		10		5	V	V _{DS} = -15 V, I _D = -1 μA
8 IDSS Saturation Drain Current	-10		-5		mA	V _{DS} = -20 V, V _{GS} = 0
9 VDS(on) Drain-Source ON Voltage		-0.5		-0.5	V	V _{GS} = 0, I _D = -6 mA (P1086), I _D = -3 mA (P1087)
9 rDS(on) Static Drain-Source ON Resistance		75		150	Ω	I _D = -1 mA, V _{GS} = 0
10 rds(on) Drain-Source ON Resistance		75		150	Ω	I _D = 0, V _{GS} = 0 f = 1 kHz
11 Ciss Common-Source Input Capacitance		45		45	pF	V _{DS} = -15 V, V _{GS} = 0 f = 1 MHz
12 Crss Common-Source Reverse Transfer Capacitance		10		10	pF	V _{DS} = 0, V _{GS} = 12 V (P1086) V _{GS} = 7 V (P1087)
13 td(on) Turn-ON Delay Time		15		15	ns	V _{DD} = -6 V, V _{GS(on)}} = 0
14 tr Rise Time		20		75	ns	V _{GS(off)}} I _{D(on)} R _L
15 td(off) Turn-OFF Delay Time		15		75	ns	P1086 12 V -6 mA 910 Ω
16 tf Fall Time		50		100	ns	P1087 7 V -3 mA 1.8K Ω

NOTE:
 1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PS



low-leakage pico-amp diodes designed for . . .

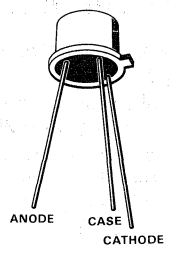
- Clipping Circuits
- Diode Switching
- High Impedance Protection Circuits

- BENEFITS**
- Very High Off-Isolation
1 pA Max (PAD1)

ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current	50 mA
Total Device Dissipation	300 mW
Storage Temperature Range	-55°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

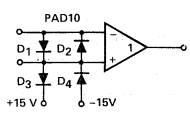
TO-18
See Section 6



(Case lead for
PAD1, 2, & 5 only)

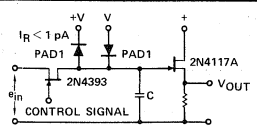
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Typ	Max	Unit	Test Conditions
S T A T I C	I _R Reverse Current			-1	pA	V _R = -20 V
				-2		
				-5		
				-10		
				-20		
				-50		
				-100		
B V R	Breakdown Voltage (Reverse)	-45		-120	V	I _R = -1 μA
		-35				
V F	Forward Voltage Drop		0.8	1.5		I _F = 5 mA
D Y N	C _R Capacitance			0.8	pF	V _R = -5 V, f = 1 MHz
				2		



APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D₁ and D₂. Common mode input voltage limited by PADS D₃ and D₄ to ±15 V.



Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

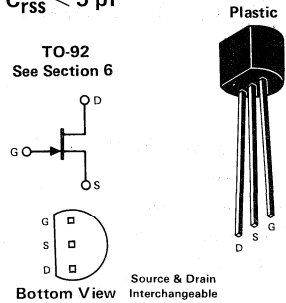
Performance Curves NC See Section 4

BENEFITS

- Low Insertion Loss
High Accuracy in Test Systems
 $r_{DS(on)} < 30 \Omega$ (PN4091)
- High Off-Isolation
 $I_{D(off)} < 200 \text{ pA}$
- High Speed
 $t_{rise} < 10 \text{ ns}$ (PN4091)
- Short Sample and Hold Aperture Time
 $C_{rss} < 5 \text{ pF}$

ABSOLUTE MAXIMUM RATINGS (25°C)

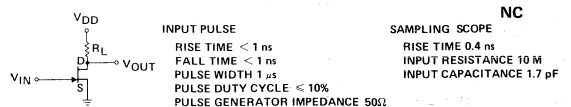
Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C).	360 mW
Operating Temperature Range.	-55 to 135°C
Storage Temperature Range.	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	PN4091		PN4092		PN4093		Unit	Test Conditions			
	Min	Max	Min	Max	Min	Max					
1 BV _{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	I _G = -1 μA, V _{DS} = 0			
2 I _{DGO} Drain Reverse Current		200		200		200	pA	V _{GS} = -20 V, I _S = 0			
3		400		400		400	nA	150°C			
4	I _{D(off)} Drain Cutoff Current					200	pA	V _{DS} = 20 V	V _{GS} = -6 V	150°C	
5						400	nA		V _{GS} = -8 V		
6							200		pA	V _{GS} = -12 V	150°C
7							400		nA		
8			200						pA		
9			400						nA		
10 V _{GS(off)} Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	V _{DS} = 20 V, I _D = 1 nA			
11 I _{DSS} Saturation Drain Current (Note 1)	30		15		8		mA	V _{DS} = 20 V, V _{GS} = 0			
12	V _{DS(on)} Drain-Source ON Voltage					0.2	V	V _{GS} = 0	I _D = 2.5 mA		
13									I _D = 4 mA		
14			0.2						I _D = 6.6 mA		
15 r _{DS(on)} Static Drain-Source ON Resistance		30		50		80	Ω	V _{GS} = 0, I _D = 1 mA			
16 r _{ds(on)} Drain-Source ON Resistance		30		50		80	Ω	V _{GS} = 0, I _D = 0			
17 C _{iss} Common-Source Input Capacitance		16		16		16	pF	V _{DS} = 20 V, V _{GS} = 0			
18 C _{rss} Common-Source Reverse Transfer Capacitance		5		5		5		V _{DS} = 0, V _{GS} = -20 V			
19 t _{d(on)} Turn-ON Delay Time		15		15		20	ns	V _{DD} = 3 V, V _{GS(on)} = 0			
20 t _r Rise Time		10		20		40		I _{D(on)} V _{GS(off)} R _L			
21 t _{off} Turn-OFF Time		40		60		80		PN4091 6.6 mA -12 V 425 Ω			
								PN4092 4 -8 700			
								PN4093 2.5 -6 1120			

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



PN4117 PN4117A PN4118 PN4118A
 PN4119 PN4119A PN4120 PN4120A

n-channel JFETs designed for . . .



Performance Curves NT
 See Section 4

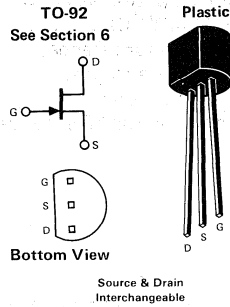
- Ultra-High Input Impedance Amplifiers
- Electrometers
- pH Meters
- Smoke Detectors

BENEFITS

- Low Power
 $I_{DSS} < 90 \mu A$ (PN4117)
- Minimum Circuit Loading
 $I_{GSS} < 1 \text{ pA}$ (PN4117A Series)

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage -40 V
 Gate Current 10 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	PN4117 PN4117A		PN4118 PN4118A		PN4119 PN4119A		PN4120 PN4120A		Unit	Test Conditions			
	Min	Max	Min	Max	Min	Max	Min	Max					
S T A T I C	IGSS	Gate Reverse Current PN4117 Series Only		-10	-10	-10	-10	-20	pA	VGS = -20 V, VDS = 0	100°C		
		Gate Reverse Current (Typical) PN4117A Series Only		-1*	-1*	-1*	-5*	pA					
	IGSS	Gate Reverse Current (Typical) PN4117A Series Only		-2.5	-2.5	-2.5	-10	nA	VGS = -20 V, VDS = 0	100°C			
D Y N A M I C	BVGS	Gate-Source Breakdown Voltage		-40	-40	-40	-40	-40	V	IG = -1 μA, VDS = 0			
	VGS(off)	Gate-Source Cutoff Voltage		-0.6	-1.8	-1	-3	-2	-6	3	VDS = 10 V, ID = 1 nA		
	IDSS	Saturation Drain Current (Note 2)		0.03	0.09	0.08	0.24	0.20	0.60	0.03	0.3	VDS = 10 V, VGS = 0	
	gfs	Common-Source Forward Transconductance (Note 2)		70	210	80	250	100	330	70	300	VDS = 10 V, VGS = 0	f = 1 kHz
gos	Common-Source Output Conductance			3		5		10		20	f = 1 MHz		
Ciss	Common-Source Input Capacitance			3		3		3		3			
Crss	Common-Source Reverse Transfer Capacitance			1.5		1.5		1.5		1.5			

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied.

NT

2

n-channel JFETs designed for . . .



Performance Curves NP, NH
 See Section 4

■ General Purpose Amplifiers

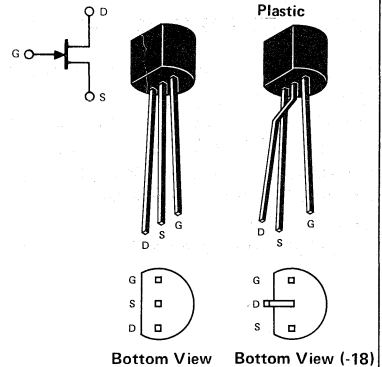
BENEFITS

- Low Cost
- High Input Impedance
 $I_G = 35 \text{ pA}$ Typically
- Low Noise
 $\bar{e}_n = 5 \text{ nV}/\sqrt{\text{Hz}}$ Typically @ 1 kHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-30V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	-55 to 135°C
Storage Temperature Range	-55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
 See Section 6



Bottom View Bottom View (-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Source & Drain
 Interchangeable

Characteristic	PN4302		PN4303		PN4304		Unit	Test Conditions				
	Min	Max	Min	Max	Min	Max						
S T A T I C	1	I_{GSS}	Gate Reverse Current (Note 2)		1		nA	$V_{GS} = -10 \text{ V},$ $V_{DS} = 0$ $T_A = 85^\circ \text{C}$				
			0.1		-0.1		μA					
	3	BV_{GSS}	Gate-Source Breakdown Voltage		-30		V					
	4	$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4.0		-6.0		$I_G = -1 \mu\text{A}, V_{DS} = 0$			
	5	I_{DSS}	Saturation Drain Current (Note 3)		0.5		5.0		4.0	10	0.5	15
D Y N A M I C	6	g_{fs}	Common-Source Forward Transconductance (Note 3)		1000		2000	1000	μmho	$V_{DS} = 20 \text{ V},$ $V_{GS} = 0$	f = 1 kHz	
	7	g_{os}	Common-Source Output Conductance		50		50	50				
	8	C_{rss}	Common-Source Reverse Transfer Capacitance		3		3	3	pF	f = 1 MHz		
	9	C_{iss}	Common-Source Input Capacitance		6		6	6		$V_{DG} = 10 \text{ V},$ $I_S = 0$	f = 140 kHz	
	10	C_{DG}	Drain-Gate Capacitance		2		2	2		$V_{DS} = 10 \text{ V},$ $V_{GS} = 0$	f = 1 kHz, $R_{gen} = 1.0 \text{M } \Omega$	
	11	NF	Noise Figure		2.0		2.0	3.0	dB	$V_{DS} = 20 \text{ V},$ $V_{GS} = 0$	f = 10 MHz	
	12	$ y_{fs} $	Common-Source Short Circuit Forward Transadmittance (Note 3)		700		1400	700	μmho	$V_{DS} = 20 \text{ V},$ $V_{GS} = 0$		

NP, NH

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A .
3. Pulse test duration = 2 ms.

PN4391 PN4392 PN4393
 PN4391-18 PN4392-18 PN4393-18



n-channel JFETs designed for ...

- Analog Switches
- Commutators
- Choppers

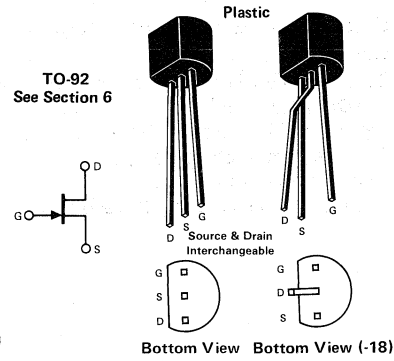
Performance Curves NC
 See Section 4

BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
 Purely Resistive
 High Isolation Resistance from Driver
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage -40 V
 Forward Gate Current 50 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	PN4391		PN4392		PN4393		Unit	Test Conditions		
	Min	Max	Min	Max	Min	Max				
1 IGSS Gate Reverse Current		-1.0		-1.0		-1.0	nA	VGS = -20 V, VDS = 0	100°C	
3 BVGSS Gate-Source Breakdown Voltage	-40		-40		-40		V	IG = -1 μA, VDS = 0		
5 ID(off) Drain Cutoff Current						1.0	nA	VDS = 20 V	VGS = -5 V	100°C
						1.0			VGS = -7 V	100°C
		1.0							VGS = -12 V	100°C
		200								
10 VGS(off) Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	VDS = 20 V, ID = 1 mA		
11 IDSS Saturation Drain Current (Note 1)	50	150	25	100	5	60	mA	VDS = 20 V, VGS = 0		
13 VDS(on) Drain-Source ON Voltage				0.4			V	VGS = 0	ID = 3 mA	
									ID = 6 mA	
		0.4							ID = 12 mA	
15 rDS(on) Static Drain-Source ON Resistance		30		60		100	Ω	VGS = 0, ID = 1 mA		
16 rds(on) Drain-Source ON Resistance		30		60		100	Ω	VGS = 0, VDS = 0	f = 1 kHz	
17 Ciss Common-Source Input Capacitance		14		14		14	pF	VDS = 20 V, VGS = 0		
19 Crss Common-Source Reverse Transfer Capacitance						3.5			VGS = -5 V	f = 1 MHz
		3.5				3.5			VGS = -7 V	
20 VGS = -12 V								VGS = -12 V		
21 tD(on) Turn-ON Delay Time		15		15		15	ns	VDD = 10 V, VGS(on) = 0	RL	
22 tr Rise Time		5		5		5				
23 tD(off) Turn-OFF Delay Time		20		35		50				PN4391 12 mA -12 V 800 Ω
	24 tf Fall Time		15		20	30				PN4392 6 -7 1.6K
								PN4393 3 -5 3.2K		

2

NC

NOTE:
 1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

n-channel JFETs designed for . . .



Performance Curves NH
See Section 4

- VHF Amplifiers
- Mixers

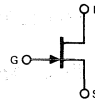
BENEFITS

- Low Noise
NF = 3 dB Typical at 400 MHz
- Wide Band
High g_{fs}/C_{iss} Ratio

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -30V
 Gate Current 10 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C

TO-92
See Section 6



Plastic



Bottom View
Source & Drain Interchangeable

Characteristic		Min	Max	Unit	Test Conditions	
S T A T I C	1 I_{GSS} Gate Reverse Current		1.0	nA	$V_{GS} = -15\text{ V}, V_{DS} = 0\text{ V}$	
	3 BV_{GSS} Gate-Source Breakdown Voltage	-30		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0\text{ V}$	
	4 $V_{GS(off)}$ Gate-Source Cutoff Voltage		-6		$V_{DS} = 15\text{ V}, I_D = 1\text{ nA}$	
	5 I_{DSS} Saturation Drain Current (Note 1)	5	15	mA		
D Y N A M I C	6 g_{fs} Common-Source Forward Transconductance	4500	7500	μmho	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	
	7 g_{os} Common-Source Output Conductance		50			f = 1 kHz
	8 C_{rss} Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
	9 C_{iss} Common-Source Input Capacitance		4			
10 C_{oss} Common-Source Output Capacitance		2				

Characteristic	100 MHz		400 MHz		Unit	Test Conditions
	Min	Max	Min	Max		
11 g_{iss} Common-Source Input Conductance		100		1000	μmho	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$
12 b_{iss} Common-Source Input Susceptance		2500		10,000		
13 g_{oss} Common-Source Output Conductance		75		100		
14 b_{oss} Common-Source Output Susceptance		1000		4000		
15 g_{fs} Common-Source Forward Transconductance			4000		dB	$V_{DS} = 15\text{ V}, I_D = 5\text{ mA}$
16 G_{ps} Common-Source Power Gain	18		10			$V_{DS} = 15\text{ V}, I_D = 5\text{ mA}, R_G = 1\text{ K}\ \Omega$
17 NF Noise Figure		2		4		

NH

NOTES:

1. Pulse test duration = 300 μs .

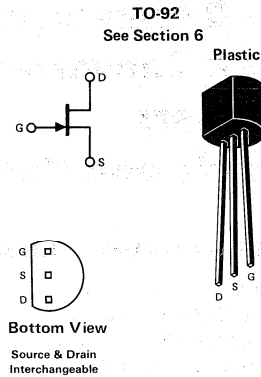
n-channel JFET designed for . . .

■ Low and Medium Frequency Amplifiers

- BENEFITS**
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -25V
 Gate Current (FWD) 10 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C) 360 mW
 Operating Temperature Range -55 to 135°C
 Storage Temperature Range -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	Min	Max	Unit	Test Conditions		
1 2 3 4 5	S T A T I C	I_{GSS} Gate Reverse Current		-10 -0.6	nA μ A	$V_{GS} = -15$ V, $V_{DS} = 0$	$T_A = 85^\circ$ C	
		BV_{GSS} Gate-Source Breakdown Voltage	-25		V			$I_G = -10$ μ A, $V_{DS} = 0$
		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-0.4	-8.0				$V_{DS} = 15$ V, $I_D = 1$ μ A
		V_{GS} Gate-Source Voltage		-7.5				$V_{DS} = 15$ V, $I_D = 100$ μ A
6		I_{DSS} Saturation Drain Current	1.0	40	mA	$V_{DS} = 15$ V, $V_{GS} = 0$		
7		$r_{ds(on)}$ Drain-Source ON Resistance		500	Ω	$V_{GS} = 0$, $I_D = 0$		
8 9 10 11	D Y N A M I C	g_{fs} Common-Source Forward Transconductance	2000	9000	μ mho	$V_{DS} = 15$ V, $V_{GS} = 0$	$f = 1$ kHz	
		g_{os} Common-Source Output Conductance		200				
		g_{fs} Common-Source Forward Transconductance	1800		pF		$f = 1$ MHz	
		C_{iss} Common-Source Input Capacitance		20				
12		C_{rss} Common-Source Reverse Transfer Capacitance		5.0				
13		NF Common-Source Spot Noise Figure		3.0	dB	$R_G = 150k$ Ω	$f = 1$ kHz	
14		e_N Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 15$ V, $I_D = 1$ mA	NBW = 150 Hz	

*JEDEC registered data

2

n-channel DMOS FETs designed for. . .



- High-Speed Switching
- Analog Switch
- Multiplexer
- Digital Switch
- A to D Converters
- D to A Converters
- Choppers
- Sample and Hold

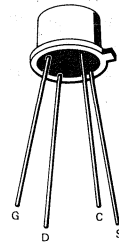
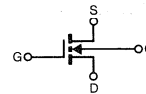
BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1 ns)
- Gate can accept $\pm 40V$

ABSOLUTE MAXIMUM RATINGS (°C)

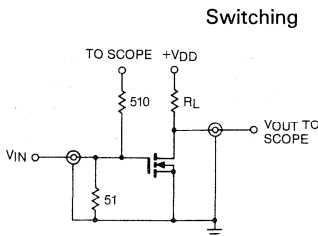
Drain Current	50mA
Total Device Dissipation at 25°C		
Case Temperature	1.2W
Storage Temperature Range	-55 to +125°C
Lead Temperature (1/16" from case for 10 sec.)	300°C

TO-72
See Section 6



PARAMETER	SD210	SD212	SD214	UNIT
V _{DS} Drain-to-source	+30	+10	+20	Vdc
V _{SD} Source-to-drain*	+10	+10	+20	Vdc
V _{DB} Drain-to-substrate	+30	+15	+25	Vdc
V _{SB} Source-to-substrate	+15	+15	+25	Vdc
V _{GS} Gate-to-source	± 40	± 40	± 40	Vdc
V _{GB} Gate-to-substrate	± 40	± 40	± 40	Vdc
V _{GD} Gate-to-drain	± 40	± 40	± 40	Vdc

TEST CONDITIONS

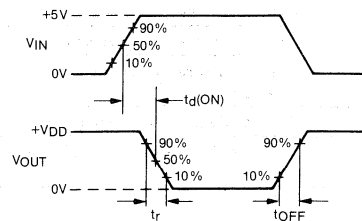


Input pulse: $t_d, t_r < 1\text{ ns}$
Pulse width = 100ns
Rep rate = 1 MHz

SAMPLING SCOPE

$t_r < 360\text{ ps}$
 $R_{IN} = 1\text{ M}\Omega$
 $C_{IN} = 2.0\text{ pF}$

Typical Switching Waveform



SWITCHING CHARACTERISTICS

VDD	RL	td(ON) (ns)		tr(ns)		tOFF(ns)	
		Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7	0.8	0.8	1.0	9.0	*
15	1k	0.9	1.0	1.0	1.0	14.0	*

*tOFF is dependent on RL and CL and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

	PARAMETER	TEST CONDITIONS	SD210			SD212			SD214			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Breakdown voltage BV _{DS} Drain-to-source	V _{GS} = V _{BS} = 0V, I _D = 10μA V _{GS} = V _{BS} = -5V, I _S = 10nA	30	35		10	25		20	25	V	
			10	25		10	25		20	25		
	BV _{SD} Source-to-drain	V _{GD} = V _{BD} = -5V I _D = 10nA	10			10			20			
BV _{DB} Drain-to-substrate	V _{GB} = 0V, source OPEN I _D = 10nA	15			15			25				
BV _{SB} Source-to-substrate	V _{GB} = 0V, drain OPEN I _S = 10μA	15			15			25				
5	Leakage current I _{DS} (OFF) Drain-to-source	V _{GS} = V _{BS} = -5V V _{DS} = +10V V _{DS} = +20V		1	10				1	10	nA	
6	I _{SD} (OFF) Source-to-drain	V _{GD} = V _{BD} = -5V V _{SD} = +10V V _{SD} = +20V		1	10				1	10		
7	I _{GBS} Gate	V _{DB} = V _{SB} = 0V V _{GB} = ±40V			0.1				0.1	0.1		
8	V _T Threshold voltage	V _{DS} = V _{GS} = V _T , I _S = 1μA V _{SB} = 0V	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	
9	r _{DS} (ON) Drain-to-source resistance	I _D = 1.0mA, V _{SB} = 0 V _{GS} = +5V V _{GS} = +10V V _{GS} = +15V V _{GS} = +20V V _{GS} = +25V		50	70				50	70	Ω	
				30	45				30	45		
				23					23			
				19					19			
				17					17			

AC ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	SD210			SD212			SD214			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
10	g _{fs} Forward trans-conductance	V _{DS} = 10V, V _{SB} = 0V I _D = 20mA, f = 1kHz	10	15		10	15		10	15	mmhos	
11	Small Signal Capacitances (See capacitance model)	V _{DS} = 10V, f = 1MHz V _{GS} = V _{BS} = -15V									pF	
			C _(GS+GD+GB) Gate node	2.4	3.5		2.4	3.5		2.4		3.5
			C _(GD+DB) Drain node	1.3	1.5		1.3	1.5		1.3		1.5
			C _(GS+SB) Source node	3.5	4.0		3.5	4.0		3.5		4.0
			C _{DG} Reverse transfer	0.3	0.5		0.3	0.5		0.3		0.5

2

n-channel DMOS FETs designed for. . .



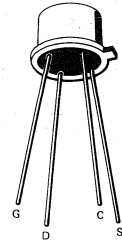
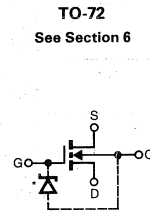
- High-Speed Switching
- Analog Switch
- Multiplexer
- Digital Switch
- A to D Converters
- D to A Converters
- Choppers
- Sample and Hold

BENEFITS

- Ultra low feedback capacitance (0.30pF)
- High switching speeds (<1 ns)
- Diode protected gate

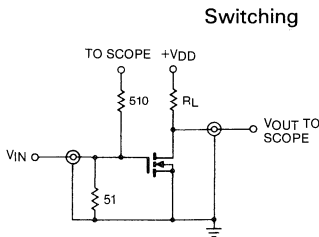
ABSOLUTE MAXIMUM RATINGS (°C)

Drain Current50mA
Total Device Dissipation at 25°C	
Case Temperature1.2W
Storage Temperature Range-55 to +125°C
Lead Temperature (1/16" from case for 10 sec.)300°C



PARAMETER	SD211	SD213	SD215	UNIT
V _{DS} Drain-to-source	+30	+10	+20	Vdc
V _{SD} Source-to-drain*	+10	+10	+20	Vdc
V _{DB} Drain-to-substrate	+30	+15	+25	Vdc
V _{SB} Source-to-substrate	+15	+15	+25	Vdc
V _{GS} Gate-to-source	-15 +25	-15 +25	-25 +30	Vdc
V _{GB} Gate-to-substrate	-0.3 +25	-0.3 +25	-0.3 +30	Vdc
V _{GD} Gate-to-drain	-30 +25	-15 +25	-25 +30	Vdc

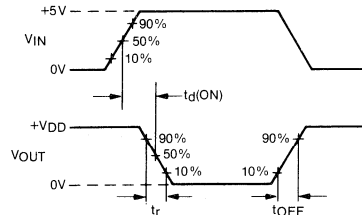
TEST CONDITIONS



Input pulse: $t_d, t_r < 1$ ns
Pulse width = 100ns
Rep rate = 1 MHz

SAMPLING SCOPE
 $t_r < 360$ ps
 $R_{IN} = 1$ M Ω
 $C_{IN} = 2.0$ pF

Typical Switching Waveform



SWITCHING CHARACTERISTICS

VDD	RL	td(ON) (ns)		tr(ns)		toff(ns)	
		Typ	Max	Typ	Max	Typ	Max
5	880	0.6	1.0	0.7	1.0	9.0	*
10	880	0.7	1.0	0.8	1.0	9.0	*
15	1k	0.9	1.0	1.0	1.0	14.0	*

*toff is dependent on RL and CL and does not depend on the device characteristics.

DC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

	PARAMETER	TEST CONDITIONS	SD211			SD213			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
S T A T I C	Breakdown voltage BV_{DS} Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$ $V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	30	35				20	25			V
	BV_{SD} Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10		20				
	BV_{DB} Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15		25				
	BV_{SB} Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15		25				
	Leakage current I_{DS} (OFF) Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$ $V_{DS} = +20V$		1	10		1	10		1	10	nA
	I_{SD} (OFF) Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$ $V_{SD} = +20V$		1	10		1	10		1	10	
	I_{GBS} Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = +25V$ $V_{GB} = +30V$			10			10			10	μA
	V_T Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
	r_{DS} (ON) Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		50	70		50	70		50	70	Ω
			30	45		30	45		30	45		
				23			23			23		
				19			19			19		
										17		

AC ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	SD211			SD213			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
10	g_{fs} Forward trans-conductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		mmhos
D Y N A M I C	Small Signal Capacitances (See capacitance model)	$V_{DS} = 10V$, $f = 1MHz$ $V_{GS} = V_{BS} = -15V$										pF
	$C_{(GS+GD+GB)}$ Gate node		2.4	3.5		2.4	3.5		2.4	3.5		
	$C_{(GD+DB)}$ Drain node		1.3	1.5		1.3	1.5		1.3	1.5		
	$C_{(GS+SB)}$ Source node		3.5	4.0		3.5	4.0		3.5	4.0		
	C_{DG} Reverse transfer		0.3	0.5		0.3	0.5		0.3	0.5		

n-channel JFETs designed for . . .



- Analog Switches
- Commutators
- Choppers

Performance Curves NC
See Section 4

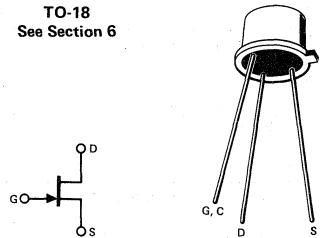
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 50 \Omega$ (U202)
- Good Off-Isolation
 $I_{D(off)} < 1 \text{ nA}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -30 V
 Gate Current 50 mA
 Total Device Dissipation at 25°C Case Temperature
 (Derate 10 mW/°C) 1.8 W
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-18
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		U200		U201		U202		Unit	Test Conditions			
		Min	Max	Min	Max	Min	Max					
S T A T I C	1	IGSS	Gate Reverse Current		-1		-1		nA	VGS = -20 V, VDS = 0		
					-1		-1		-1		µA	150°C
	3	BVGSS	Gate-Source Breakdown Voltage	-30		-30		-30		V	IG = -1 µA, VDS = 0	
4	VGS(off)	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		VDS = 20 V, ID = 10 nA		
5	ID(off)	Drain Cutoff Current		1		1		1	nA	VDS = 10 V, VGS = -12 V		
				1		1		1	µA		150°C	
6	IDSS	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	VDS = 20 V, VGS = 0		
7	rdS(on)	Drain-Source ON Resistance		150		75		50	ohm	VGS = 0, ID = 0	f = 1 kHz	
D Y N	8	Ciss	Common-Source Input Capacitance (Note 1)		30		30		30	pF	VDS = 20 V, VGS = 0	f = 1 MHz
					8		8		8		VDS = 0, VGS = -12 V	
9	Crss	Common-Source Reverse Transfer Capacitance		8		8		8		VDS = 0, VGS = -12 V		

NOTE:

1. Pulse test required, pulsewidth = 300 µsec, duty cycle ≤ 3%.

NC



monolithic dual n-channel JFETs designed for . . .

Performance Curves NQP
See Section 4

■ Differential Amplifiers

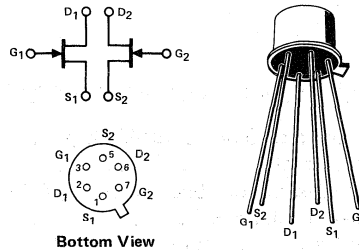
BENEFITS

- Good Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	50 mA
Total Device Dissipation at 25°C (Derate 1.7 mW/°C to 200°C)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions	
1	I _{GSS} Gate Reverse Current		-100	pA	V _{GS} = -30 V, V _{DS} = 0	150°C
2			-500	nA		
3	BV _{GSS} Gate-Source Breakdown Voltage	-50			I _G = -1 μA, V _{DS} = 0	
4	V _{GS(off)} Gate-Source Cutoff Voltage	-0.5	-4.5	V	V _{DS} = 20 V, I _D = 1 nA	
5	V _{GS} Gate-Source Voltage	-0.3	-4.0			
6	I _G Gate Operating Current		-50	pA	V _{DG} = 20 V, I _D = 200 μA	125°C
			-250	nA		
7	I _{DSS} Saturation Drain Current (Note 1)	0.5	5.0	mA	V _{DS} = 20 V, V _{GS} = 0	
8	g _{fs} Common-Source Forward Transconductance (Note 1)	1000	5000		V _{DS} = 20 V, V _{GS} = 0	f = 1 kHz
		1000				f = 100 MHz
9	g _{fs} Common-Source Forward Transconductance (Note 1)	600	1600	μmho	V _{DG} = 20 V, I _D = 200 μA	
10	g _{os} Common-Source Output Conductance		35		V _{DS} = 20 V, V _{GS} = 0	f = 1 kHz
11	g _{os} Common-Source Output Conductance		10		V _{DG} = 20 V, I _D = 200 μA	
12	C _{iss} Common-Source Input Capacitance		6	pF	f = 1 MHz	
13	C _{rss} Common-Source Reverse Transfer Capacitance		2		V _{DS} = 20 V, V _{GS} = 0	
14	e _n Equivalent Short Circuit Input Noise Voltage		80	nV/√Hz	f = 100 Hz	

Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	I _{G1} - I _{G2} Differential Gate Current	10	10	10	10	10	nA	V _{DG} = 20 V, I _D = 200 μA	125°C
16	$\frac{ I_{DSS1} - I_{DSS2} }{I_{DSS1}}$ Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V _{DS} = 20 V, V _{GS} = 0	
17	V _{GS1} - V _{GS2} Differential Gate-Source Voltage	5	10	15	20	25	mV	V _{DG} = 20 V, I _D = 200 μA	
18	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		
19		10	25	50	75	100			
20	$\frac{(g_{fs1} - g_{fs2})}{g_{fs1}}$ Transconductance Match (Note 1)	3	5	5	10	15	%		
21	g _{os1} - g _{os2} Differential Output Conductance	5	5	5	5	5	μmho	f = 1 kHz	

NOTES:

1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

NQP

2

matched dual n-channel JFET designed for . . .



Performance Curves NZF-D
See Section 4

■ Wideband Differential Amplifiers

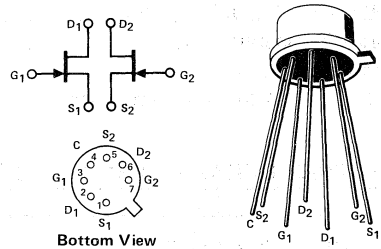
BENEFITS

- High Gain through 100 MHz
 $g_{fs} = 5000 \mu\text{mho}$ Minimum
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 85^\circ\text{C}$ (Derate $3.85 \text{ mW}/^\circ\text{C}$)	250 mW
Total Device Dissipation, $T_A = 85^\circ\text{C}$ (Derate $7.7 \text{ mW}/^\circ\text{C}$)	500 mW
Storage Temperature Range	-65 to + 200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

Characteristic		Min	Max	Unit	Test Conditions	
1 S T A T I C	I_{GSS} Gate Reverse Current		-100	pA	$V_{GS} = -15 \text{ V}, V_{DS} = 0$ 150°C	
			-250	nA		
	BV_{GSS} Gate-Source Breakdown Voltage	-25		V	$I_G = -1 \mu\text{A}, V_{DS} = 0$	
4 D Y N A M I C	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-1	-5		$V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$	
	I_{DSS} Saturation Drain Current (Note 1)	5	40	mA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$	
	g_{fs} Common-Source Forward Transconductance	5000	10,000	μmho	$V_{DS} = 10 \text{ V}, I_D = 5 \text{ mA}$	$f = 1 \text{ kHz}$
		5000	10,000		$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$	$f = 100 \text{ MHz}$
	g_{os} Common-Source Output Conductance		150		$V_{DS} = 10 \text{ V}, I_D = 5 \text{ mA}$	$f = 1 \text{ kHz}$
g_{os} Common-Source Output Conductance		150			$f = 100 \text{ MHz}$	
10 M I C	C_{iss} Common-Source Input Capacitance		5	pF	$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$	$f = 1 \text{ MHz}$
	C_{rss} Common-Source Reverse Transfer Capacitance		1.2			$f = 10 \text{ kHz}$
12	\bar{e}_n Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{\text{Hz}}}$		$f = 10 \text{ kHz}$
13 M A T C H I N G	$\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		$V_{DS} = 10 \text{ V}, V_{GS} = 0$	
14 H I N G	$ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		100	mV	$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$	
		$\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Note 2)	0.85	1		
	$ g_{os1} - g_{os2} $ Differential Output Conductance			20		μmho

NOTES:
1. Pulse test required, pulse width = 300 μs , duty cycle $\leq 30\%$.
2. Assumes smaller value in numerator.

NZF-D

n-channel JFETs designed for . . .



U290 U291

- Analog Switches
- Commutators
- Choppers

Performance Curves NVA
See Section 4

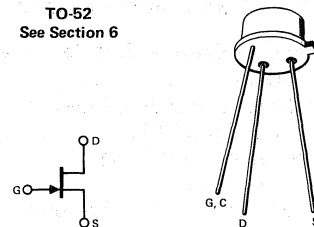
BENEFITS

- Ultra-Low Insertion Loss
 $r_{DS(on)} < 2.5 \Omega$ (U290)
- High Off-Isolation
 $I_{D(off)} < 1 \text{ nA}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage -30 V
 Gate Current 100 mA
 Drain Current 1.5 A
 Total Device Dissipation at 25°C
 Free-Air Temperature (Note 1) 500 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-52
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U290		U291		Unit	Test Conditions	
	Min	Max	Min	Max			
1 I _{GSS} Gate Reverse Current		-1	-1	-1	nA	V _{GS} = -15 V, V _{DS} = 0	150°C
2		-1	-1	-1	μA		
3 BV _{GS} Gate-Source Breakdown Voltage	-30		-30		V	I _G = -1 μA, V _{DS} = 0	
4 V _{GS(off)} Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		V _{DS} = 15 V, I _D = 3 nA	
5 I _{D(off)} Drain Cutoff Current		1		1	nA	V _{DS} = 5 V, V _{GS} = -10 V	150°C
6		1		1	μA		
7 V _{DS(on)} Drain-Source ON Voltage		25		70	mV	V _{GS} = 0, I _D = 10 mA	
8 I _{DSS} Saturation Drain Current (Note 2)	500		200		mA	V _{DS} = 10 V, V _{GS} = 0	
9 r _{DS(on)} Static Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V _{GS} = 0 V, I _D = 10 mA	
10 r _{ds(on)} Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V _{GS} = 0, I _D = 0	f = 1 kHz
11 C _{SGO} Source-Gate OFF Capacitance		30		30	pF	V _{GS} = 15 V, I _D = 0	f = 1 MHz
12 C _{DGO} Drain-Gate OFF Capacitance		30		30		V _{DG} = 15 V, I _S = 0	
13 C _{SG+C_{DG}} Source Gate Plus Drain Gate On Capacitance		160		160		V _{DS} = 0, V _{GS} = 0	
14 t _{d(on)} Turn-ON Delay Time		15		15	ns	V _{DD} = 1.5 V, I _{D(on)} = 30 mA, R _L = 50 Ω, V _{GS(on)} = 0 V, V _{GS(off)} = -12 V (U290) V _{GS(off)} = -7 V (U291)	
15 t _r Rise Time		20		20			
16 t _{d(off)} Turn-OFF Delay Time		15		15			
17 t _f Fall Time		20		20			

NOTES:

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

NVA

2

p-channel JFETs designed for . . .



Performance Curves PS
See Section 4

- Analog Switches
- Commutators
- Choppers

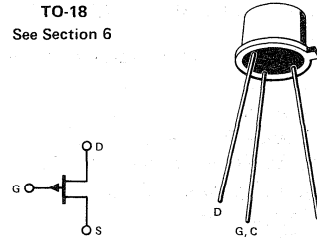
BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 85 \Omega$ (U304)
- High Off-Isolation
 $I_{D(off)} < 500 \text{ pA}$

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . . 30 V
 Gate Current 50 mA
 Total Device Dissipation, Free-Air
 (Derate 2.8 mW/°C) 350 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 60 seconds) 300°C

TO-18
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		U304		U305		U306		Unit	Test Conditions			
		Min	Max	Min	Max	Min	Max					
1 2 3 4 5 6 7 8 9 10 11 12	S T A T I C	I _{GSS}	Gate Reverse Current		500		500		500	pA	V _{GS} = 20 V, V _{DS} = 0 150°C	
				1.0		1.0		1.0				
		BV _{GSS}	Gate-Source Breakdown Voltage		30		30		30		V	I _G = 1 μA, V _{DS} = 0 V _{DS} = -15 V, I _D = -1 μA
V _{GS(off)}	Gate-Source Cutoff Voltage		5	10	3	6	1	4				
		V _{DS(on)}	Drain-Source ON Voltage		-1.3		-0.8		-0.6	mA	V _{DS} = -15 V, V _{GS} = 0 V _{DS} = -15 V, I _D = -15 mA (U304), I _D = -7 mA (U305), I _D = -3 mA (U306)	
		I _{DSS}	Saturation Drain Current (Note 2)		-30	-90	-15	-60	-5			-25
		I _{D(off)}	Drain Cutoff Current		-500		-500		-500	pA	V _{DS} = -15 V, V _{GS} = 12 V (U304), V _{GS} = 7 V (U305), V _{GS} = 5 V (U306) 150°C	
				-1.0		-1.0		-1.0				
		r _{DS(on)}	Static Drain-Source ON Resistance		85		110		175	Ω	V _{GS} = 0 V, I _D = -1 mA	
		r _{ds(on)}	Drain-Source ON Resistance		85		110		175			
	D Y N A M I C	C _{iss}	Common-Source Input Capacitance		27		27		27	pF	V _{DS} = -15 V, V _{GS} = 0 f = 1 kHz V _{DS} = 0, V _{GS} = 12 V (U304), V _{GS} = 7 V (U305), V _{GS} = 5 V (U306) f = 1 MHz	
			C _{rss}	Common-Source Reverse Transfer Capacitance		7		7				7
13 14 15 16	S W I T C H	t _{d(on)}	Turn-ON Delay Time		20		25		25	ns	U304 U305 U306 V _{DD} -10 V -6 V -6 V V _{GS(off)} 12 V 7 V 5 V R _L 580 Ω 743 Ω 1800 Ω V _{GS(on)} 0 0 0 I _{D(on)} -15 mA -7 mA -3 mA	
			t _r	Rise Time		15		25				35
		t _{d(off)}	Turn-OFF Delay Time		10		15		20			
		t _f	Fall Time		25		40		60			

NOTES:
 1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
 2. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

PS

n-channel JFETs designed for . . .



- VHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

Performance Curves NZA
See Section 4

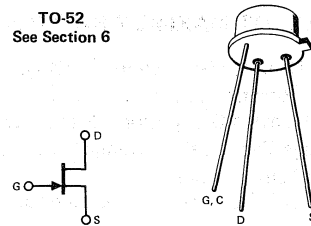
BENEFITS

- Industry Standard
- High Power Gain
16 dB at 105 MHz, Common-Gate
11 dB at 450 MHz, Common-Gate
- Low Noise
2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -25 V
 Gate Current 20 mA
 Total Power Dissipation at T_A = 25°C 500 mW
 Power Derating to 150°C 4.0 mW/°C
 Storage Temperature Range -65 to + 200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-52
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U308			U309			U310			Unit	Test Conditions	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1 2 S T A T I C	I _{GSS}	Gate Reverse Current		-150		-150		-150		pA	V _{GS} = -15 V, V _{GS} = 0	T _A = 125°C
				-150		-150		-150		nA		
3	BV _{GSS}	Gate-Source Breakdown Voltage		-25		-25		-25		V	I _G = -1 μA, V _{DS} = 0	
4	V _{GS(off)}	Gate-Source Cutoff Voltage		-1.0	-6.0	-1.0	-4.0	-2.5	-6.0		V _{DS} = 10 V, I _D = 1 nA	
5	I _{DSS}	Saturation Drain Current (Note 1)		12	60	12	30	24	60	mA	V _{DS} = 10 V; V _{GS} = 0	
6	V _{GS(f)}	Gate-Source Forward Voltage			1.0		1.0		1.0	V	I _G = 10 mA, V _{DS} = 0	
7 8 D Y N A M I C	g _{fg}	Common-Gate Forward Transconductance (Note 1)		10	17	10	17	10	17	mmho	V _{DS} = 10 V, I _D = 10 mA	f = 1 kHz
		g _{og}	Common-Gate Output Conductance			250		250		250		
9	C _{gd}	Drain-Gate Capacitance			2.5		2.5		2.5	pF	V _{GS} = -10 V, V _{DS} = 10 V	
10	C _{gs}	Gate-Source Capacitance			5.0		5.0		5.0		f = 1 MHz	
11	e _n	Equivalent Short Circuit Input Noise Voltage			10		10		10	nV/√Hz	V _{DS} = 10 V, I _D = 10 mA	
12 13 H I	g _{fg}	Common-Gate Forward Transconductance			15		15		15	mmho	V _{DS} = 10 V, I _D = 10 mA	f = 105 MHz
				14		14		14	f = 450 MHz			
14 15 F R E Q	g _{og}	Common-Gate Output Conductance			0.18		0.18		0.18	mmho	V _{DS} = 10 V, I _D = 10 mA	f = 105 MHz
				0.32		0.32		0.32	f = 450 MHz			
16 17 R E Q	G _{pg}	Common-Gate Power Gain (Note 2)		14	16	14	16	14	16	dB	V _{DS} = 10 V, I _D = 10 mA	f = 105 MHz
				10	11	10	11	10	11			f = 450 MHz
18 19	NF	Noise Figure		1.5	2.0	1.5	2.0	1.5	2.0	dB	V _{DS} = 10 V, I _D = 10 mA	f = 105 MHz
				2.7	3.5	2.7	3.5	2.7	3.5			f = 450 MHz

NOTES:

1. Pulse test duration = 2 ms.
2. Gain (G_{pg}) measured at optimum input noise match.

NZA

U308 U309 U310
PLASTIC EQUIVALENT J308 SERIES

2

n-channel JFET designed for . . .



- VHF Amplifiers
- Oscillators
- Mixers

Performance Curves NZA
See Section 4

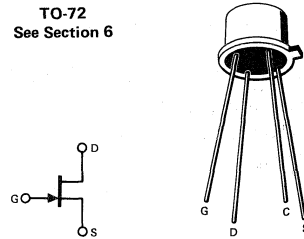
BENEFITS

- High Power Gain
16 dB Typ @ 105 MHz, Common-Gate
11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
1.5 dB Typ @ 105 MHz
2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -25 V
 Gate Current 10 mA
 Total Device Dissipation (Derate 1.7 mW/°C) 300 mW
 Storage Temperature Range -65 to +200°C
 Lead Temperature
 (1/16" from case for 10 seconds) 300°C

TO-72
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic		Min	Max	Typ	Unit	Test Conditions	
S T A T I C	I _{GSS} Gate Reverse Current		-150		pA	V _{GS} = -15 V, V _{DS} = 0	
			-150		nA		150°C
	BV _{GSS} Gate-Source Breakdown Voltage	-25			V	I _G = -1 μA, V _{DS} = 0	
	V _{GS(off)} Gate-Source Cutoff Voltage	-1	-6			V _{DS} = 10 V, I _D = 1 nA	
	I _{DSS} Saturation Drain Current (Note 1)	20	60		mA	V _{DS} = 10 V, V _{GS} = 0	
V _{GS(f)} Gate-Source Forward Voltage		1		V	I _G = 1 mA, V _{DS} = 0		
D Y N	g _{fg} Common-Gate Forward Transconductance (Note 1)	10,000		17,000	μmho	V _{DS} = 10 V, I _D = 10 mA	f = 1 kHz
	g _{og} Common-Gate Output Conductance		250				
	C _{gd} Gate-Drain Capacitance		2.5		pF	V _{DG} = 10 V, I _D = 5 mA	f = 1 MHz
	C _{gs} Gate-Source Capacitance		5.0				

NOTE:
1. Pulse test duration = 2 ms.

NZA



monolithic dual n-channel JFETs designed for . . .

- Low Noise FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

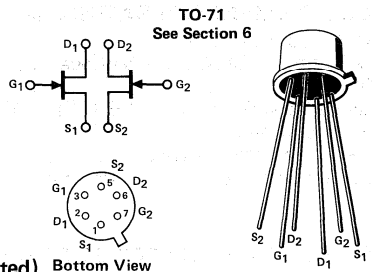
Performance Curves NNR
See Section 4

BENEFITS

- Minimum System Error and Calibration
5 mV Offset Maximum (U401)
95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
10 $\mu\text{V}/^\circ\text{C}$ Maximum (U401, 02)
- Operates from Low Power Supply Voltages
 $V_{GS(\text{off})} < 2.5 \text{ V}$
- Simplifies Amplifier Design
Output Conductance $< 2 \mu\text{mho}$
- Low Noise
 $\bar{e}_n = 6 \text{ nV}/\sqrt{\text{Hz}}$ at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side) @ $T_A = 85^\circ\text{C}$ derate 2.6 mW/ $^\circ\text{C}$	300 mW
Total Device Dissipation @ $T_A = 85^\circ\text{C}$ (derate 5 mW/ $^\circ\text{C}$)	500 mW
Storage Temperature Range	-65 to 200°C



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted) Bottom View

Characteristic	U401		U402		U403		U404		U405		U406		Unit	Test Conditions
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1 BV_{GSS} Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	$V_{DS} = 0, I_G = -1 \mu\text{A}$
2 I_{GSS} Gate Reverse Current (Note 1)		-25		-25		-25		-25		-25		-25	pA	$V_{DS} = 0, V_{GS} = -30 \text{ V}$
3 $V_{GS(\text{off})}$ Gate-Source Cutoff Voltage	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	V	$V_{DS} = 15 \text{ V}, I_D = 1 \text{ nA}$
4 $V_{GS(\text{on})}$ Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3		$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$
5 I_{DSS} Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$
6 I_G Gate Current (Note 1)		-15		-15		-15		-15		-15		-15	pA	$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$
7 I_G Gate Current (Note 1)		-10		-10		-10		-10		-10		-10	nA	$T_A = 125^\circ\text{C}$
8 BV_{G1-G2} Gate-Gate Breakdown Voltage	± 50		± 50		± 50		± 50		± 50		± 50		V	$V_{DS} = 0, V_{GS} = 0, I_G = \pm 1 \mu\text{A}$
9 g_{fs} Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000		$V_{DS} = 10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ kHz}$
10 g_{os} Common-Source Output Conductance		20		20		20		20		20		20	μmho	
11 g_{fs} Common-Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000		$f = 1 \text{ kHz}$
12 g_{os} Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0		$V_{DG} = 15 \text{ V}, I_D = 200 \mu\text{A}$ $f = 1 \text{ MHz}$
13 C_{iss} Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF	
14 C_{rss} Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0		
15 \bar{e}_n Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\mu\text{V}/\sqrt{\text{Hz}}$	$V_{DS} = 15 \text{ V}, V_{GS} = 0$ $f = 10 \text{ Hz}$
16 CMRR Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	$V_{DG} = 10 \text{ to } 20 \text{ V}, I_D = 200 \mu\text{A}$
17 $ V_{GS1} - V_{GS2} $ Differential Gate-Source Voltage		5		10		10		15		20		40	mV	$V_{DG} = 10 \text{ V}, I_D = 200 \mu\text{A}$
18 $\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$ Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10 \text{ V}, I_D = 200 \mu\text{A}$ $T_A = -55^\circ\text{C}, T_B = +25^\circ\text{C}$ $T_C = +125^\circ\text{C}$

NOTES:
 1. Approximately doubles for every 10°C increase in T_A . 2. Pulse test duration = 300 μs ; duty cycle $\leq 3\%$. 3. CMRR = $20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right]$. $\Delta V_{DD} = 10 \text{ V}$.
 4. Measured at end points, T_A, T_B and T_C . NNR

monolithic dual n-channel JFETs designed for . . .



- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

Performance Curves NQP
See Section 4

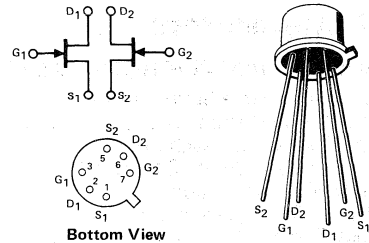
BENEFITS

- Low Cost
- Minimum System Error and Calibration
10 mV Offset Maximum (U410)
70 dB Minimum CMRR (U410)
- Low Drift with Temperature
10 $\mu\text{V}/^\circ\text{C}$ Maximum (U410)
- Simplifies Amplifier Design
Low Output Conductance

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air)	375 mW
Power Derating	3.0 mW/°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	.300°C

TO-71
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U410			U411			U412			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1 I _{GSS} Gate Reverse Current (Note 1)			-200			-200			-200	pA	V _{DS} = 0, V _{GS} = -30 V
2 V _{GS(off)} Gate-Source Cutoff Voltage	-1.0	-3.5		-1.0	-3.5		-1.0	-3.5		V	V _{DS} = 20 V, I _D = 1 nA
3 BV _{GS} Gate-Source Breakdown Voltage	-40			-40			-40				V _{DS} = 0 V, I _G = -1 μA
4 I _{DSS} Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	V _{DS} = 20 V, V _{GS} = 0 V
5 I _G Gate Current (Note 1)			-200			-200			-200	pA	V _{DG} = 20 V, I _D = 200 μA
6 V _{GS} Gate-Source Voltage	-0.2	-3.0		-0.2	-3.0		-0.2	-3.0		V	
7 g _{fs} Common-Source Forward Transconductance	1,000	4,000		1,000	4,000		1,000	4,000		μmho	V _{DS} = 20 V, V _{GS} = 0 V
	600	1,200	600	1,200	600	1,200					V _{DG} = 20 V, I _D = 200 μA
		20		20		20					V _{DS} = 20 V, V _{GS} = 0 V
9 g _{os} Common-Source Output Conductance			5			5			5		V _{DG} = 20 V, I _D = 200 μA
11 C _{iss} Common-Source Input Capacitance		4.5			4.5			4.5		pF	V _{DS} = 20 V, V _{GS} = 0 V
12 C _{rss} Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2			f = 1 MHz
13 \bar{e}_n Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	V _{DS} = 20 V, I _D = 200 μA
14 V _{GS1} -V _{GS2} Differential Gate-Source Voltage			10			20			40	mV	V _{DG} = 20 V, I _D = 200 μA
15 $\frac{\Delta V_{GS1}-V_{GS2} }{\Delta T}$ Gate-Source Differential Drift (Note 3)			10			25			80	$\mu\text{V}/^\circ\text{C}$	V _{DG} = 20 V, I _D = 200 μA T _A = 25°C to T _B = 85°C
16 CMRR Common-Mode Rejection Ratio (Note 4)		80		80				70		dB	V _{DD} = 10 V to V _{DD} = 20 V I _D = 200 μA

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec ; duty cycle \leq 3%.
3. Measured at end points, T_A and T_B.
4. $\text{CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right]$, $\Delta V_{DD} = 10 \text{ V}$.

NQP

monolithic dual n-channel JFETs designed for . . .



Performance Curves NNT See Section 4

BENEFITS

- High Input Impedance
 $I_G = 0.25 \mu A$ Maximum (U421-3)
- High Gain $g_{fs} = 120 \mu mho$ Minimum @
 $I_D = 30 \mu A$ (U421-6)
- Low Power Supply Operation
 $V_{GS(off)} = 2 V$ Maximum (U421-3)
- Minimum System Error and Calibration
10 mV Maximum Offset
90 dB Minimum CMRR (U421, U424)

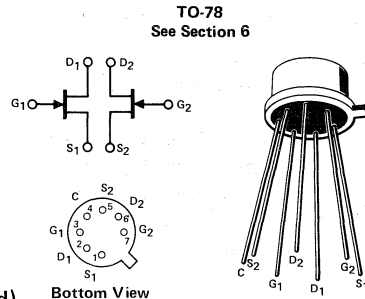
Very High Input Impedance Differential Amplifiers

Electrometers

Impedance Converters

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), $T_A = 25^\circ C$ (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, $T_A = 25^\circ C$ (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	-65 to +150°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U421-3			U424-6			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max		
1 S BV _{GSS} Gate-Source Breakdown Voltage	-40	-60		-40	-60		V	$I_G = -1 \mu A, V_{DS} = 0$
2 T BV _{G1G2} Gate-Gate Breakdown Voltage	±40			±40			V	$I_G = -1 \mu A, I_D = 0, I_S = 0$
3 A I _{GSS} Gate Reverse Current (Note 1)			1.0			3.0	pA	$V_{GS} = -20 V, V_{DS} = 0$
			1.0			3.0	nA	
4 T I _G Gate Operating Current (Note 1)			.25			0.5	pA	$V_{DG} = 10 V, I_D = 30 \mu A$
			250			500	pA	
5 A V _{GS(off)} Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-3.0	V	$V_{DS} = 10 V, I_D = 1 nA$
6 T V _{GS} Gate-Source Voltage			-1.8			-2.9	V	$V_{DG} = 10 V, I_D = 30 \mu A$
7 A I _{DSS} Saturation Drain Current	60		1000	60		1800	μA	$V_{DS} = 10 V, V_{GS} = 0$
8 T g _{fs} Common-Source Forward Transconductance	300		1500	300		1500	μS	$V_{DS} = 10 V, V_{GS} = 0$
9 A g _{os} Common-Source Output Conductance			5.0			5.0	μS	
10 T C _{iss} Common-Source Input Capacitance			3.0			3.0	pF	f = 1 MHz
11 A C _{rss} Common-Source Reverse Transfer Capacitance			1.5			1.5	pF	f = 1 MHz
12 T g _{fs} Common-Source Forward Transconductance	120		350	120		350	μS	$V_{DG} = 10 V, I_D = 30 \mu A$
13 A g _{os} Common-Source Output Conductance			3.0			3.0	μS	
14 T e _n Equivalent Short Circuit Input Noise Voltage			20			20	nV/√Hz	f = 10 Hz
			10			10	nV/√Hz	f = 1 kHz
15 A NF Noise Figure			1.0			1.0	dB	f = 10 Hz, R _G = 10M Ω

Characteristic	U421, 4			U422, 5			U423, 6			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
16 M V _{GS1} - V _{GS2} Differential Gate-Source Voltage			10			15			25	mV	$V_{DG} = 10 V, I_D = 30 \mu A$
17 A V _{GS1} - V _{GS2} / ΔT Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	$V_{DG} = 10 V, I_D = 30 \mu A, T_A = -55^\circ C, T_B = 25^\circ C, T_C = 125^\circ C$
18 T CMRR Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	$I_D = 30 \mu A, V_{DG} = 10$ to $20 V$

NOTES:

1. Approximately doubles for every 10°C increase in T_A .

$$3. \text{ CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right] \quad \Delta V_{DD} = 10 V.$$

NNT

2. Measured at end points T_A, T_B and T_C .

4. Case lead not connected.

U421 U422 U423 U424 U425 U426

2

monolithic dual n-channel JFETs designed for . . .



Performance Curves NNT
See Section 4

BENEFITS

- High Input Impedance
 $I_G = 5 \text{ pA}$ (U427)
- High Gain $g_{fs} = 120 \text{ } \mu\text{mho}$ Minimum @
 $I_D = 30 \text{ } \mu\text{A}$
- Low Power Supply Operation
 $V_{GS(\text{off})} = 2 \text{ V}$ Maximum (U427)
- Minimum System Error and Calibration
25 mV Maximum Offset

■ **Very High Input Impedance
Differential Amplifiers**

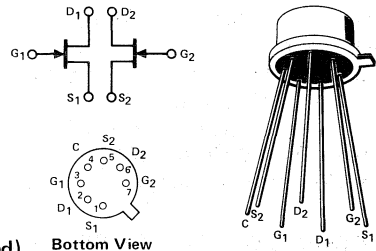
Electrometers

■ **Impedance Converters**

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	$\pm 40 \text{ V}$
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), $T_A = 25^\circ\text{C}$ (Derate $3.2 \text{ mW}/^\circ\text{C}$ to 150°C)	400 mW
Total Device Dissipation, $T_A = 25^\circ\text{C}$ (Derate $6.0 \text{ mW}/^\circ\text{C}$ to 150°C)	750 mW
Storage Temperature Range	$-65 \text{ to } +150^\circ\text{C}$

TO-78
See Section 6



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Characteristic	U427			U428			Unit	Test Conditions	
																			Min	Typ	Max	Min	Typ	Max		Min	Max
S T A T I C	BV _{GS}	Gate-Source Breakdown Voltage	-40	-60		-40	-60												V	$I_G = -1 \text{ } \mu\text{A}, V_{DS} = 0$							
	BV _{G1G2}	Gate-Gate Breakdown Voltage	± 40			± 40													V	$I_G = -1 \text{ } \mu\text{A}, I_D = 0, I_S = 0$							
	I _{GSS}	Gate Reverse Current (Note 1)			5				10										pA	$T = +25^\circ\text{C}$ $V_{GS} = -20 \text{ V}, V_{DS} = 0$							
	I _G	Gate Operating Current (Note 1)			5				10										nA	$T = +125^\circ\text{C}$ $V_{DG} = 10 \text{ V}, I_D = 30 \text{ } \mu\text{A}$							
D Y N A M I C	I _G	Gate Operating Current (Note 1)			3			5											pA	$T = +25^\circ\text{C}$							
	I _G	Gate Operating Current (Note 1)			3			5											nA	$T = +125^\circ\text{C}$							
	V _{GS(off)}	Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-3.0											V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$							
	V _{GS}	Gate Source Voltage			-1.8			-2.9											V	$V_{DG} = 10 \text{ V}, I_D = 30 \text{ } \mu\text{A}$							
	I _{DSS}	Saturation Drain Current	60		1000	60		1800											μA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$							
	g _{fs}	Common-Source Forward Transconductance	300		800	300		1500											μS	$V_{DS} = 10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ kHz}$							
	g _{os}	Common-Source Output Conductance			3.0			5.0											μS	$V_{DS} = 10 \text{ V}, V_{GS} = 0$ $f = 1 \text{ MHz}$							
	C _{iss}	Common-Source Input Capacitance			3.0			3.0											pF	$V_{DG} = 10 \text{ V}, I_D = 30 \text{ } \mu\text{A}$ $f = 1 \text{ kHz}$							
	C _{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5											pF	$f = 10 \text{ Hz}$ $f = 1 \text{ kHz}$							
	M A T C H	g _{fs}	Common-Source Forward Transconductance	120		350	120		350											μS	$f = 10 \text{ Hz}$ $f = 1 \text{ kHz}$ $R_G = 10 \text{ M}\Omega$						
g _{os}		Common-Source Output Conductance			0.5		1.0												μS								
	e _n	Equivalent Short Circuit Input Noise Voltage			20		50		20		70								nV $\sqrt{\text{Hz}}$								
	NF	Noise Figure					1.0				1.0								dB								
	V _{GS1} - V _{GS2}	Differential Gate-Source Voltage					25												mV	$V_{DG} = 10 \text{ V}, I_D = 30 \text{ } \mu\text{A}$							
	V _{GS1} - V _{GS2} ΔT	Differential Gate-Source Voltage Change With Temperature (Note 2)					40												$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10 \text{ V}, I_D = 30 \text{ } \mu\text{A}, T_A = -55^\circ\text{C}, T_B = 25^\circ\text{C}, T_C = 125^\circ\text{C}$							
	CMRR	Common Mode Rejection Ratio (Note 3)			90			90											dB	$I_D = 30 \text{ } \mu\text{A}, V_{DG} = 10 \text{ to } 20 \text{ V}$							

NOTES

1. Approximately doubles for every 10°C increase in T_A .
2. Measured at end points T_A, T_B and T_C .
3. $\text{CMRR} = 20 \log_{10} \left[\frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right]$ $\Delta V_{DD} = 10 \text{ V}$.
4. Case lead not connected.

NNT

matched dual n-channel JFETs designed for . . .



■ VHF/UHF Amplifiers

Performance Curves NZF See Section 4

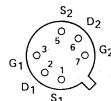
BENEFITS

- High Gain
 $g_{fs} = 4500 \mu\text{mho}$ Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

ABSOLUTE MAXIMUM RATINGS (25°C)

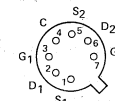
Gate-To-Gate Voltage	±50 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating	2.8 mW/°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 6

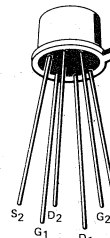
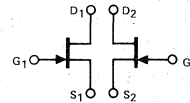


Bottom View

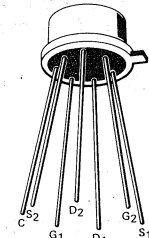
TO-78
See Section 6



Bottom View



TO-71 = U440, U441



TO-78 = U443, U444

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U440/U443			U441/U444			Unit	Test Conditions
	Min	Typ	Max	Min	Typ	Max		
1 S T A T I C I C	I_{GSS}		-500			-500	pA	$V_{DS} = 0, V_{GS} = -15 \text{ V}$
2	$V_{GS(off)}$		-6			-6	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ nA}$
3	BV_{GSS}		-25			-25		$V_{DS} = 0, I_G = -1 \mu\text{A}$
4	I_{DSS}	6	30	6		30	mA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$
5	I_G		-500			-500	pA	$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$
6 D Y N A M I C	g_{fs}	4,500	9,000	4,500		9,000	μmho	$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$
7	g_{os}		200			200		
8	C_{iss}		3.5			3.5	pF	f = 1 MHz
9	C_{rss}		0.8			0.8		
10 M A T	$ V_{GS1} - V_{GS2} $		10			20	mV	$V_{DG} = 10 \text{ V}, I_D = 5 \text{ mA}$

NOTES:

1. Approximately doubles for every 10°C increase in T_A .
2. Pulse test duration = 300 μsec ; duty cycle $\leq 3\%$.

NZF

U1897 U1897-18 U1898 U1898-18 U1899 U1899-18

2

n-channel JFETs designed for . . .



- Analog Switches
- Choppers
- Commutators

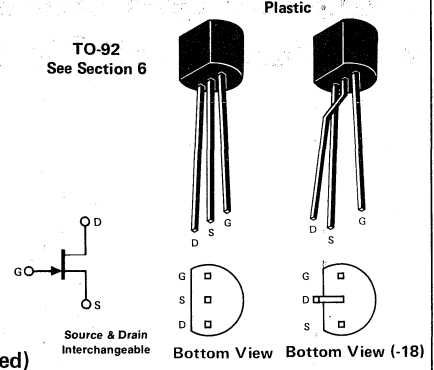
Performance Curves NC
See Section 4

BENEFITS

- Low Insertion Loss
 $r_{DS(on)} < 30 \Omega$ (U1897)
- No Error or Offset Voltage Generated by Closed Switch
Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage -40V
 Gate Current 10 mA
 Total Device Dissipation at 25°C Ambient
 (Derate 3.27 mW/°C). 360 mW
 Operating Temperature Range. -55 to 135°C
 Storage Temperature Range. -55 to 150°C
 Lead Temperature Range
 (1/16" from case for 10 seconds) 300°C



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	U1897		U1898		U1899		Unit	Test Conditions																								
	Min	Max	Min	Max	Min	Max																										
1 BV _{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1 \mu A, V_{DS} = 0$																								
2 BV _{DGO} Drain-Gate Breakdown Voltage	40		40		40		V	$I_G = -1 \mu A, I_S = 0$																								
3 BV _{SOG} Source-Gate Breakdown Voltage	40		40		40		V	$I_G = -1 \mu A, I_D = 0$																								
4 I _{GSS} Gate Reverse Current		-400		-400		-400	pA	$V_{GS} = -20 V, V_{DS} = 0$																								
5 I _{DGO} Drain-Gate Leakage Current		200		200		200	pA	$V_{DG} = 20 V, I_S = 0$																								
6 I _{SOG} Source-Gate Leakage Current		200		200		200	pA	$V_{SG} = 20 V, I_D = 0$																								
7 I _{D(off)} Drain Cutoff Current		200		200		200	nA	$V_{DS} = 20 V, V_{GS} = -12 V$ (U1897) $V_{GS} = -8 V$ (U1898) $V_{GS} = -6 V$ (U1899) $T_A = 85^\circ C$																								
8		10		10		10	nA																									
9 V _{GS(off)} Gate-Source Cutoff Voltage	-5.0	-10	-2.0	-7.0	-1.0	-5.0	V		$V_{DS} = 20 V, I_D = 1 nA$																							
10 I _{DSS} Saturation Drain Current (Note 1)	30		15		8.0		mA	$V_{DS} = 20 V, V_{GS} = 0$																								
11 V _{DS(on)} Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0, I_D = 6.6 mA$ (U1897) $I_D = 4.0 mA$ (U1898), $I_D = 2.5 mA$ (U1899)																								
12 r _{DS(on)} Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1 mA, V_{GS} = 0$																								
13 C _{DG} Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20 V, I_S = 0$																								
14 C _{SG} Source-Gate Capacitance		5		5		5		$V_{SG} = 20 V, I_D = 0$																								
15 C _{iss} Common-Source Input Capacitance		16		16		16		$V_{DS} = 20 V, V_{GS} = 0$	f = 1 MHz																							
16 C _{rss} Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5																										
17 t _{d(on)} Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions																								
18 t _r Rise Time		10		20		40																										
19 t _{off} Turn-OFF Time		40		60		80																										
								<table border="0"> <tr> <td></td> <td>U1897</td> <td>U1898</td> <td>U1899</td> </tr> <tr> <td>V_{DD}</td> <td>3 V</td> <td>3 V</td> <td>3 V</td> </tr> <tr> <td>V_{GS(on)}</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>V_{GS(off)}</td> <td>-12 V</td> <td>-8 V</td> <td>-6 V</td> </tr> <tr> <td>R_L</td> <td>430 Ω</td> <td>700 Ω</td> <td>1100 Ω</td> </tr> <tr> <td>I_{D(on)}</td> <td>6.6 mA</td> <td>4 mA</td> <td>2.5 mA</td> </tr> </table>		U1897	U1898	U1899	V _{DD}	3 V	3 V	3 V	V _{GS(on)}	0	0	0	V _{GS(off)}	-12 V	-8 V	-6 V	R _L	430 Ω	700 Ω	1100 Ω	I _{D(on)}	6.6 mA	4 mA	2.5 mA
	U1897	U1898	U1899																													
V _{DD}	3 V	3 V	3 V																													
V _{GS(on)}	0	0	0																													
V _{GS(off)}	-12 V	-8 V	-6 V																													
R _L	430 Ω	700 Ω	1100 Ω																													
I _{D(on)}	6.6 mA	4 mA	2.5 mA																													

NOTE:

1. Pulse test pulsewidth = 300 μs ; duty cycle $\leq 3\%$.

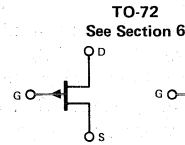
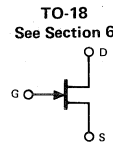
NC

voltage-controlled resistor FETs designed for . . .

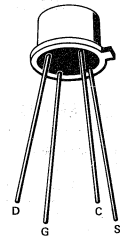


Performance Curves NC NP NT PC PE See Section 4

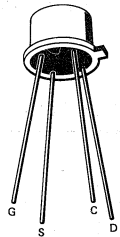
- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control



VCR2N
VCR4N



VCR3P
VCR5P



VCR7N

ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage 15 V
 Gate Current 10 mA
 Total Device Dissipation at $T_A = 25^\circ\text{C}$
 (Derate at 2.0 mW/°C to 175°C) 300 mW
 Storage Temperature Range -55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

	Characteristic	VCR2N		VCR4N		VCR7N		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
1	ST A T I C I GSS		-5		-0.2		-0.1	nA	$V_{GS} = -15\text{ V}, V_{DS} = 0$
2	BV GSS	-15		-15		-15		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$
3	VGS(off)	-3.5	-7	-3.5	-7	-2.5	-5		$I_D = 1\ \mu\text{A}, V_{DS} = 10\text{ V}$
4	rds(on)	20	60	200	600	4,000	8,000	Ω	$V_{GS} = 0, I_D = 0$ f = 1 kHz
5	CD go		7.5		3		1.5	pF	$V_{GD} = -10\text{ V}, I_S = 0$ f = 1 MHz
6	CS go		7.5		3		1.5	pF	$V_{GS} = -10\text{ V}, I_D = 0$

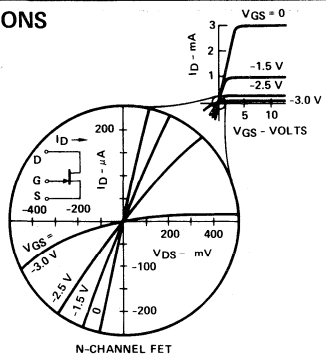
NC NP NT

P-Channel VCR FETs

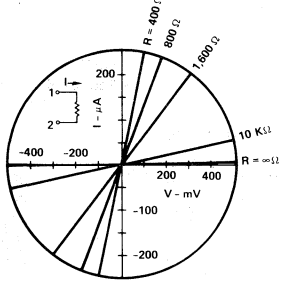
	Characteristic	VCR3P		VCR5P		Unit	Test Conditions
		Min	Max	Min	Max		
1	ST A T I C I GSS		20		10	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0$
2	BV GSS	15		15		V	$I_G = 1\ \mu\text{A}, V_{DS} = 0$
3	VGS(off)	3.5	7	3.5	7		$I_D = -1\ \mu\text{A}, V_{DS} = -10\text{ V}$
4	rds(on)	70	200	300	900	Ω	$V_{GS} = 0, I_D = 0$ f = 1 kHz
5	CD go		6		3	pF	$V_{GD} = 10\text{ V}, I_S = 0$ f = 1 MHz
6	CS go		6		3	pF	$V_{GS} = 10\text{ V}, I_D = 0$

PE PC

APPLICATIONS



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$ Figure 1



FOUR FIXED RESISTORS V-I Characteristic of Four Fixed Resistors Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around $V_{DS} = 0$, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{DS} occurs when $V_{GS} = 0$ and, as V_{GS} approaches the pinch-off voltage, r_{DS} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and $V_{GS} = \text{constant}$, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around $V_{DS} = 0$. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds} , it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at $I_D/I_{DSS} = 0.001$. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as

V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{DS} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical $0.7\%/^{\circ}\text{C}$ temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical $0.3\%/^{\circ}\text{C}$ t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

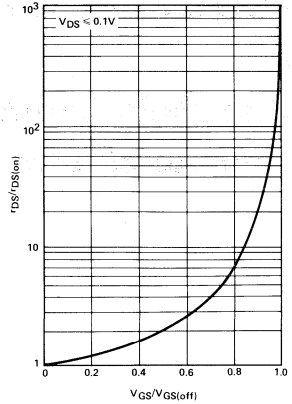


Fig. 3

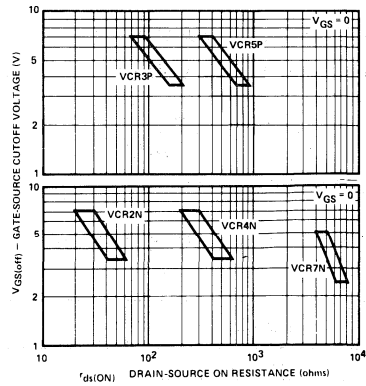


Fig. 4

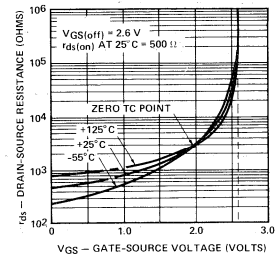


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

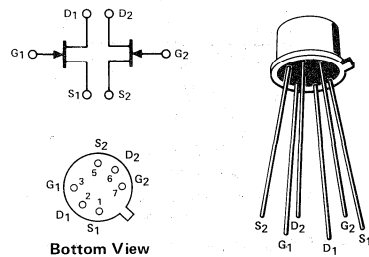
* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

voltage-controlled resistor FETs designed for . . .



- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

TO-71
See Section 6



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage 25 V
 Gate Current 10 mA
 Total Device Dissipation at $T_A = 25^\circ\text{C}$
 (Derate at $2.0\text{ mW}/^\circ\text{C}$ to 175°C) 300 mW
 Storage Temperature Range -55 to $+175^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic	VCR11N		Unit	Test Conditions	
	Min	Max			
1 I_{GSS} Gate Reverse Current		-0.2	nA	$V_{GS} = -15\text{ V}, V_{DS} = 0$	
2 BV_{GSS} Gate-Source Breakdown Voltage	-25		V	$I_G = -1\ \mu\text{A}, V_{DS} = 0$	
3 $V_{GS(off)}$ Gate-Source Cutoff Voltage	-8	-12		$I_D = 1\ \mu\text{A}, V_{DS} = 10\text{ V}$	
4 $r_{ds(on)}$ Drain Source ON Resistance	100	200	Ω	$V_{GS} = 0, I_D = 0$	$f = 1\text{ kHz}$
5 C_{dgo} Drain-Gate Capacitance		8	pF	$V_{GD} = -10\text{ V}, I_S = 0$	$f = 1\text{ MHz}$
6 C_{sgo} Source-Gate Capacitance		8		$V_{GS} = -10\text{ V}, I_D = 0$	
7 $r_{DS}^{min} / r_{DS}^{max}$.95	1	Ω	$V_{DS} = 100\text{ mV}$	$r_{DS1} = 200\ \Omega$
	.95	1		$V_{GS1} = V_{GS2}$	$r_{DS1} = 2\text{ k}\Omega$

Note
 1 V_{GS1} + Control Voltage necessary to force r_{DS} to $200\ \Omega$ or $2\text{ k}\Omega$.

NSH*
 *Contact factory for geometry information.

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

Tips on Selecting the Right FET for Your Application

The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 3-4, "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 3-6, "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to "Geometry Characteristics," section 4 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets," section 2 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications," pages 3-9 through 3-18 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

Siliconix FET Application Selection Preferences

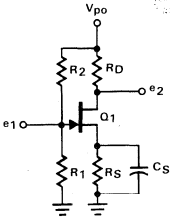
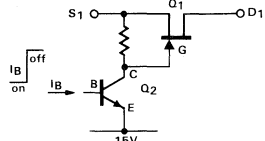
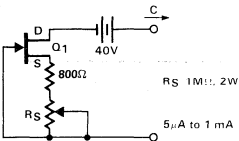
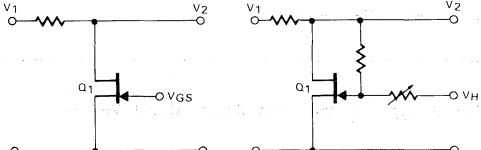
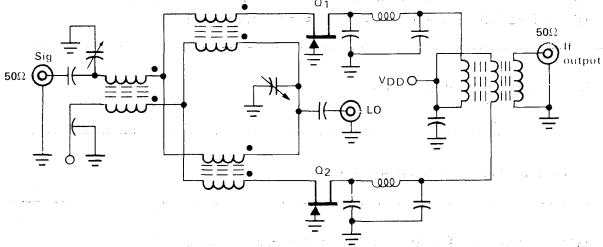
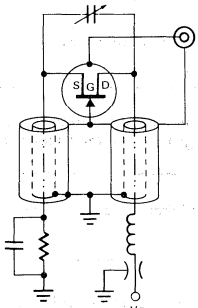
Additional Information

POPULAR PRODUCT TYPES	Additional Information																		
	2N4117-9, PN4117A-19A	2N4117-20, A	2N4338-41, J201-4	J304-5	2N4416, 2N5454-6	PN4416	2N3821-2, 2N4221-2	2N5457-9	2N4867-9 A	J230-2	U308-10, J308-10	J300, J210-2	J105-7, U290-1	2N5432-4	J108-10	2N4856-81, 2N4391-3	J111-13, PN4391-3	3N163, 4, MFE823	U421-U428
PROCESS DESIGNATION	NT	NP	NH	NRL	NS	NZA	NZF	NVA	NIP	NC	MRA	NNT							
Low Current Amplifier	P	S		S	S						P	P							
Low Freq Amplifier ≤ 100 Hz		S		S	S						P								
High Freq Amplifier > 100 MHz			P			P	P												
HF ≥ 400 MHz Prime						P	S												
General Purpose Amplifier		P	P	P						P									
Low Noise Amp (10 Hz e _n)		P	S	S	S				S	P									
Low Noise Amp > 50 MHz			P	S		P	P												
High Frequency Mixer			P			P	P												
Dual Diff Pair																			P
AGC Amplifier			P	P			P												
Electrometer Preamp	P																		P
Microvolt Amplifier	P																		P
Low Leakage Diode	P	S																	
Low Leakage Dual Diode																			P
Smoke Detector Input	P															P			
Battery Operated Amp < 1.5V	P	P																	P
Diff/Single Ended Inp. Stag.																			P
High Slew Rate Diff Amp																			
Active Filter		S	P	P															
Oscillator		S	P	P		P	P												
Voltage Controlled Resistor		S	P	P							P								
Hybrid Chips	P	P	P	P							P								P
Analog/Digital Switch			S					P	P		P	S							
Multiplexing			P	S				S	S	P	P								
Choppers								P	P	P									
Reed Relay Replacement								P	P										
Sub pA Dual Diff Pair																			P
Sample Hold			P	S						P		S							
Buffer Interface to CMOS																			
Matched Switch																			
Current Limiter										P									
Current Source	S	S		LV															LV
High Voltage Protection Diode																			

P = PRIME CHOICE
 S = SECONDARY (ALTERNATIVE) CHOICE
 LV = LIMITED VALUE

How to Choose the Correct FET for Your Application

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters
AMPLIFIER	Audio Buffer Differential High Input Impedance High Frequency FET Input Op Amp Low Distortion Low Supply Voltage Low Noise Preamplifier Video	Low noise (\bar{e}_n), g_{fs}/g_{os} Low I_G , high g_{fs} Good matching V_{GS} , g_{fs} , I_{DSS} , I_G Very low I_G (eg., MOSFET) High g_{fs}/C_{iss} ratio, NF, RF parameters Good matching V_{GS} , g_{fs} , I_{DSS} , I_G High $V_{GS(off)}$ compared to signal amplitude Low $V_{GS(off)}$ Low e_n , i_n , low 1/f noise, low NF Operate near I_{DZO} , high g_{fs}/I_D ratio High g_{fs}/C_{iss} ratio, NF	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS} @ I_D = \text{const}$	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times
SWITCHES	Analog Gates Choppers Commutators Digital Integrator Reset Sample and Hold	Fast switching time $r_{DS}/I_{D(off)}$ switching efficiency Low C_{rSS} Fast switching time Very low $R_{DS(on)}$, High I_{DSS} Low C_{rSS}	$R_{DS(on)}$ vs Capacitance	g_{fs} g_{os} $I_{DSS \text{ max}}$
CONSTANT CURRENT SOURCE	Current Limiting Reference Current Source Biasing	Low g_{OSS} , low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs BV_{GSS}	g_{fs} , $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance
VOLTAGE CONTROLLED RESISTORS	Gain Control Amplitude Stability Attenuators	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs} , BV_{GSS} , I_{DSS}
MIXERS	VHF UHF Double Balanced	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rSS} Matching characteristics		$r_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$
OSCILLATORS	Class A Class C	Good g_{fs} at operating frequency Low C_{iss} for VHF operation	g_{fs} vs Capacitance	

Basic Circuit*	Preferred Parts																																																																				
 <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>V_{DD} (V)</th> <th>R_S Ω</th> <th>R₁ MΩ</th> <th>R₂ MΩ</th> <th>C_S nF</th> <th>I_{DD} mA</th> <th>R_D Ω</th> <th>g₀ (V)</th> <th>A_V</th> </tr> </thead> <tbody> <tr> <td rowspan="3">20</td> <td>2K</td> <td>4.7</td> <td>11</td> <td>100</td> <td>5</td> <td>1K</td> <td>1.5</td> <td>8-11</td> </tr> <tr> <td>330</td> <td>1</td> <td>∞</td> <td>100</td> <td>8</td> <td>820</td> <td>1.5</td> <td>9</td> </tr> <tr> <td>330</td> <td>1</td> <td>∞</td> <td>0</td> <td>8</td> <td>820</td> <td>3</td> <td>1.9</td> </tr> <tr> <td rowspan="3">30</td> <td>2K</td> <td>4.7</td> <td>11</td> <td>100</td> <td>6</td> <td>2.7K</td> <td>5</td> <td>18-24</td> </tr> <tr> <td>330</td> <td>1</td> <td>∞</td> <td>100</td> <td>8</td> <td>1.5K</td> <td>2.5</td> <td>15</td> </tr> <tr> <td>330</td> <td>1</td> <td>∞</td> <td>0</td> <td>8</td> <td>1.5K</td> <td>5.5</td> <td>3.3</td> </tr> <tr> <td>V_{DD} = 15 V_{SS} = -15</td> <td>4.7K</td> <td>1</td> <td colspan="2">Source Follower</td> <td>5</td> <td>0</td> <td>11</td> <td>0.97</td> </tr> </tbody> </table> <p style="text-align: center;">JFET Voltage Amplifier Stage Application Note: TA70-2</p>	V _{DD} (V)	R _S Ω	R ₁ MΩ	R ₂ MΩ	C _S nF	I _{DD} mA	R _D Ω	g ₀ (V)	A _V	20	2K	4.7	11	100	5	1K	1.5	8-11	330	1	∞	100	8	820	1.5	9	330	1	∞	0	8	820	3	1.9	30	2K	4.7	11	100	6	2.7K	5	18-24	330	1	∞	100	8	1.5K	2.5	15	330	1	∞	0	8	1.5K	5.5	3.3	V _{DD} = 15 V _{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97	<p>J111-3 PN4091-3 2N4094-3 2N4856-61 2N4339-40 2N4867-69 J230-32 J202-4 J308-10 U308-10</p>
V _{DD} (V)	R _S Ω	R ₁ MΩ	R ₂ MΩ	C _S nF	I _{DD} mA	R _D Ω	g ₀ (V)	A _V																																																													
20	2K	4.7	11	100	5	1K	1.5	8-11																																																													
	330	1	∞	100	8	820	1.5	9																																																													
	330	1	∞	0	8	820	3	1.9																																																													
30	2K	4.7	11	100	6	2.7K	5	18-24																																																													
	330	1	∞	100	8	1.5K	2.5	15																																																													
	330	1	∞	0	8	1.5K	5.5	3.3																																																													
V _{DD} = 15 V _{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97																																																													
 <p style="text-align: center;">Shunt-Resistor Analog Switch Application Note: AN73-5</p>	<p>2N4091-3 2N4391-3 PN4091-3 PN4391-3 J108-10 J105-7 U290-1 2N5432-4</p>																																																																				
 <p style="text-align: center;">Equivalent Circuit of a JFET Current Limiter Application Note: DI71-1</p>	<p>CRR Series J501-11 J552-7 Any J-FET</p>																																																																				
 <p style="text-align: center;">Distortion Free Voltage Controlled Attenuator (VCR) Application Note: AN73-1</p>	<p>VCR Series Any J-FET</p>																																																																				
 <p style="text-align: center;">Single-Balanced VHF Balanced Mixer Application Note: AN72-1</p>	<p>U430-1 U440-1-3-4 2N5911-12 U308-10 J308-10 2N4416</p>																																																																				
 <p style="text-align: center;">UHF Transmission Line Oscillator Application Note: DI73-2</p>	<p>2N4416 PN4416 U308-10 J308-10</p>																																																																				

*for further details see Application Notes, Index 5

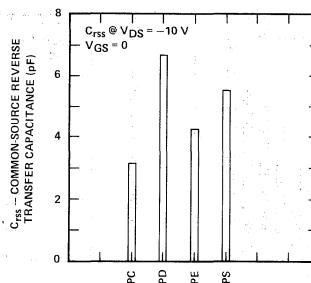
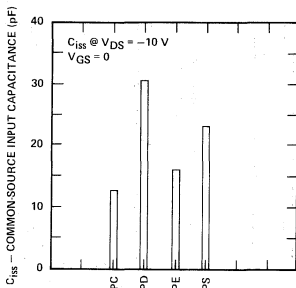
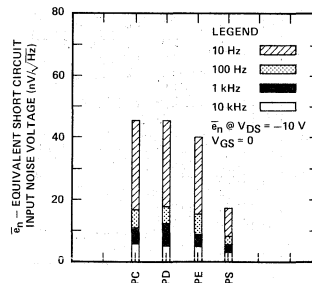
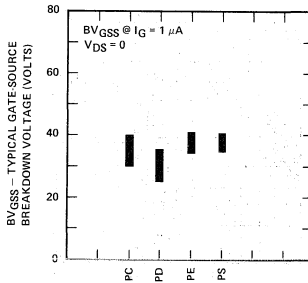
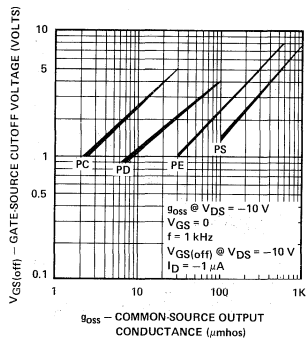
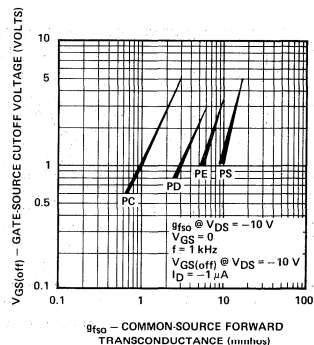
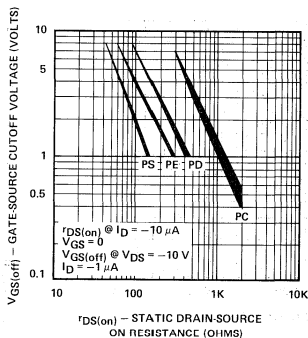
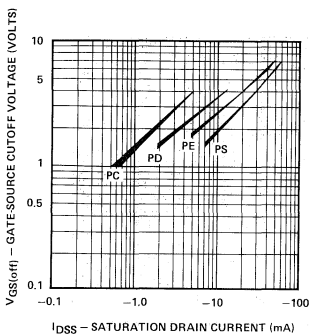
JFET Geometry Selector Guide

USEFUL JFET INFORMATION

C_{iss}	$= C_{qs} + C_{gd}$	Input Capacitance
C_{oss}	$= C_{ds} + C_{gs} + C_{bd}$	Output Capacitance
C_{rss}	$= C_{qd}$	Reverse Feedback Capacitance
I_{DZ}	$= I_{DSS} \left(\frac{0.63}{V_{GS(off)}} \right)^2$	Variation of $I_{(zero\ tc)}$ with Gate Source Cutoff Voltage
g_{fso}	$= K \frac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage (K = 1.5 to 2.5; typically = 2 for N-channel junction FET)
g_{fs}	$= g_{fso} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)$	Variation of g_{fs} with gate bias
g_{fs}	$= g_{fso} \sqrt{I_D / I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	$= \frac{2 I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	$\approx V_{GS(off)} \left(\frac{I_D}{I_{DSS}} \right)^{1/2}$	Drain voltage at which drain current saturates
r_{DS}	$\approx \frac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region
r_{DS}	$\approx \frac{ V_{GS(off)} ^2}{K I_{DSS} [V_{GS(off)} - V_{GS}]}$	K = 1.5 to 2.5 Variation of drain resistance in the triode region
I_D	$= I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

JFET Geometry Selector Guide (Cont'd)

P-Channel JFETs



Product Specifications

Product Specifications

3

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
2N4117	N	72	0.01	0.03	1.8	40	0.03	0.09	70	210	3	—	—	NT	LOW LEAKAGE	
2N4117A	N	72	0.001	0.03	1.8	40	0.03	0.09	70	210	3	—	—	NT	LOW LEAKAGE	
2N4118	N	72	0.01	0.08	3.0	40	0.08	0.24	80	250	3	—	—	NT	LOW LEAKAGE	
2N4118A	N	72	0.001	0.08	3.0	40	0.08	0.24	90	250	3	—	—	NT	LOW LEAKAGE	
2N4119	N	72	0.01	0.2	6.0	40	0.2	0.6	100	330	3	—	—	NT	LOW LEAKAGE	
2N4119A	N	72	0.001	0.2	6.0	40	0.2	0.6	100	330	3	—	—	NT	LOW LEAKAGE	
PN4117	N	92	0.01	0.03	—	—	0.03	0.09	70	210	—	—	—	NT	LOW LEAKAGE	
PN4117A	N	92	0.001	0.03	—	—	0.03	0.09	70	210	—	—	—	NT	LOW LEAKAGE	
PN4118	N	92	0.01	0.08	—	—	0.08	0.24	80	250	—	—	—	NT	LOW LEAKAGE	
PN4118A	N	92	0.001	0.08	—	—	0.08	0.24	80	250	—	—	—	NT	LOW LEAKAGE	
PN4119	N	92	0.01	0.2	—	—	0.2	0.6	100	330	—	—	—	NT	LOW LEAKAGE	
PN4119A	N	92	0.001	0.2	—	—	0.2	0.6	100	330	—	—	—	NT	LOW LEAKAGE	
PN4120	N	92	—	—	—	—	—	—	—	—	—	—	—	NT	LOW LEAKAGE	
FN4117	N	72	0.005	0.03	—	—	0.03	0.09	70	210	3	—	—	NT	LOW LEAKAGE	
FN4117A	N	72	0.001	0.03	—	—	0.03	0.09	70	210	3	—	—	NT	LOW LEAKAGE	
FN4118	N	72	0.005	0.08	—	—	0.08	0.24	80	250	3	—	—	NT	LOW LEAKAGE	
FN4118A	N	72	0.001	0.08	—	—	0.08	0.24	80	250	3	—	—	NT	LOW LEAKAGE	
FN4119	N	72	0.005	0.2	—	—	0.2	0.6	100	330	3	—	—	NT	LOW LEAKAGE	
FN4119A	N	72	0.001	0.2	—	—	0.2	0.6	100	330	3	—	—	NT	LOW LEAKAGE	
FN4392	N	18	0.1	25	—	—	25	100	—	—	—	—	—	NC	LOW LEAKAGE	
FN4393	N	18	0.1	5.0	—	—	5.0	60	—	—	—	—	—	NC	LOW LEAKAGE	
2N4220A	N	72	0.1	0.5	4.0	30	0.5	3.0	1000	4000	6	2.5	1M	NRL	LOW NOISE	
2N4221A	N	72	0.1	2.0	6.0	30	2.0	6.0	2000	5000	6	2.5	1M	NRL	LOW NOISE	
2N4222	N	72	0.1	5.0	8.0	30	5.0	15	2500	6000	6	2.5	1M	NRL	LOW NOISE	
2N4338	N	18	0.1	0.2	1.0	50	0.2	0.6	600	1800	7	1*0	1M	NP	LOW NOISE	
2N4339	N	18	0.1	0.5	1.8	50	0.5	1.5	800	2400	7	1.0	1M	NP	LOW NOISE	
2N4340	N	18	0.1	1.2	3.0	50	1.2	3.6	1300	3000	7	1.0	1M	NP	LOW NOISE	
2N4341	N	18	0.1	3.0	6.0	50	3.0	9.0	2000	4000	7	1.0	1M	NP	LOW NOISE	
2N4867	N	72	0.25	0.4	2.0	40	0.4	1.2	700	2000	25	20	—	NS or NP	LOW NOISE	
2N4867A	N	72	0.25	0.4	2.0	40	0.4	1.2	700	2000	25	10	—	NS or NP	LOW NOISE	
2N4868	N	72	0.25	1.0	3.0	40	1.0	3.0	1000	3000	25	20	—	NS or NP	LOW NOISE	
2N4868A	N	72	0.25	1.0	3.0	40	1.0	3.0	1000	3000	25	10	—	NS or NP	LOW NOISE	
2N4869	N	72	0.25	2.5	5.0	40	2.5	7.5	1300	4000	25	20	—	NS or NP	LOW NOISE	
2N4869A	N	72	0.25	2.5	5.0	40	2.5	7.5	1300	4000	25	10	—	NS or NP	LOW NOISE	
2N4869B	N	72	0.25	0.7	3.0	40	0.7	3.0	1000	2500	—	30	—	NS or NP	LOW NOISE	
J230	N	92	0.25	0.7	3.0	40	0.7	3.0	1000	2500	—	30	—	NS or NP	LOW NOISE	
J230-18	N	92	0.25	2.0	5.0	40	2.0	6.0	1500	3000	—	30	—	NS or NP	LOW NOISE	
J231	N	92	0.25	5.0	5.0	40	5.0	6.0	1500	3000	—	30	—	NS or NP	LOW NOISE	
J231-18	N	92	0.25	2.0	5.0	40	2.0	6.0	1500	3000	—	30	—	NS or NP	LOW NOISE	
J232	N	92	0.25	5.0	6.0	40	5.0	10	2500	4000	—	30	—	NS or NP	LOW NOISE	

Product Specifications

Product Specifications (Cont'd)

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
J232-18	N	92	0.25	—	6.0	40	5.0	10	2500	4000	—	30	—	NS		
J270-18	P	92	0.2	—	2.0	30	2.0	15	6000	15000	—	—	—	PS		
2N3819	N	92	2.0	—	8.0	25	2.0	20	2000	6500	8.0	—	—	NRL		
2N3823	N	72	0.5	—	8.0	30	4.0	20	3500	6500	6	2.5	1K	NRL		
2N4223	N	72	0.25	—	8.0	30	3.0	18	3000	7000	6	5.0	1K	NRL		
2N4224	N	72	0.5	—	8.0	30	2.0	20	2000	7500	6	—	—	NRL		
2N4416	N	72	0.1	—	6.0	30	5.0	15	4500	7500	4	2.0	1K	NH		
2N4416A	N	72	0.1	—	6.0	35	5.0	15	4500	7500	4	2.0	1K	NH		
2N5078	N	72	0.25	—	8.0	30	4.0	25	4500	10000	6	3.0	1K	—		
2N5484	N	92	1.0	—	3.0	25	1.0	5.0	3000	6000	5	3.0	1K	NH		
2N5485	N	92	1.0	—	4.0	25	1.0	4.0	3500	7000	5	2.0	1K	NH		
2N5486	N	92	1.0	—	6.0	25	8.0	20	4000	8000	5	2.0	1K	NH		
2N5668	N	92	2.0	—	4.0	25	1.0	5.0	1500	6500	7	2.5	1K	NH		
2N5669	N	92	2.0	—	6.0	25	4.0	10	2000	6500	7	2.5	1K	NH		
2N5670	N	92	2.0	—	8.0	25	8.0	20	3000	7500	7.0	2.5	1K	NH		
J210	N	92	0.1	—	3.0	25	2.0	15	4000	12000	—	—	—	NZF		
J211	N	92	0.1	—	4.5	20	7.0	20	7000	12000	—	—	—	NZF		
J212	N	92	0.1	—	6.0	25	15	40	7000	12000	—	—	—	NZF		
J270	P	92	0.2	—	2.0	30	2.0	15	6000	15000	—	—	—	PS		
J271	P	92	0.2	—	4.5	30	6.0	50	8000	18000	—	—	—	PS		
J300	N	92	0.5	—	6.0	25	6.0	30	4500	9000	5.5	—	—	NZF		
J304	N	92	0.1	—	6.0	30	5.0	15	4500	7500	—	—	—	NH		
J305	N	92	0.1	—	3.0	30	1.0	8.0	3000	—	—	—	—	NH		
J308	N	92	1.0	—	6.5	25	12	60	8000	20000	—	—	—	NZA		
J309	N	92	1.0	—	4.0	25	12	30	10000	20000	7.5	—	—	NZA		
J310	N	92	1.0	—	6.5	25	24	60	8000	18000	7.5	—	—	NZA		
PN4416	N	92	1.0	—	6.5	25	5.0	15	4500	7500	4.0	2.0	1K	NH		
MPF102	N	92	2.0	—	7.5	25	2.0	20	2000	7500	7.0	—	—	NH		
MPF108	N	92	1.0	—	8.0	25	1.5	24	2000	7500	6.5	2.5	1M	NH		
MPF112	N	92	100	—	10	25	1.0	25	1000	7500	—	—	—	NH		
U308	N	52	0.15	—	6.0	25	12	60	10000	20000	7.5	—	—	NZA		
U309	N	52	0.15	—	4.0	25	12	30	10000	20000	7.5	—	—	NZA		
U310	N	52	0.15	—	6.0	25	24	60	10000	18000	7.5	—	—	NZA		
U311	N	72	0.15	—	6.0	25	20	60	10000	20000	7.5	—	—	NZA		
U312	N	52	0.1	—	6.0	25	10	30	6000	10000	5.0	—	—	NZF		

Product Specifications (Cont'd)

Product Specifications

3

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
U1837	N	92	0.25	—	8.0	30	4.0	25	4500	10000	6.0	3.0	1K	NH	RF AMP	
U1837-18	N	92	0.25	—	8.0	30	4.0	25	4500	10000	6.0	2.0	1K	NH	RF AMP	
2N3824	N	72	0.1	0.1	8.0	50	—	—	—	—	6.0	—	—	NRL	SWITCHES & CHOPPERS	
2N3966	N	72	0.1	1.0	6.0	30	2.0	—	—	—	6.0	—	—	NH	SWITCHES & CHOPPERS	
2N3970	N	18	0.25	0.25	10	40	50	150	—	—	25	—	—	NC	SWITCHES & CHOPPERS	
2N3971	N	18	0.25	0.25	5.0	40	25	75	—	—	25	—	—	NC	SWITCHES & CHOPPERS	
2N3972	N	18	0.25	0.25	3.0	40	5.0	30	—	—	25	—	—	NC	SWITCHES & CHOPPERS	
2N4091	N	18	0.2	0.2	10	40	30	—	—	—	16	—	—	NC	SWITCHES & CHOPPERS	
2N4092	N	18	0.2	0.2	7.0	40	15	—	—	—	16	—	—	NC	SWITCHES & CHOPPERS	
2N4093	N	18	0.2	0.2	5.0	40	8.0	—	—	—	16	—	—	NC	SWITCHES & CHOPPERS	
2N4391	N	18	0.1	0.1	10	40	50	150	—	—	14	—	—	NC	SWITCHES & CHOPPERS	
2N4392*	N	18	0.1	0.1	5.0	40	25	75	—	—	14	—	—	NC	SWITCHES & CHOPPERS	
2N4393*	N	18	0.1	0.1	3.0	40	5.0	30	—	—	14	—	—	NC	SWITCHES & CHOPPERS	
2N4856	N	18	0.25	0.25	10	40	50	—	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4856A	N	18	0.25	0.25	10	40	50	—	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4857	N	18	0.25	0.25	6.0	40	20	100	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4857A	N	18	0.25	0.25	6.0	40	20	100	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4858	N	18	0.25	0.25	4.0	40	8.0	80	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4858A	N	18	0.25	0.25	4.0	40	8.0	80	—	—	10	—	—	NC	SWITCHES & CHOPPERS	
2N4859	N	18	0.25	0.25	10	30	50	—	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4859A	N	18	0.25	0.25	10	30	50	—	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4860	N	18	0.25	0.25	6.0	30	20	100	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4860A	N	18	0.25	0.25	6.0	30	20	100	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4861	N	18	0.25	0.25	4.0	30	8.0	80	—	—	18	—	—	NC	SWITCHES & CHOPPERS	
2N4861A	N	18	0.25	0.25	4.0	30	8.0	80	—	—	10	—	—	NC	SWITCHES & CHOPPERS	
2N5018	P	18	2.0	10.0	10	30	10	—	—	—	45	—	—	PS	SWITCHES & CHOPPERS	
2N5019	P	18	2.0	10.0	5.0	30	5.0	—	—	—	45	—	—	PS	SWITCHES & CHOPPERS	
2N5114	P	18	0.5	0.5	10	30	30	90	—	—	25	—	—	PS	SWITCHES & CHOPPERS	
2N5115	P	18	0.5	0.5	6.0	30	15	60	—	—	25	—	—	PS	SWITCHES & CHOPPERS	
2N5116	P	18	0.5	0.5	4.0	30	150	25	—	—	30	—	—	PS	SWITCHES & CHOPPERS	
2N5432	N	52	0.2	0.2	10	25	100	—	—	—	30	—	—	NIP	SWITCHES & CHOPPERS	
2N5433	N	52	0.2	0.2	9.0	25	100	—	—	—	30	—	—	NIP	SWITCHES & CHOPPERS	
2N5434	N	52	0.2	0.2	4.0	25	30	—	—	—	10	—	—	NC	SWITCHES & CHOPPERS	
2N5638	N	92	1.0	1.0	12	30	50	—	—	—	10	—	—	NC	SWITCHES & CHOPPERS	
2N5639	N	92	1.0	1.0	8.0	30	25	—	—	—	10	—	—	NC	SWITCHES & CHOPPERS	

*FN4392 and FN4393 available

Product Specifications

Product Specifications (Cont'd)

N & P-Channel Single JFETs																
PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate	Chnl Ω, Max.		
2N5640	N	92	1.0	1.0	6.0	30	5.0	-	-	-	10	-	-	100	NC	
2N5653	N	92	1.0	1.0	12	30	40	-	-	-	10	-	-	50	NC	
2N5654	N	92	1.0	1.0	8.0	30	15	-	-	-	10	-	-	100	NC	
J105	N	92	3.0	3.0	10.0	25	500	-	-	-	-	-	-	3.0	NVA	
J105-18	N	92	3.0	3.0	10.0	25	500	-	-	-	-	-	-	3.0	NVA	
J106	N	92	3.0	3.0	6.0	25	200	-	-	-	-	-	-	6.0	NVA	
J106-18	N	92	3.0	3.0	6.0	25	200	-	-	-	-	-	-	6.0	NVA	
J107	N	92	3.0	3.0	4.5	25	100	-	-	-	-	-	-	8.0	NVA	
J107-18	N	92	3.0	3.0	4.5	25	100	-	-	-	-	-	-	8.0	NVA	
J108	N	92	3.0	3.0	10	25	80	-	-	-	-	-	-	8.0	NIP	
J108-18	N	92	3.0	3.0	10	25	80	-	-	-	-	-	-	8.0	NIP	
J109	N	92	3.0	3.0	6.0	25	40	-	-	-	-	-	-	12	NIP	
J109-18	N	92	3.0	3.0	6.0	25	40	-	-	-	-	-	-	12	NIP	
J110	N	92	3.0	3.0	4.0	25	10	-	-	-	-	-	-	18	NIP	
J110-18	N	92	3.0	3.0	4.0	25	10	-	-	-	-	-	-	18	NIP	
J111	N	92	1.0	1.0	10	35	20	-	-	-	-	-	-	30	NC	
J111-18	N	92	1.0	1.0	10	35	20	-	-	-	-	-	-	30	NC	
J112	N	92	1.0	1.0	5.0	35	5.0	-	-	-	-	-	-	50	NC	
J112-18	N	92	1.0	1.0	5.0	35	5.0	-	-	-	-	-	-	50	NC	
J113	N	92	1.0	1.0	3.0	35	2.0	-	-	-	-	-	-	100	NC	
J113-18	N	92	1.0	1.0	3.0	35	2.0	-	-	-	-	-	-	100	NC	
J174	P	92	1.0	1.0	10	30	20	100	-	-	-	-	-	85	PS	
J174-18	P	92	1.0	1.0	10	30	20	100	-	-	-	-	-	85	PS	
J175	P	92	1.0	1.0	6.0	30	7.0	60	-	-	-	-	-	125	PS	
J175-18	P	92	1.0	1.0	6.0	30	7.0	60	-	-	-	-	-	125	PS	
J176	P	92	1.0	1.0	4.0	30	2.0	25	-	-	-	-	-	250	PS	
J176-18	P	92	1.0	1.0	4.0	30	2.0	25	-	-	-	-	-	250	PS	
J177	P	92	1.0	1.0	2.25	30	1.5	20	-	-	-	-	-	300	PS	
J177-18	P	92	1.0	1.0	2.25	30	1.5	20	-	-	-	-	-	300	PS	
PN4391	N	92	1.0	1.0	10	40	50	150	-	-	-	-	-	30	NC	
PN4391-18	N	92	1.0	1.0	10	40	50	150	-	-	-	-	-	30	NC	
PN4392	N	92	1.0	1.0	5.0	40	25	100	-	-	-	-	-	60	NC	
PN4392-18	N	92	1.0	1.0	5.0	40	25	100	-	-	-	-	-	60	NC	
PN4393	N	92	1.0	1.0	3.0	40	5.0	60	-	-	-	-	-	100	NC	
PN4393-18	N	92	1.0	1.0	3.0	40	5.0	60	-	-	-	-	-	100	NC	
P1086	P	92	2.0	2.0	10	30	10	45	-	-	-	-	-	75	PS	
P1086-18	P	92	2.0	2.0	10	30	10	45	-	-	-	-	-	75	PS	

Product Specifications (Cont'd)

Product Specifications

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 4)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.		
P1087	P	92	2.0	10.0	5.0	30	5.0	—	—	—	45	—	—	PS	PS	
P1087-18	P	92	2.0	10.0	5.0	30	5.0	—	—	—	45	—	—	PS	PS	
SD210	N	72	100	100	2.0	30	10	—	—	—	3.5	—	—	DMCB-B	DMCB-B	
SD211	N	72	100	100	2.0	30	10	—	—	—	3.5	—	—	DMCB-A	DMCB-A	
SD212	N	72	100	100	2.0	10	10	—	—	—	3.5	—	—	DMCB-B	DMCB-B	
SD213	N	72	100	100	2.0	10	10	—	—	—	3.5	—	—	DMCB-A	DMCB-A	
SD214	N	72	100	100	2.0	20	10	—	—	—	3.5	—	—	DMCB-B	DMCB-B	
SD215	N	72	100	100	2.0	20	10	—	—	—	3.5	—	—	DMCB-A	DMCB-A	
U200	N	18	1.0	1.0	3.0	30	3.0	—	—	—	30	—	—	NC	NC	
U201	N	18	1.0	1.0	5.0	30	15	—	—	—	30	—	—	NC	NC	
U202	N	18	1.0	1.0	10	30	30	—	—	—	30	—	—	NC	NC	
U290	N	52	1.0	1.0	10	30	500	—	—	—	60	—	—	NVA	NVA	
U291	N	52	1.0	1.0	4.5	30	200	—	—	—	60	—	—	NVA	NVA	
U304	P	18	0.5	0.5	10	30	30	—	—	—	27	—	—	PS	PS	
U305	P	18	0.5	0.5	6.0	30	15	—	—	—	27	—	—	PS	PS	
U306	P	18	0.5	0.5	4.0	30	5.0	—	—	—	27	—	—	PS	PS	
U1897	N	92	0.4	0.2	10	40	30	—	—	—	16	—	—	NC	NC	
U1897-18	N	92	0.4	0.2	10	40	30	—	—	—	16	—	—	NC	NC	
U1898	N	92	0.4	0.2	7.0	40	15	—	—	—	16	—	—	NC	NC	
U1898-18	N	92	0.4	0.2	7.0	40	15	—	—	—	16	—	—	NC	NC	
U1899	N	92	0.4	0.2	5.0	40	8.0	—	—	—	16	—	—	NC	NC	
U1899-18	N	92	0.4	0.2	5.0	40	8.0	—	—	—	16	—	—	NC	NC	
2N2608	P	18	10	—	4.0	30	0.9	—	—	—	17	—	—	PC	PC	
2N2609	P	18	30	—	4.0	30	2500	—	—	—	30	—	—	PD	PD	
2N2843	P	18	10	—	1.7	30	0.2	—	—	—	17	—	—	PC	PC	
2N2844	P	18	30	—	1.7	30	0.44	—	—	—	30	—	—	PD	PD	
2N3329	P	72	10	10	5.0	20	1.0	—	—	—	20	—	—	PC	PC	
2N3330	P	72	10	10	6.0	20	2.0	—	—	—	20	—	—	PC	PC	
2N3331	P	72	10	10	8.0	20	5.0	—	—	—	20	—	—	PC	PC	
2N3332	P	72	10	10	6.0	20	1.0	—	—	—	20	—	—	PC	PC	
2N3368	N	18	5.0	—	11.5	40	2.0	—	—	—	20	—	—	NP	NP	
2N3369	N	18	5.0	—	6.5	40	0.5	—	—	—	20	—	—	NP	NP	
2N3370	N	18	5.0	—	3.2	40	0.1	—	—	—	20	—	—	NP	NP	
2N3382	P	72	15	—	5.0	30	3.0	—	—	—	—	—	—	PE	PE	
2N3384	P	72	15	—	5.0	30	15.0	—	—	—	—	—	—	PE	PE	
2N3386	P	72	15	—	9.5	30	15.0	—	—	—	—	—	—	PE	PE	

Product Specifications (Cont'd)

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD		OUTPUT CONDUCTANCE g _{os} (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
						Min.	Max.	Min.	Max.			Static Match (mV, Max.)	Temp Tracking μV/°C			
2N5196	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	5.0	5.0	50	NP-D	
2N5197	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	10	10	50	NP-D	
2N5198	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	20	20	50	NP-D	
2N5199	N	71	0.025	4.0	50	0.7	7.0	1000	—	6.0	20	15	40	50	NP-D	
2N5545	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	5.0	10	25	NP-D	
2N5546	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	10	20	25	NP-D	
2N5547	N	71	0.1	4.5	50	0.5	8.0	1500	—	6.0	200	15	40	25	NP-D	
2N5902	N	78	0.005	4.5	40	0.03	0.5	70	—	3.0	0.2	5.0	5.0	1.0	NT	
2N5903	N	78	0.005	4.5	40	0.03	0.5	70	—	3.0	0.2	5.0	10	1.0	NT	
2N5904	N	78	0.005	4.5	40	0.03	0.5	70	—	3.0	0.2	10	20	1.0	NT	
2N5905	N	78	0.005	4.5	40	0.03	0.5	70	—	3.0	0.2	15	40	1.0	NT	
2N5906	N	78	0.002	4.5	40	0.03	0.5	70	—	3.0	0.1	5.0	5.0	1.0	NT	
2N5907	N	78	0.002	4.5	40	0.03	0.5	70	—	3.0	0.1	5.0	10	1.0	NT	
2N5908	N	78	0.002	4.5	40	0.03	0.5	70	—	3.0	0.1	10	20	1.0	NT	
2N5909	N	78	0.002	4.5	40	0.03	0.5	70	—	3.0	0.1	15	20	1.0	NT	
U401	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	10	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	10	2.0	NNR	
U404	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	15	25	2.0	NNR	
U405	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	20	40	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	40	80	2.0	NNR	
U421	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	10	10	0.5	NNT	
U422	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	15	25	0.5	NNT	
U423	N	78	0.001	2.0	40	0.06	1.0	300	1500	3.0	10	25	40	0.5	NNT	
U424	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	10	10	1.0	NNT	
U425	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	15	25	1.0	NNT	
U426	N	78	0.003	3.0	40	0.06	1.8	300	1500	3.0	10	25	40	1.0	NNT	
U427	N	78	0.005	2.0	40	0.06	1.8	250	—	3.0	—	25	40	3.0	NNT	
U428	N	78	0.005	3.0	40	0.06	1.8	250	—	3.0	—	40	80	5.0	NNT	
2N5515	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	5.0	5.0	1.0	NS or NOP	
2N5516	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	5.0	10	1.0	NS or NOP	
2N5517	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	10	20	1.0	NS or NOP	
2N5518	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	15	40	1.0	NS or NOP	
2N5519	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	30	15	80	1.0	NS or NOP	
2N5520	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	5.0	5.0	1.0	NS or NOP	
2N5521	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	5.0	10	1.0	NS or NOP	
2N5522	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	15	20	1.0	NS or NOP	
2N5523	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	15	40	1.0	NS or NOP	
2N5524	N	71	0.25	4.0	40	0.5	7.5	1000	—	25	15	15	80	1.0	NS or NOP	
U401	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	10	10	2.0	NNR	

Product Specifications

Product Specifications (Cont'd)

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE (gfs (μmhos))		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD		OUTPUT CONDUCTANCE gfs (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
			Gate				Min.	Max.	Min.	Max.			Static Match (mV, Max.)	Temp Tracking (μV/°C)			
U404	N	71	0.025	10	2.5	50	0.5	2000	—	—	8.0	20	15	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	10	2.5	50	0.5	2000	—	—	8.0	20	20	40	2.0	NNR	LOW NOISE
U406	N	71	0.025	10	2.5	50	0.5	2000	—	—	8.0	20	40	80	2.0	NNR	LOW NOISE
2N5564	N	71	0.1	30	3.0	40	5.0	7500	—	—	12	50	5.0	10	45	NC	RF AMPLIFIER
2N5565	N	71	0.1	30	3.0	40	5.0	7500	—	—	12	50	10	25	45	NC	RF AMPLIFIER
2N5566	N	71	0.1	30	3.0	40	5.0	7500	—	—	12	50	20	50	45	NC	RF AMPLIFIER
2N5811	N	78	0.1	5.0	5.0	25	7.0	5000	—	—	3.0	20	10	20	100	NZF	RF AMPLIFIER
2N5812	N	78	0.1	5.0	5.0	25	7.0	5000	—	—	3.0	20	15	40	100	NZF	RF AMPLIFIER
U257	N	78	0.1	5.0	5.0	25	5.0	5000	—	—	5.0	30	100	—	150	NZF	RF AMPLIFIER
U430	N	99	0.15	12	4.0	25	12	10000	—	—	7.5	12	—	—	150	NZA	RF AMPLIFIER
U431	N	99	0.15	24	6.0	25	24	10000	—	—	7.5	10	—	—	150	NZA	RF AMPLIFIER
U440	N	71	0.50	6.0	6.0	25	6.0	4500	—	—	3.5	—	10	—	200	NZF	RF AMPLIFIER
U441	N	71	0.50	6.0	6.0	25	6.0	4500	—	—	3.5	—	20	—	200	NZF	RF AMPLIFIER
U443	N	78	.5	6	6	25	6.0	4500	9000	9000	3.5	—	10	—	200	NZF	RF AMPLIFIER
U444	N	78	.5	6.0	6.0	25	6.0	4500	9000	9000	3.5	—	20	—	200	NZF	RF AMPLIFIER
2N3921	N	71	1.0	1.0	3.0	50	1.0	1500	—	—	18	2.0	5.0	10	35	NNR or NRL-D	GENERAL PURPOSE
2N3922	N	71	1.0	1.0	3.0	50	1.0	1500	—	—	18	2.0	5.0	10	35	NNR or NRL-D	GENERAL PURPOSE
2N3954	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	5.0	10	35	NQP	GENERAL PURPOSE
2N3954A	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	5.0	10	35	NQP	GENERAL PURPOSE
2N3955	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	10	25	35	NQP	GENERAL PURPOSE
2N3955A	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	10	15	35	NQP	GENERAL PURPOSE
2N3956	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	15	50	35	NQP	GENERAL PURPOSE
2N3957	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	20	75	35	NQP	GENERAL PURPOSE
2N3958	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	0.5	25	100	35	NQP	GENERAL PURPOSE
2N4084	N	71	1.0	3.0	3.0	50	1.0	1500	—	—	18	2	15	10	35	NNR or NRL-D	GENERAL PURPOSE
2N4085	N	71	1.0	3.0	3.0	50	1.0	1500	—	—	18	2	15	25	35	NNR or NRL-D	GENERAL PURPOSE
2N5045	N	71	0.25	4.5	5.0	50	0.5	1500	—	—	8.0	200	5.0	67	25	NNR or NRL-D	GENERAL PURPOSE
2N5046	N	71	0.25	4.5	5.0	50	0.5	1500	—	—	8.0	200	10	133	25	NNR or NRL-D	GENERAL PURPOSE
2N5047	N	71	0.25	4.5	5.0	50	0.5	1500	—	—	8.0	200	15	200	25	NNR or NRL-D	GENERAL PURPOSE
2N5452	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	20	5.0	5.0	1.0	NQP	GENERAL PURPOSE
2N5453	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	20	10	10	1.0	NQP	GENERAL PURPOSE
2N5454	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	4.0	20	15	25	1.0	NQP	GENERAL PURPOSE
DN5564	N	71	1	3.0	3.0	40	5	7500	12500	12500	12	50	5	10	65	NC	GENERAL PURPOSE
DN5565	N	71	1	3.0	3.0	40	5	7500	12500	12500	12	50	10	25	65	NC	GENERAL PURPOSE
DN5566	N	71	1	3.0	3.0	40	5	7500	12500	12500	12	50	20	50	65	NC	GENERAL PURPOSE
U231	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	6.0	80	5.0	10	35	NP-D	GENERAL PURPOSE
U232	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	6.0	80	10	25	35	NP-D	GENERAL PURPOSE
U233	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	6.0	80	15	50	35	NP-D	GENERAL PURPOSE
U234	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	6.0	80	20	75	35	NP-D	GENERAL PURPOSE
U235	N	71	0.1	4.5	5.0	50	0.5	1000	—	—	6.0	80	25	100	35	NP-D	GENERAL PURPOSE
U410	N	71	0.2	3.5	4.0	40	0.5	1000	—	—	—	13	10	10	20	NQP	GENERAL PURPOSE
U411	N	71	0.2	3.5	4.0	40	0.5	1000	—	—	—	13	20	25	20	NQP	GENERAL PURPOSE
U412	N	71	0.2	3.5	4.0	40	0.5	1000	—	—	—	13	40	80	20	NQP	GENERAL PURPOSE
DN5567	N	71	0.1	3.0	3.0	40	5	60	—	—	7.0	—	20	—	—	NC	SWITCH

Product Specifications (Cont'd)

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop Volts (Max.)	Capacitance (pF, Max.)
				Min.	Max.		
DPAD1	78	Dual	1	45	120	1.5	0.8
DPAD2	72	Dual	2	45	120	1.5	0.8
DPAD5	72	Dual	5	45	120	1.5	0.8
DPAD10	72	Dual	10	35	—	1.5	2.0
DPAD20	72	Dual	20	35	—	1.5	2.0
DPAD50	72	Dual	50	35	—	1.5	2.0
DPAD100	72	Dual	100	35	—	1.5	2.0
JPAD2	92	Single	2	35	—	1.5	2.0
JPAD5	92	Single	5	35	—	1.5	2.0
JPAD10	92	Single1	10	35	—	1.5	2.0
JPAD20	92	Single	20	35	—	1.5	2.0
JPAD50	TO-92	Single	20	35	—	1.5	2.0
JPAD100	TO-92	Single	50	35	—	1.5	2.0
JPAD200	TO-92	Single	100	35	—	1.5	2.0
JPAD500	TO-92	Single	500	35	—	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	—	1.5	2.0
PAD20	18	Single	20	35	—	1.5	2.0
PAD50	18	Single	50	35	—	1.5	2.0
PAD100	18	Single	100	35	—	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	3.5	7.0	20	60	NC
VCR3P	P	72	15	3.5	7.0	70	200	PE
VCR4N	N	18	15	3.5	7.0	200	600	NP
VCR5P	P	72	15	3.5	7.0	300	900	PC
VCR7N	N	72	15	2.5	5.0	4000	8000	NT
VCR11N	N	71	30	8.0	12.0	100	200	NS

P-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω , Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	—	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	—	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	—	3.0	—	20	25	6.0	1.5	MRA

Product Specifications (Cont'd)

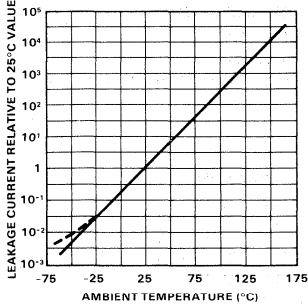
Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	—	NKL
CR024	18	0.24	10	1.00	100	10	—	NKL
CR027	18	0.27	10	1.00	100	9.0	—	NKL
CR030	18	0.30	10	1.00	100	8.0	—	NKL
CR033	18	0.33	10	1.00	100	6.6	—	NKL
CR039	18	0.39	10	1.05	100	4.1	—	NKL
CR043	18	0.43	10	1.05	100	3.3	—	NKL
CR047	18	0.47	10	1.10	100	2.7	—	NKL
CR056	18	0.56	10	1.20	100	1.9	—	NKL
CR062	18	0.62	10	1.30	100	1.55	—	NKL
CR068	18	0.68	10	1.15	100	1.35	—	NKM
CR075	18	0.75	10	1.20	100	1.15	—	NKM
CR082	18	0.82	10	1.25	100	1.00	—	NKM
CR091	18	0.91	10	1.29	100	0.88	—	NKM
CR100	18	1.00	10	1.35	100	0.80	—	NKM
CR110	18	1.10	10	1.40	100	0.70	—	NKM
CR120	18	1.20	10	1.45	100	0.64	—	NKM
CR130	18	1.30	10	1.50	100	0.58	—	NKM
CR140	18	1.40	10	1.55	100	0.54	—	NKM
CR150	18	1.50	10	1.60	100	0.51	—	NKM
CR160	18	1.60	10	1.65	100	0.475	—	NKO
CR180	18	1.80	10	1.75	100	0.42	—	NKO
CR200	18	2.00	10	1.85	100	0.395	—	NKO
CR220	18	2.20	10	1.95	100	0.37	—	NKO
CR240	18	2.40	10	2.00	100	0.345	—	NKO
CR270	18	2.70	10	2.15	100	0.32	—	NKO
CR300	18	3.00	10	2.25	100	0.30	—	NKO
CR330	18	3.30	10	2.35	100	0.28	—	NKO
CR360	18	3.60	10	2.50	100	0.265	—	NKO
CR390	18	3.90	10	2.60	100	0.255	—	NKO
CR430	18	4.30	10	2.75	100	0.245	—	NKO
CR470	18	4.70	10	2.90	100	0.235	—	NKO
CRR0240	18	.24	25	1.0	100	.9	—	NKL
CRR0360	18	.36	25	1.05	100	4.1	—	NKL
CRR0560	18	.56	25	1.30	100	1.15	—	NKL
CRR0800	18	.80	25	1.35	100	0.8	—	NKL
CRR1250	18	1.95	25	1.60	100	.54	—	NKM
CRR1950	18	1.95	25	1.95	100	.37	—	NKM
CRR2900	18	2.90	25	2.35	100	.28	—	NKO
CRR4300	18	4.30	25	3.00	100	0.5	—	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL
J552	92	0.05	50	1.5	50	2.0	2	NKL
J553	92	(.18 - 0.75)	—	.75	50	10	—	NCL
J554	92	(06 - 1.6)	—	.75	50	1.0	—	NCL
J555	92	(1.4 - 2.6)	—	.75	50	.88	—	NCL
J556	92	(2.4 - 3.8)	—	.75	50	.6	—	NCL
J557	92	(3.6 - 5.3)	—	1.5	50	.48	—	NCL
J9100	92	0.05	50	1.5	50	2.0	2	NCL
JR135V	92	0.200	—	0.9	135	2.0	—	VRMA
JR170V	92	0.200	—	0.9	170	2.0	—	VRMA
JR200V	92	0.200	—	0.9	200	2.0	—	VRMA
JR220V	92	0.200	—	0.9	220	2.0	—	VRMA
JR240V	92	0.200	—	0.9	240	2.0	—	VRMA

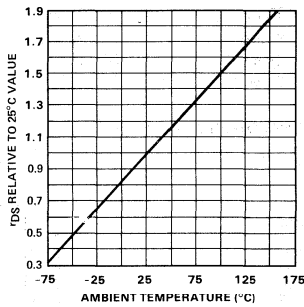
Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

Useful JFET Parameter Relationships (Approximate)

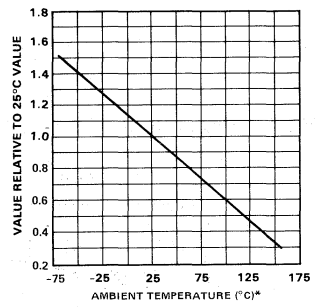
Bulk & Junction Leakage Current vs Ambient Temperature



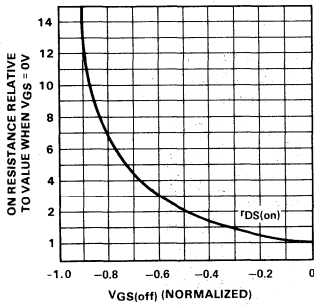
On Resistance vs Ambient Temperature



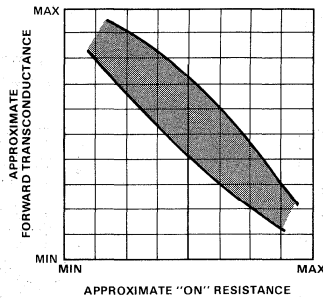
Drain Current and Transconductance vs Ambient Temperature



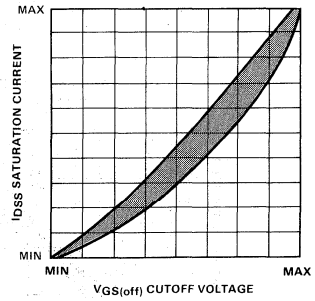
Typical $r_{DS(on)}$ vs Normalized Gate Source Cutoff Voltage



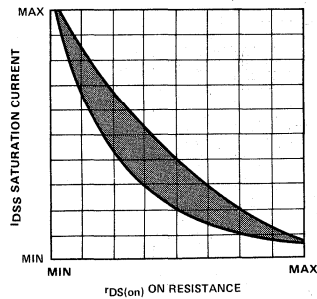
On Resistance vs Transconductance



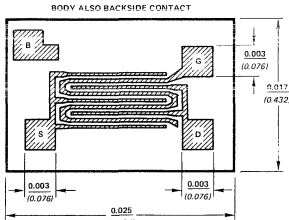
Saturation Current vs Cutoff Voltage



Saturation Current vs ON Resistance



*When $I_D > 5 \times I_{D2}$



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

enhancement-type p-channel MOSFET designed for . . .

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

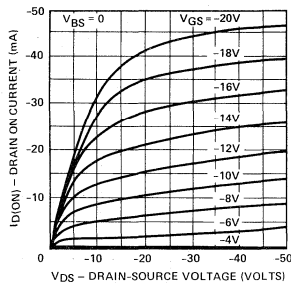
BENEFITS:

- High Gate Transient Voltage Break-down Eliminates Need for Gate Protective Diode
- Ultra-High Input Impedance
- Low Leakage
- Normally OFF

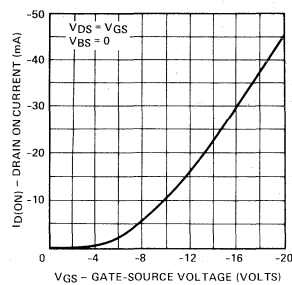
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

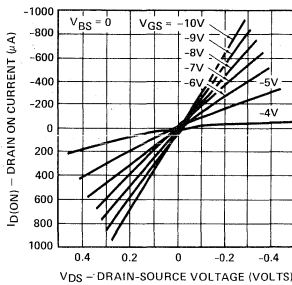
Output Characteristics



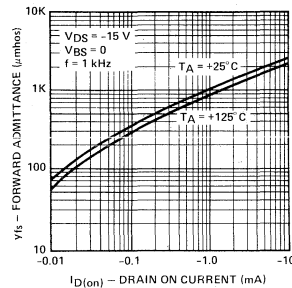
Transfer Characteristic



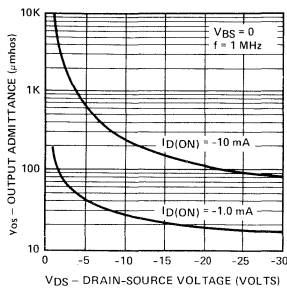
Low-Level Output Characteristics



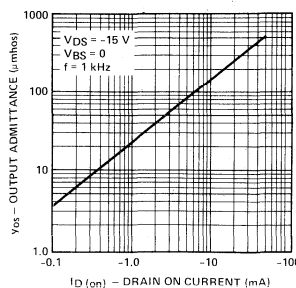
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

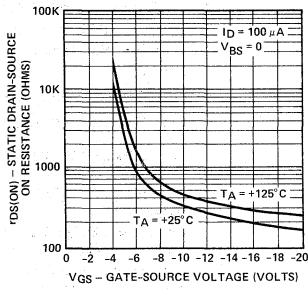


Common-Source, Short-Circuit, Output Admittance vs Drain Current

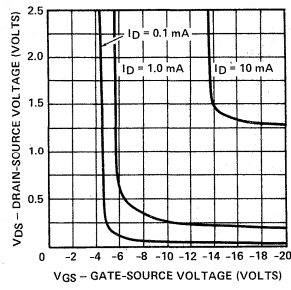


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

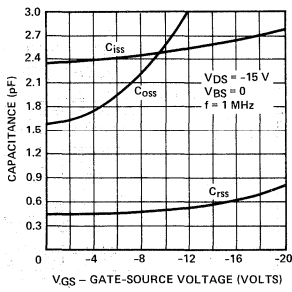
Drain-Source ON Resistance vs Gate-Source Voltage



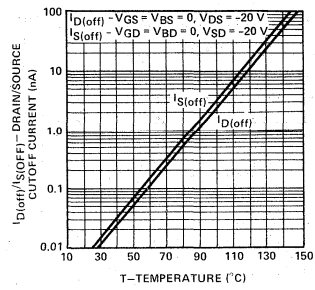
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage

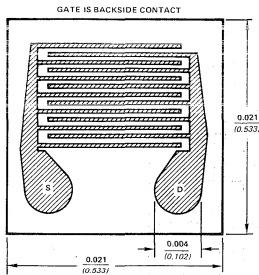


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFETs designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch



BENEFITS:

- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver
- High Off-Isolation $I_{D(off)} < 100 \mu A$
- High Speed $t_{ON} < 20 ns$

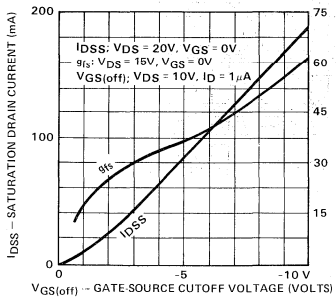
PRINCIPAL DEVICES

2N3970-72, 2N4091-93, 2N4391-93
2N4856-61, 2N4856A-61A, FN4392,93
U200-01, VCR2N
2N5638-40, 2N5653-54, J1111-13
PN4091,93 PN4391-93 U1897-99
2N5564-66, DN5564-66, DN5567
All of above single devices available in chip form
2N5566 Chip Set, DN5566 Chip Set

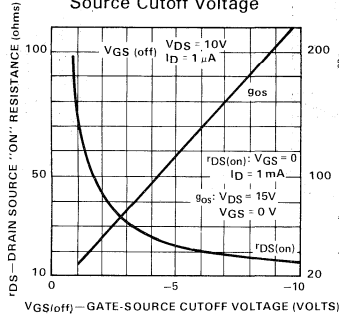
TYPE	PACKAGE
Single	TO-18
Single	TO-92
Dual	TO-71
Single	Chip
Dual	Chip

PERFORMANCE CURVES (25°C unless otherwise noted)

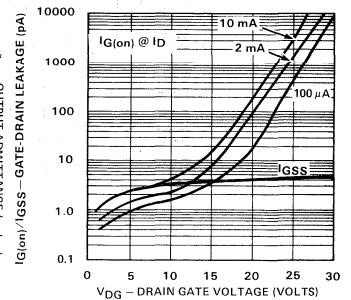
Drain Current & Transconductance vs Gate Source Voltage



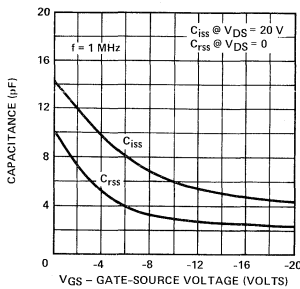
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



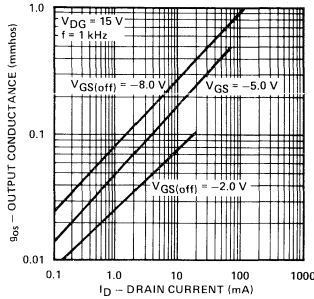
Gate Operating Current vs Drain Gate Voltage



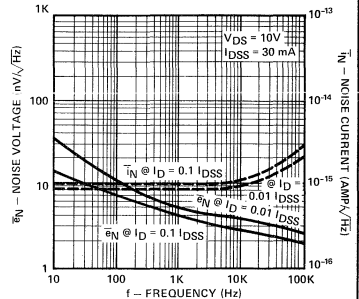
Common-Source Capacitances vs Gate-Source Voltage



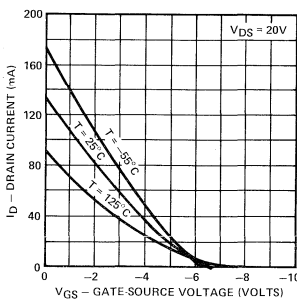
Common-Source Output Conductance vs Drain Current



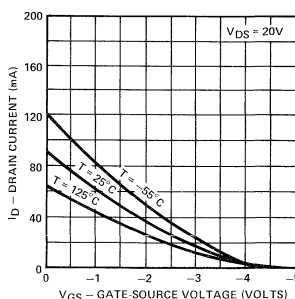
Equivalent Input Noise Voltage and Noise Current vs Frequency



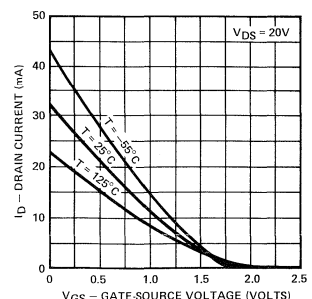
Transfer Characteristics



Transfer Characteristics

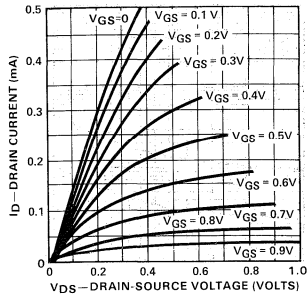


Transfer Characteristics

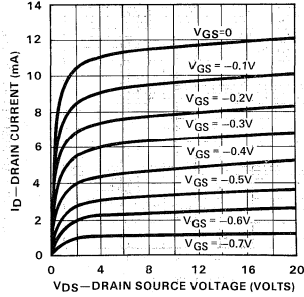


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

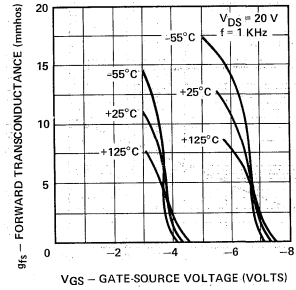
Output Characteristic
(V_{GS(off)} = -1.5V)



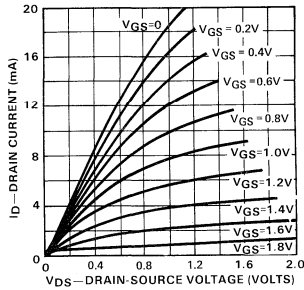
Output Characteristic
(V_{GS(off)} = -1.5V)



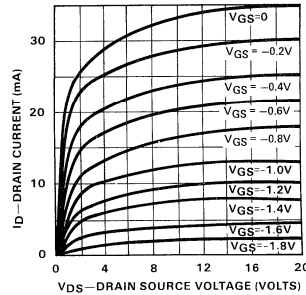
Transconductance Characteristics



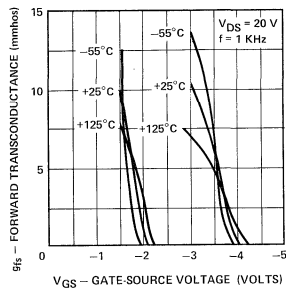
Output Characteristic
(V_{GS(off)} = -3.0V)



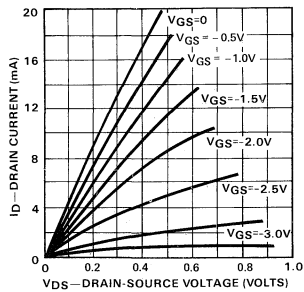
Output Characteristic
(V_{GS(off)} = -3.0V)



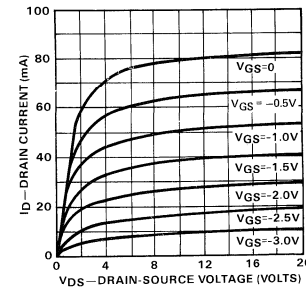
Transconductance Characteristics



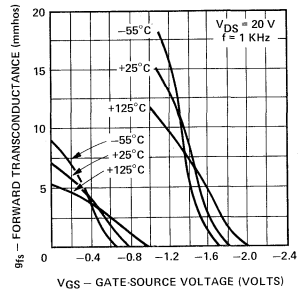
Output Characteristic
(V_{GS(off)} = -5.0V)



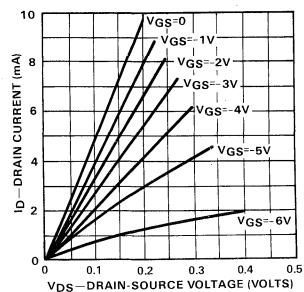
Output Characteristic
(V_{GS(off)} = -5.0V)



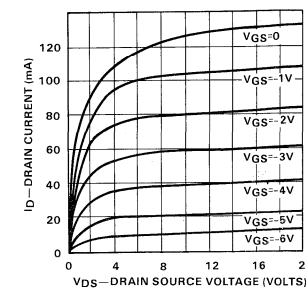
Transconductance Characteristics



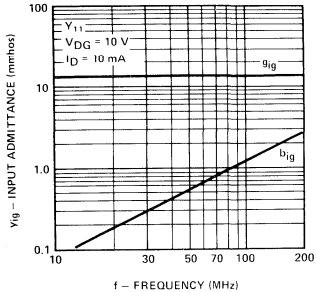
Output Characteristic
(V_{GS(off)} = -8.0V)



Output Characteristic
(V_{GS(off)} = -8.0V)

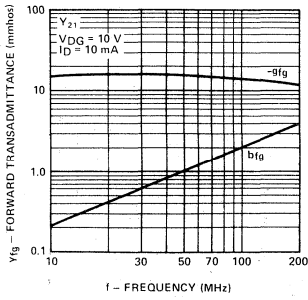


Common-Gate Input Admittance vs Frequency

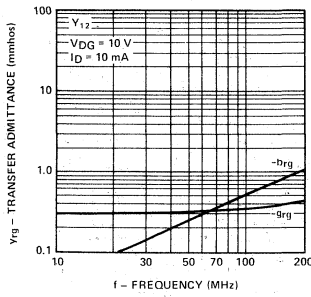


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

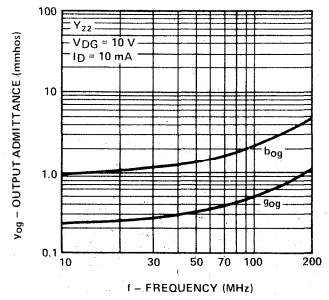
Common-Gate Forward Transmittance vs Frequency



Common-Gate Reverse Transfer Admittance vs Frequency



Common-Gate Output Admittance vs Frequency

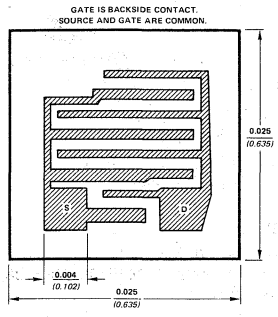




n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing

- BENEFITS:**
- Simple Two Lead Current Source
 - Simplifies Floating Current Sources
No Power Supplies Required
 - Low Cost



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

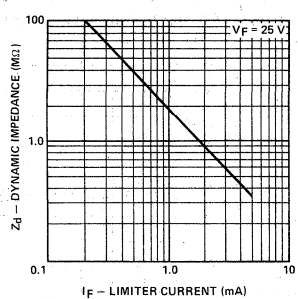
TYPE
Single
Single

PACKAGE
TO-92
Chip

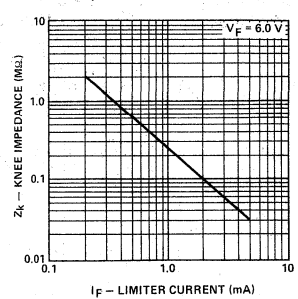
PRINCIPAL DEVICES
J500-505, J506-511, J553-7
J500CHP-505CHP, J506CHP-511 CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

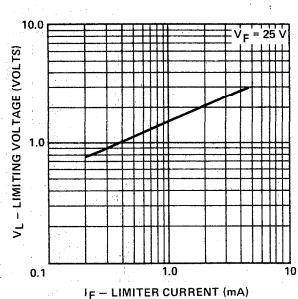
Dynamic Impedance vs Limiter Current



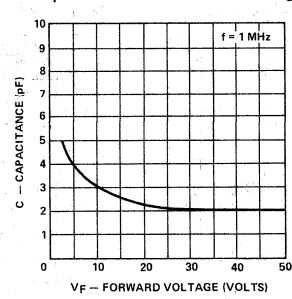
Knee Impedance vs Limiter Current



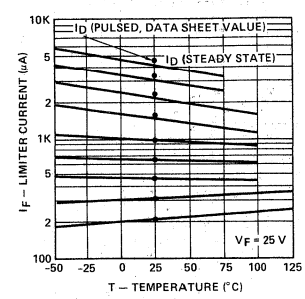
Limiting Voltage at 0.9 ID vs Limiter Current

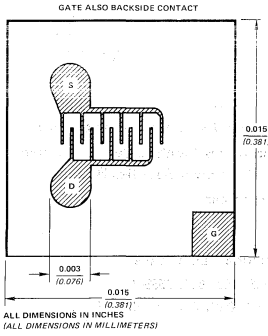


Capacitance vs Forward Voltage



**Typical Variation of ID with Temperature
Steady State and Pulsed Value**





n-channel JFET designed for . . .

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch



BENEFITS:

- Low Noise
NF = 3 dB Typical @ 400 MHz
- Wideband
High g_{fs}/C_{iss} Ratio

TYPE PACKAGE

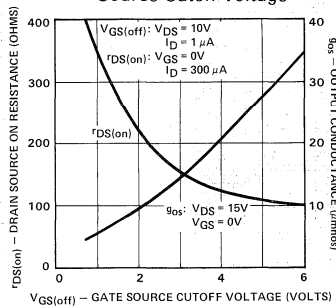
Single	TO-72
Single	TO-92
Single	Chip

PRINCIPAL DEVICES

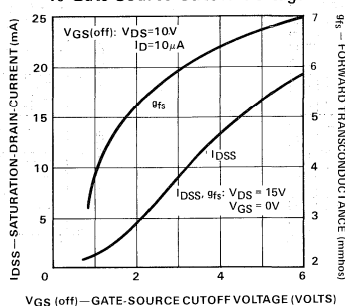
2N3966, 2N4416-16A 2N3819
2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108,
MPF112, PN4416, J304-5,
All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

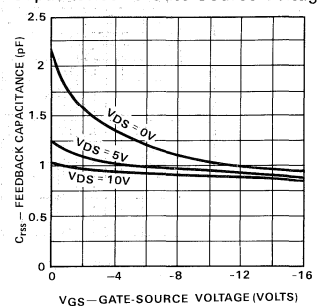
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



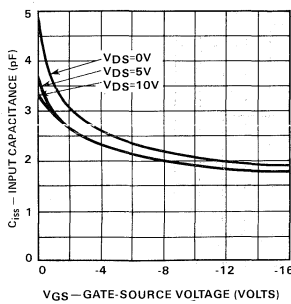
Drain Current & Transconductance vs Gate Source Cutoff Voltage



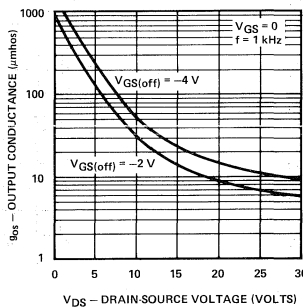
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



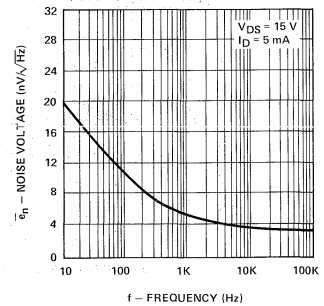
Common Source Input Capacitance vs Gate-Source Voltage



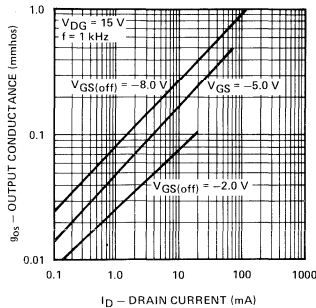
Common-Source Output Conductance vs Drain-Source Voltage



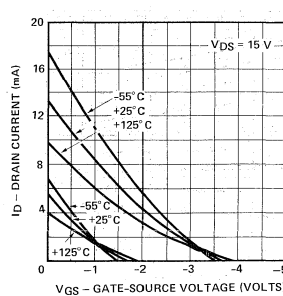
Equivalent Input Noise Voltage vs Frequency



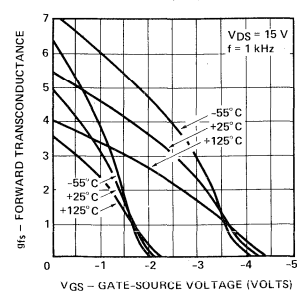
Common-Source Output Conductance vs Drain Current



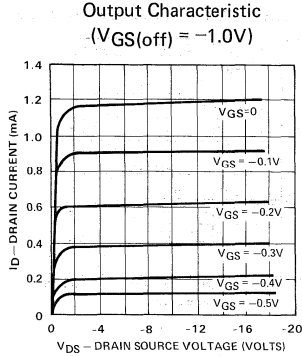
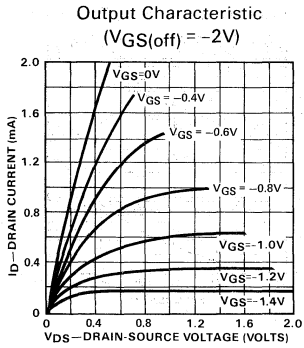
Transfer Characteristics



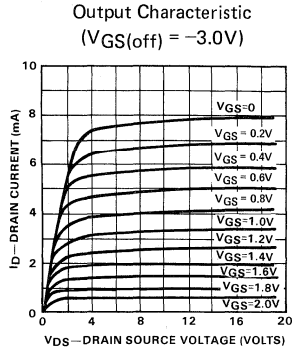
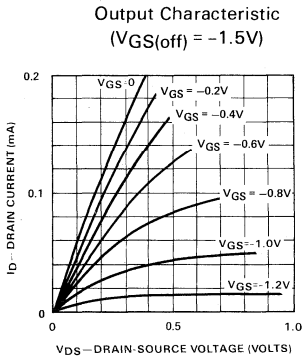
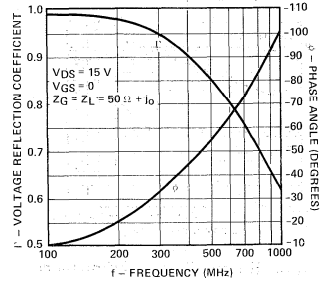
Transconductance Characteristics



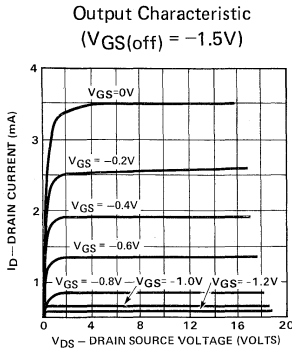
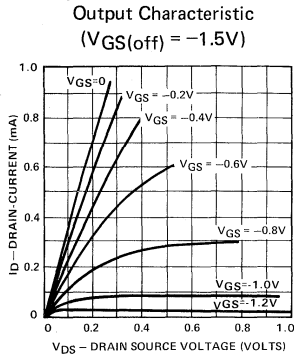
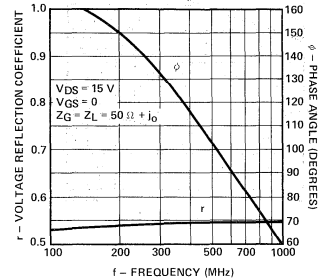
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)



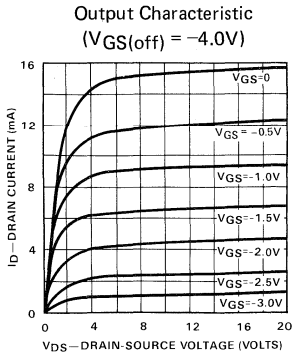
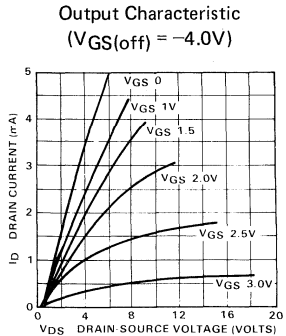
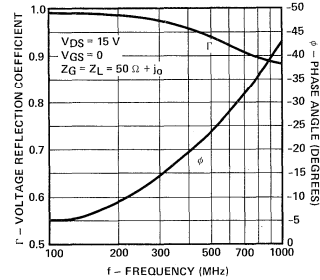
S Parameters S_{11} Common-Source vs Frequency



S Parameters S_{21} Common-Source vs Frequency

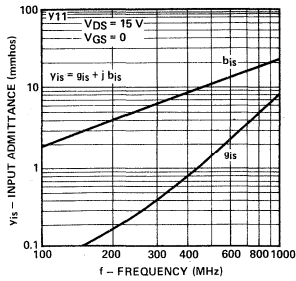


S Parameters S_{22} Common-Source vs Frequency

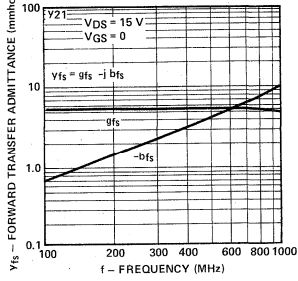


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

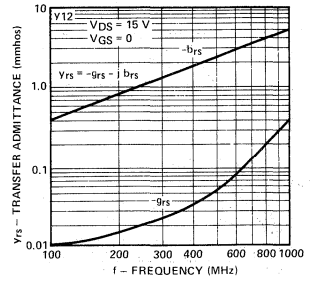
Common-Source Input Admittance vs Frequency



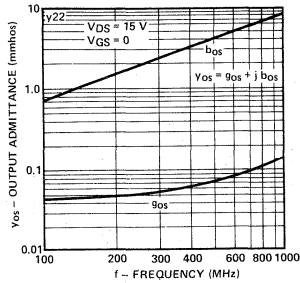
Common-Source Forward Transfer Admittance vs Frequency

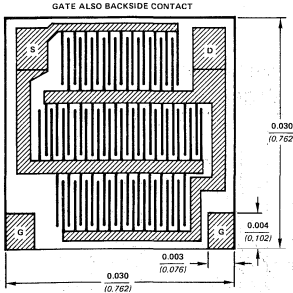


Common-Source Reverse Transfer Admittance vs Frequency



Common-Source Output Admittance vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

TYPE	PACKAGE
Single	TO-52
Single	TO-92
Single	Chip

BENEFITS:

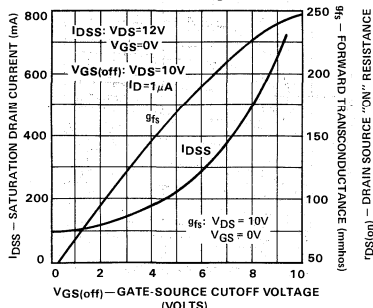
- Low Insertion Loss
- Small Error in Measurement Systems
 $V_{DS(on)} < 50 \text{ mV}$ (2N5432)
- High Off-Isolation $I_{D(off)} < 200 \text{ pA}$
- High Speed $t_{d(on)} < 4 \text{ ns}$
- Low Noise Audio-Freq Amplification
 $e_N < 2 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz

PRINCIPAL DEVICES

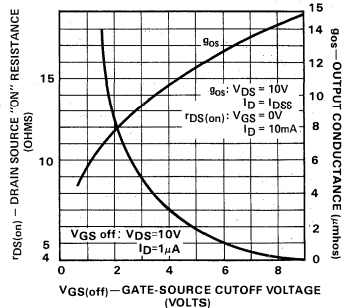
- 2N5432-34
- J108-10
- All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

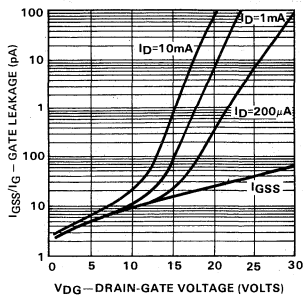
Drain Current & Forward Transconductance vs Gate Source Cutoff Voltage



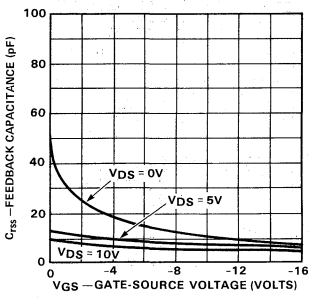
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



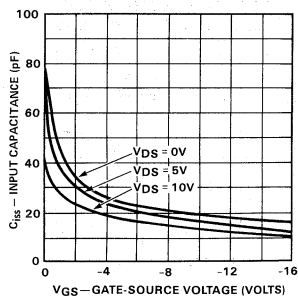
Gate Operating Current vs Drain-Gate Voltage



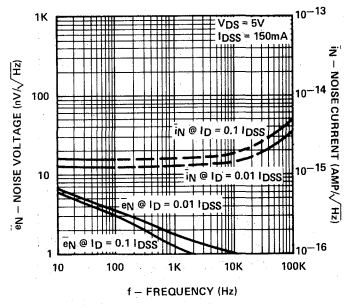
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



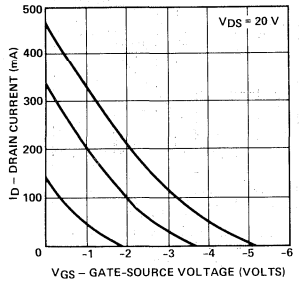
Common Source Input Capacitance vs Gate-Source Voltage



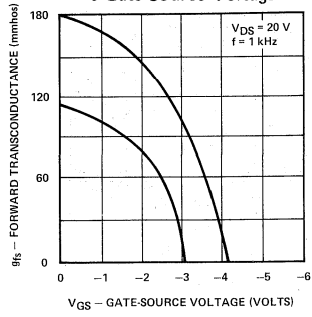
Equivalent Input Noise Voltage and Noise Current vs Frequency



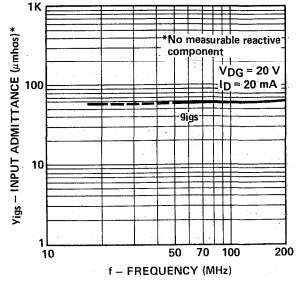
Transfer Characteristics



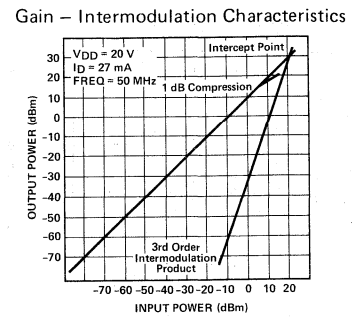
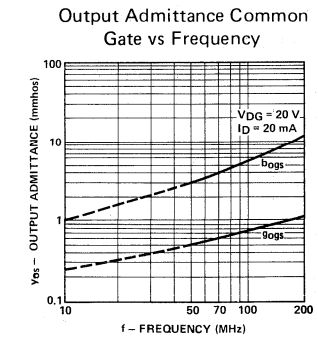
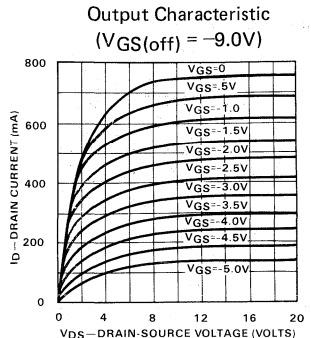
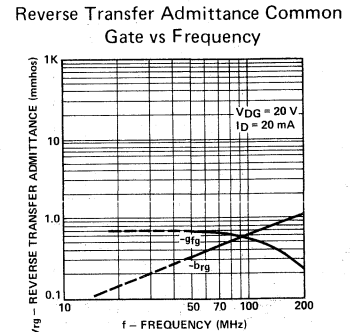
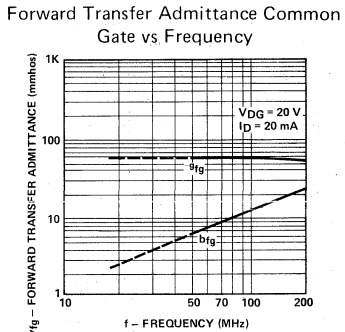
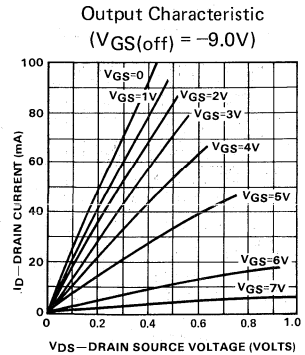
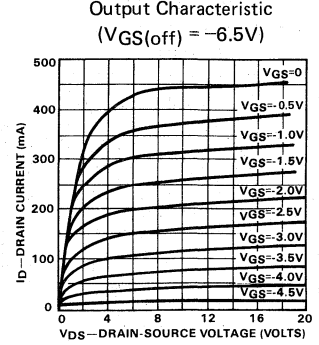
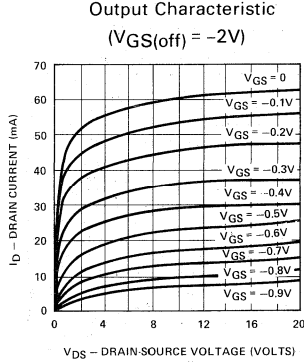
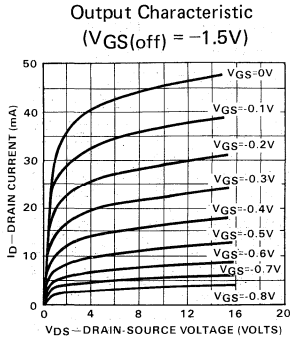
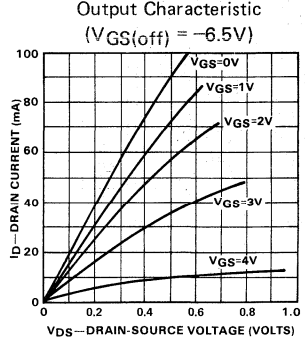
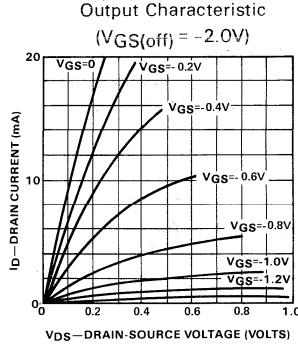
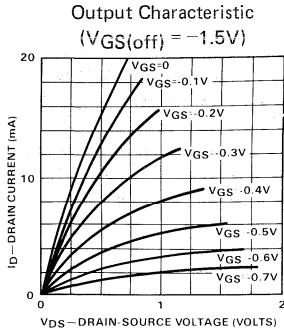
Forward Transconductance vs Gate Source Voltage

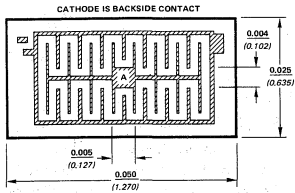


Input Admittance Common Gate vs Frequency



PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)





ALL DIMENSIONS IN INCHES
ALL DIMENSIONS IN MILLIMETERS

n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

BENEFITS:

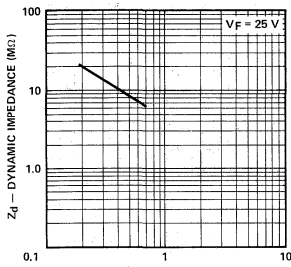
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

TYPE	PACKAGE
Single	TO-18 (2-lead)
Single	Chip

PRINCIPAL DEVICES
CR022 Thru CR062
CRR0240 Thru CRR0560
All of above

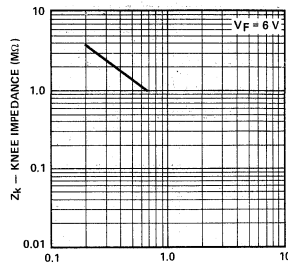
PERFORMANCE CURVES (25°C unless otherwise noted)

Dynamic Impedance vs Regulator Current



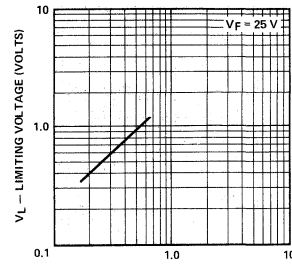
I_F - REGULATOR CURRENT (mA)

Knee Impedance vs Regulator Current



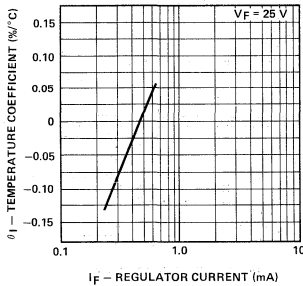
I_F - REGULATOR CURRENT (mA)

Limiting Voltage @ 0.8 If vs Regulator Current



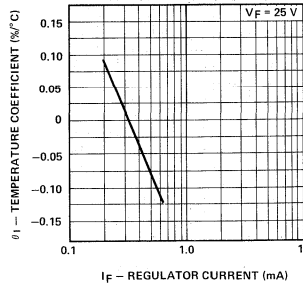
I_F - REGULATOR CURRENT (mA)

Temperature Coefficient
-55°C ≤ T_j ≤ 25°C vs Regulator Current



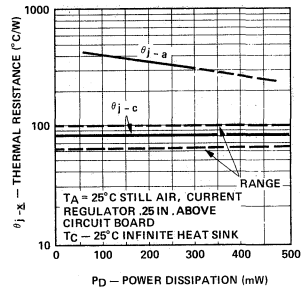
I_F - REGULATOR CURRENT (mA)

Temperature Coefficient
25°C ≤ T_j ≤ 125°C vs Regulator Current

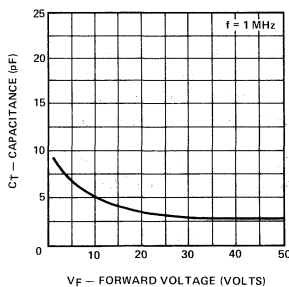


I_F - REGULATOR CURRENT (mA)

Thermal Resistance vs Power Dissipation



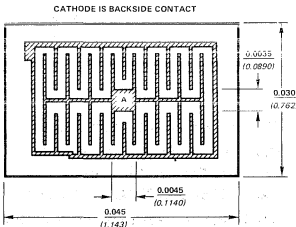
Capacitance vs Forward Voltage



V_F - FORWARD VOLTAGE (VOLTS)

NOTE: I_F , Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25^\circ\text{C})]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-c}}$ or $\frac{1}{\theta_{j-a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
ALL DIMENSIONS IN MILLIMETERS

n-channel JFET current regulator diode designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References



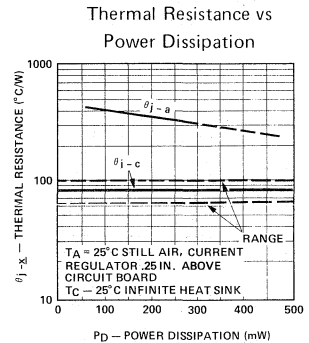
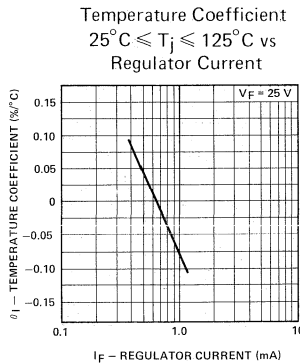
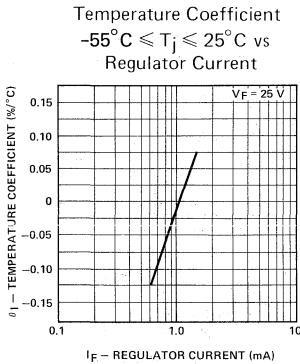
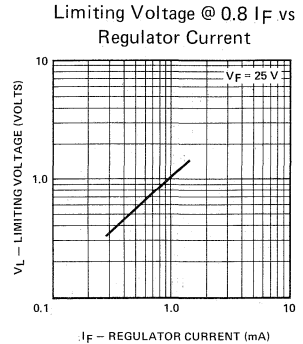
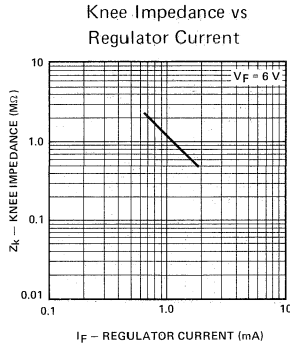
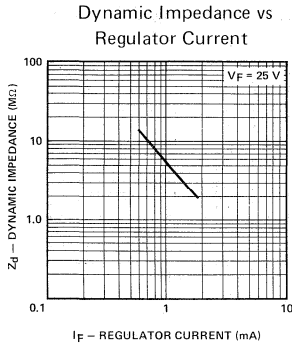
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
No Power Supplies Required

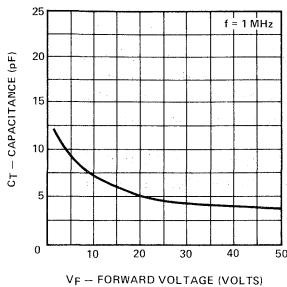
TYPE	PACKAGE
Single	TO-18 (2-lead)
Single	Chip

PRINCIPAL DEVICES
CR068 Thru CR150
CRR0800 Thru CRR1250
All of above

PERFORMANCE CURVES (25°C unless otherwise noted)



Capacitance vs Forward Voltage



NOTE: If, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_1 (T_j - 25^\circ\text{C})]$ where θ_1 is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a} P_D = T_{case} + \theta_{j-c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-c}}$ or $\frac{1}{\theta_{j-a}}$ is the derating factor for all devices.

n-channel JFET current regulator diode designed for . . .

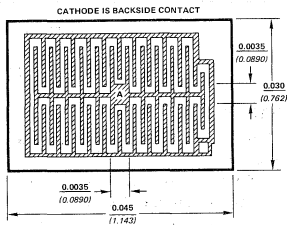
- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

PRINCIPAL DEVICES

CR160 Thru CR470
CRR1950 Thru CRR4300
All of above

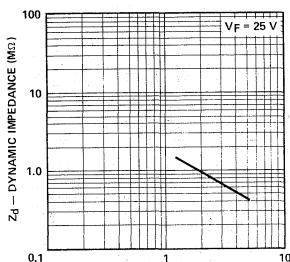


ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

TYPE	PACKAGE
Single	TO-18 (2-lead)
Single	Chip

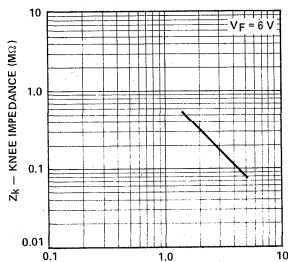
PERFORMANCE CURVES (25°C unless otherwise noted)

Dynamic Impedance vs Regulator Current



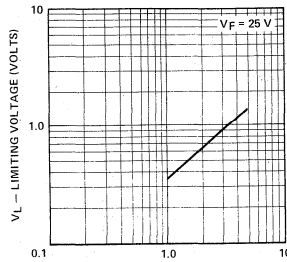
I_F - REGULATOR CURRENT (mA)

Knee Impedance vs Regulator Current



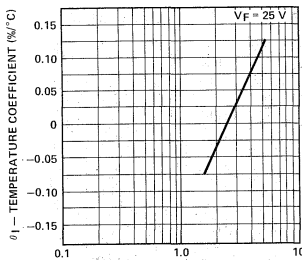
I_F - REGULATOR CURRENT (mA)

Limiting Voltage @ 0.8 I_F vs Regulator Current



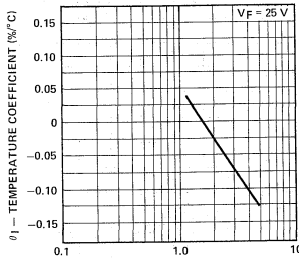
I_F - REGULATOR CURRENT (mA)

Temperature Coefficient
-55°C ≤ T_j ≤ 25°C vs Regulator Current



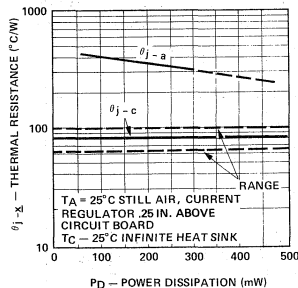
I_F - REGULATOR CURRENT (mA)

Temperature Coefficient
25°C ≤ T_j ≤ 125°C vs Regulator Current

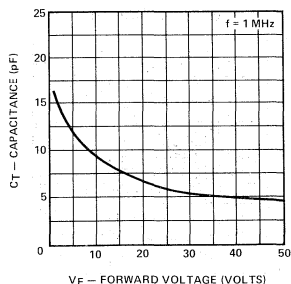


I_F - REGULATOR CURRENT (mA)

Thermal Resistance vs Power Dissipation

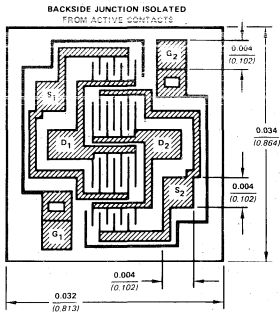


Capacitance vs Forward Voltage



NOTE: I_F , Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_j (T_j - 25^\circ\text{C})]$ where θ_j is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a} P_D = T_{case} + \theta_{j-c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-c}}$ or $\frac{1}{\theta_{j-a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators



BENEFITS:

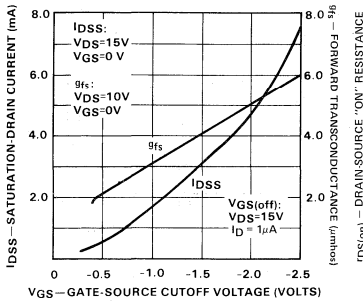
- Minimum System Error and Calibration
 - 5 mV Offset Maximum (J401)
 - 95 dB Minimum CMRR
- Low Drift With Temperature
 - 10 $\mu\text{V}/^\circ\text{C}$ (J401)
- Simplifies Amplifier Design
 - Output Conductance < 2 μmho
- Low Noise
 - $e_n = 6 \text{ nV}/\sqrt{\text{Hz}}$ at 10 Hz Typical

TYPE	PACKAGE
Dual	TO-71
Dual	Chip

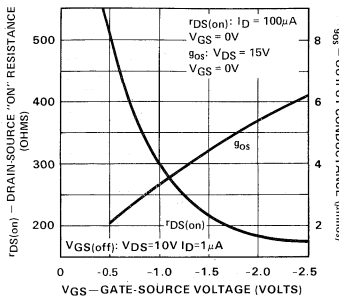
PRINCIPAL DEVICES

2N3921-2, 2N4084-5, 2N5045-7,
U401-6, 2N4085CHP,
2N5046CHP-47CHP, U403CHP-06CHP

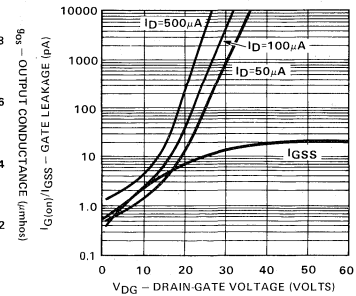
Drain Current & Transconductance vs Gate Source Voltage



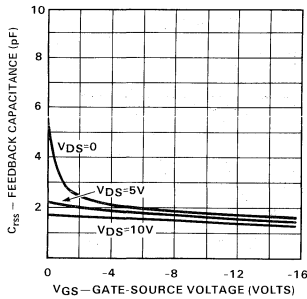
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



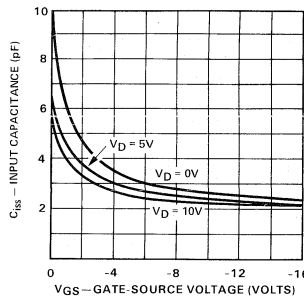
Gate Operating Current vs Drain Gate Voltage



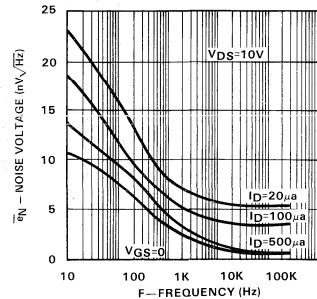
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



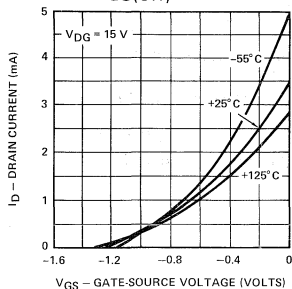
Common-Source Input Capacitance vs Gate-Source Voltage



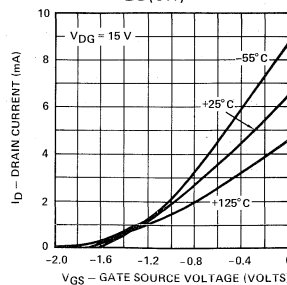
Noise Voltage vs Frequency



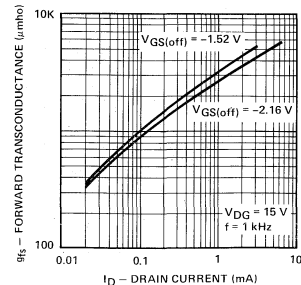
Transfer Characteristics Low VGS(off) Unit (-1.5 V)



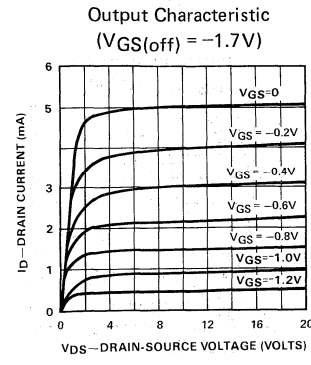
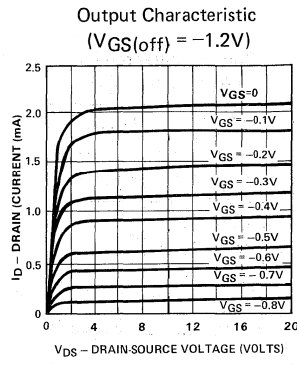
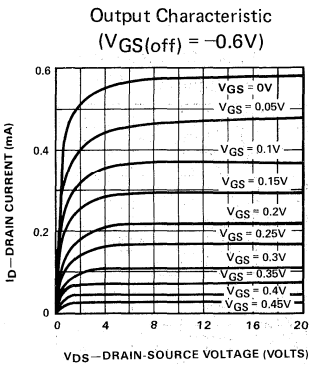
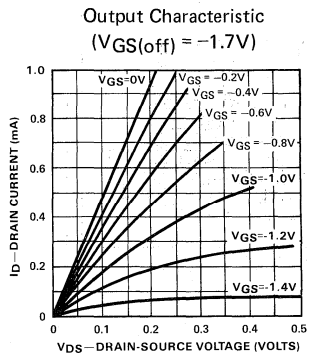
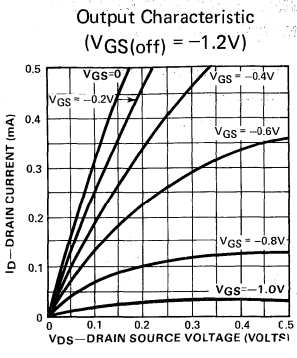
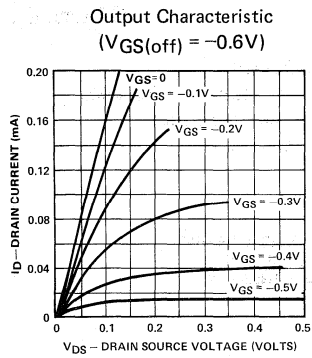
Transfer Characteristics Medium VGS(off) Unit (-2.2 V)



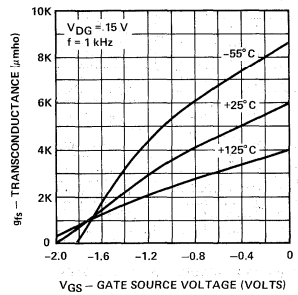
Forward Transconductance vs Drain Current



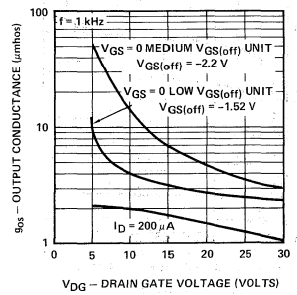
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

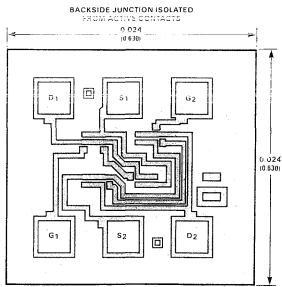


Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (-2.0V)



Output Conductance
vs Drain Gate Voltage





ALL DIMENSIONS IN INCHES
 (ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFETs designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers



BENEFITS:

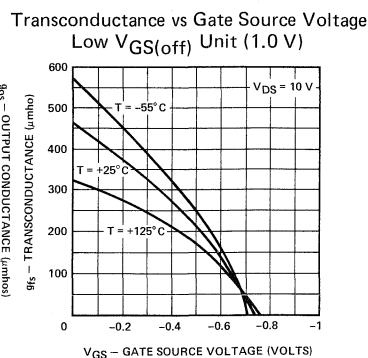
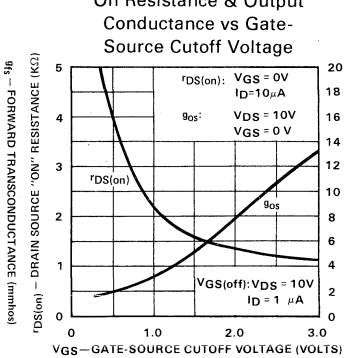
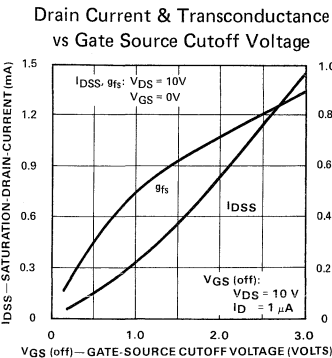
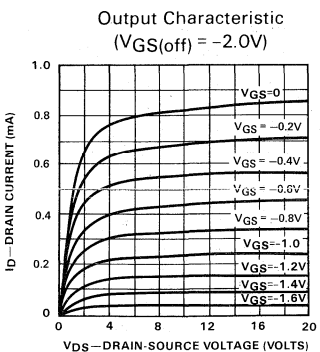
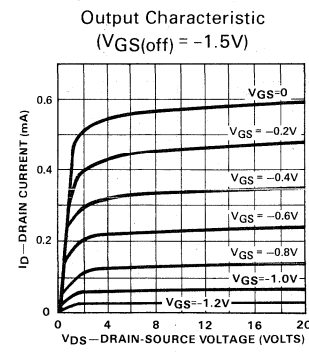
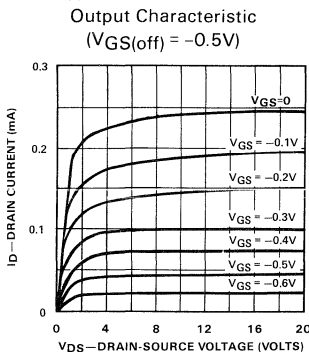
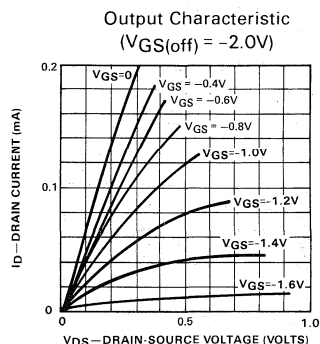
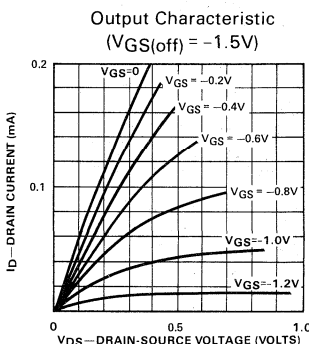
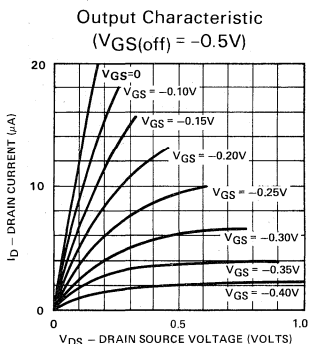
- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

TYPE
 Dual
 Dual

PACKAGE
 TO-78
 Chip

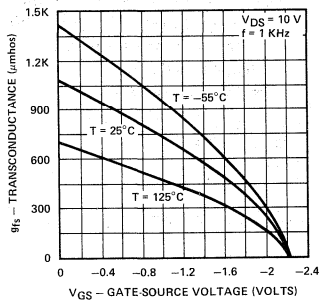
PRINCIPAL DEVICES
 U421-28, U422,
 U423, U425, U426

PERFORMANCE CURVES (25°C unless otherwise noted)

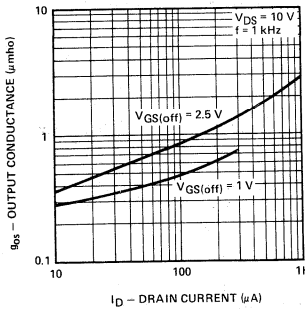


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

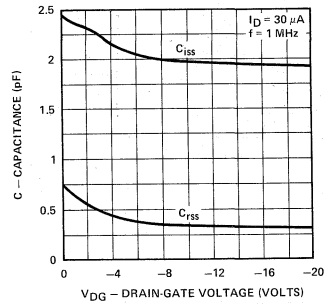
Transconductance vs Gate Source Voltage
High $V_{GS(off)}$ Unit (2.5 V)



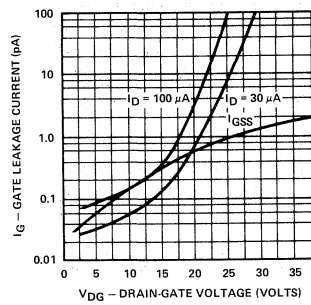
Common-Source Output Conductance vs Drain Current



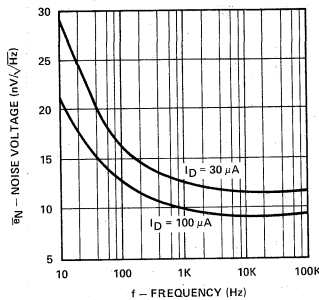
Capacitance vs Drain Gate Voltage

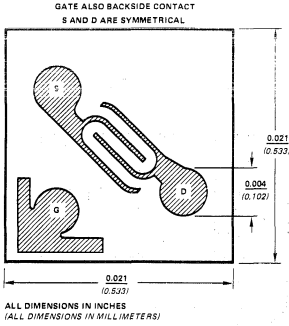


Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency





n-channel JFET designed for . . .

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

TYPE	PACKAGE
Single	TO-18
Dual	TO-71
Single	TO-92
Dual	Chip
Single	Chip



BENEFITS:

- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)} < 1 V$ (2N4338)
- High Off-Isolation As a Switch
 $I_{D(off)} < 50 pA$
- High Input Impedance

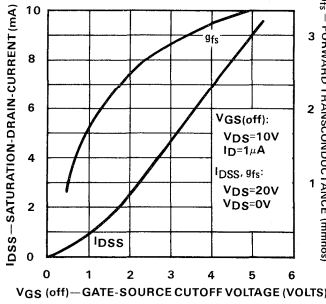
PRINCIPAL DEVICES

- 2N4338-41, VCR4N
- U231-5
- J201-204, PN4302-04

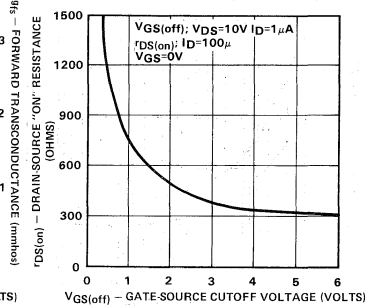
All single Part No's above

PERFORMANCE CURVES (25°C unless otherwise noted)

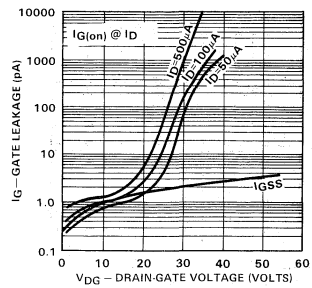
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



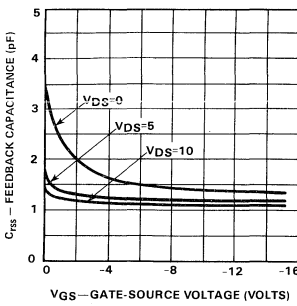
ON Resistance vs Gate-Source Cutoff Voltage



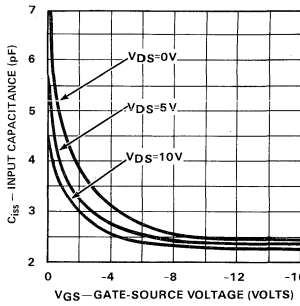
Gate Operating Current vs Drain-Gate Voltage



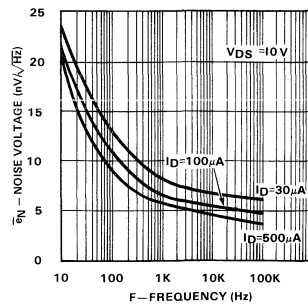
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



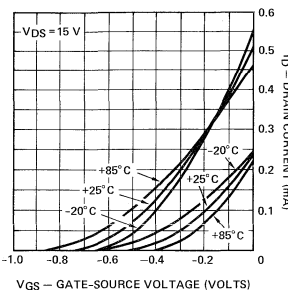
Common Source Input Capacitance vs Gate-Source Voltage



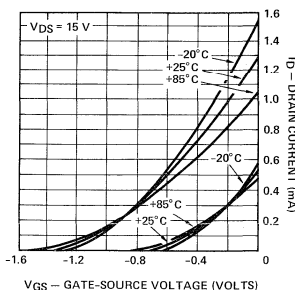
Noise Voltage vs Frequency



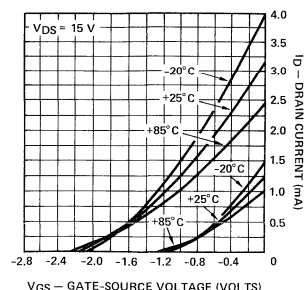
Transfer Characteristics



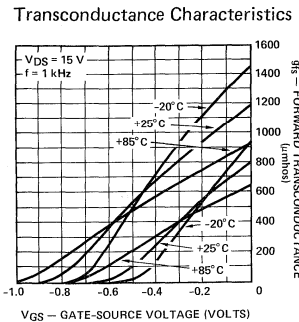
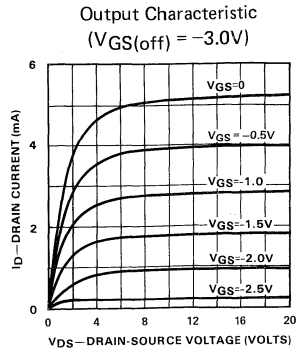
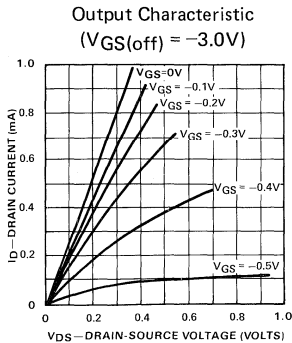
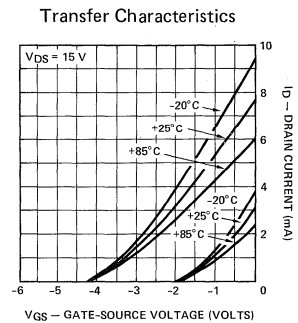
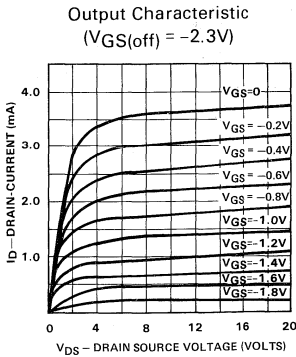
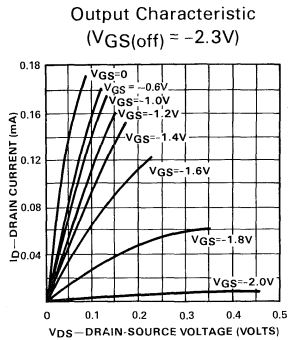
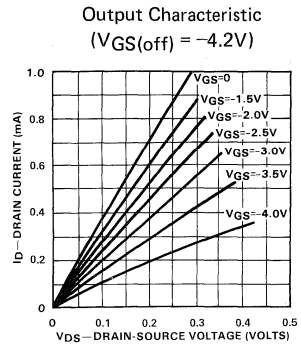
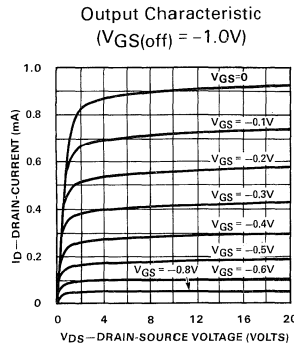
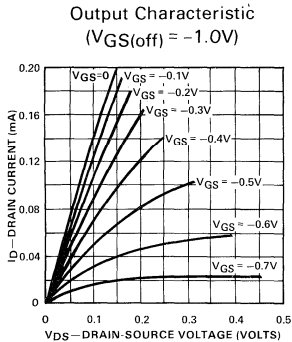
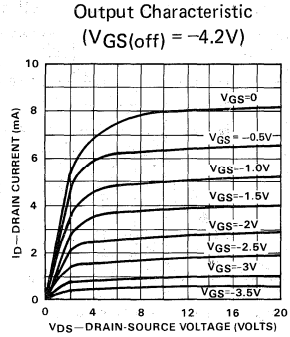
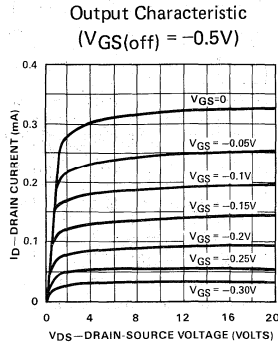
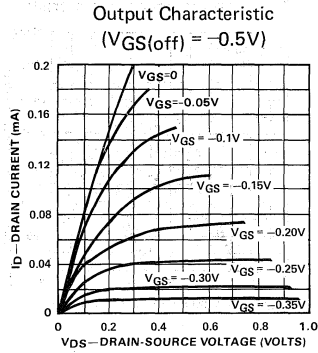
Transfer Characteristics



Transfer Characteristics

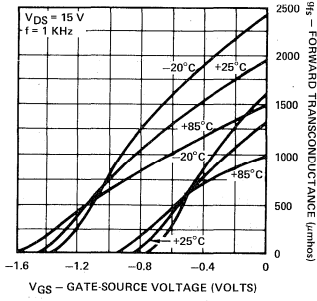


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

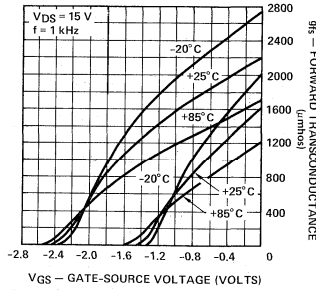


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

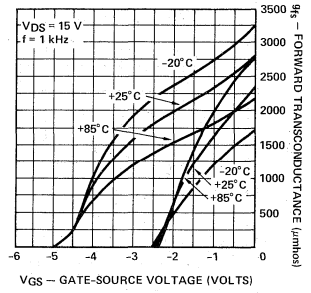
Transconductance Characteristics



Transconductance Characteristics



Transconductance Characteristics





monolithic dual n-channel JFET designed for . . .

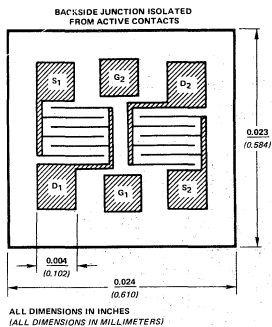
■ General Purpose Differential Amplifiers

BENEFITS:

- Low Cost
- High Input Impedance

PRINCIPAL DEVICES

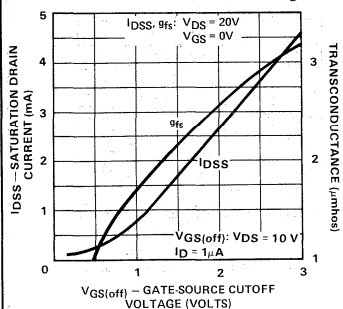
2N3954-55, 2N3954A-55A,
2N3956-58, 2N5045-47,
2N5196-99, 2N5452-37, 2N5515-21
U231-35, U410-12
2N3955, 2N3956-58
2N5047, 2N5199
2N5454, U233-35
U411, 12



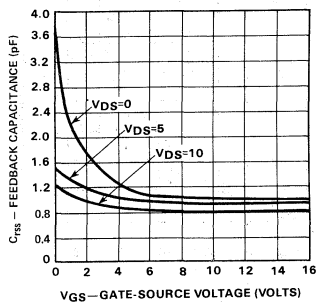
TYPE	PACKAGE
Dual	TO-71
Dual	Chip

PERFORMANCE CURVES (25°C unless otherwise noted)

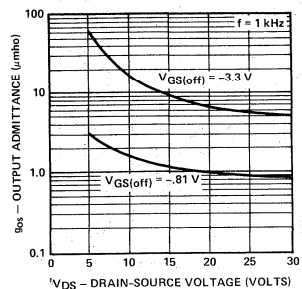
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



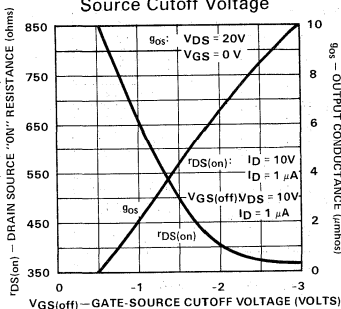
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



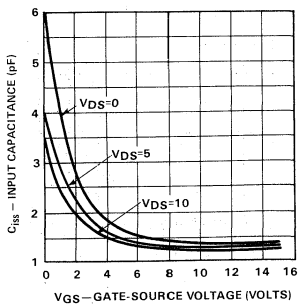
Common Source Output Admittance vs Drain-Source Voltage



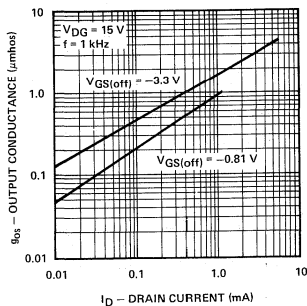
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



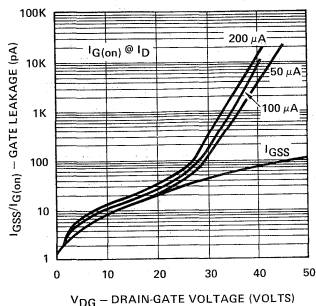
Common Source Input Capacitance vs Gate-Source Voltage



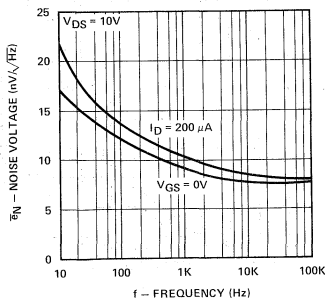
Common-Source Output Conductance vs Drain Current



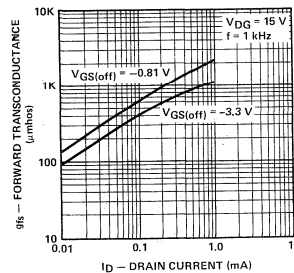
Gate Operating Current vs Drain Current



Equivalent Input Noise Voltage vs Frequency



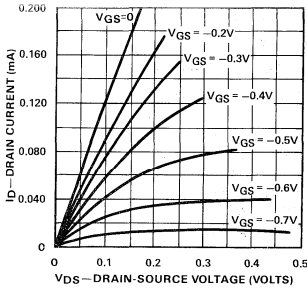
Common Source Forward Transconductance vs Drain Current



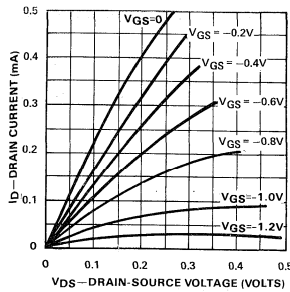
4

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

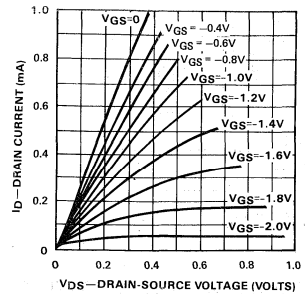
Output Characteristic
($V_{GS(off)} = -1.0V$)



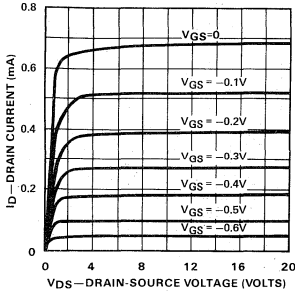
Output Characteristic
($V_{GS(off)} = -1.5V$)



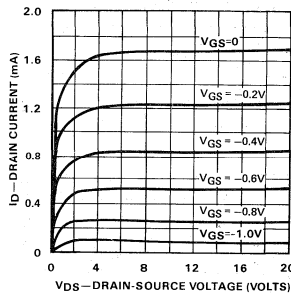
Output Characteristic
($V_{GS(off)} = -2.3V$)



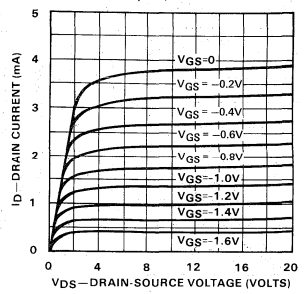
Output Characteristic
($V_{GS(off)} = -1.0V$)



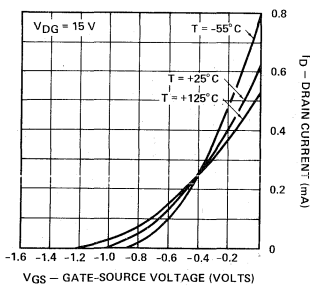
Output Characteristic
($V_{GS(off)} = -1.5V$)



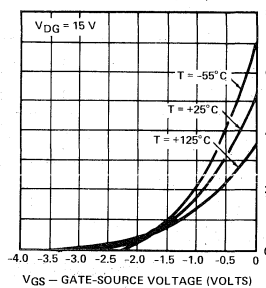
Output Characteristic
($V_{GS(off)} = -2.3V$)



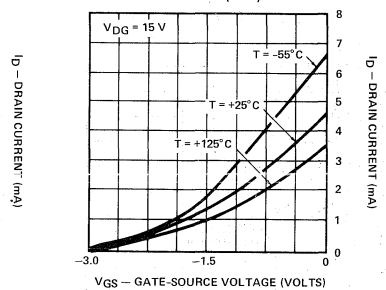
Transfer Characteristics
Low $V_{GS(off)}$



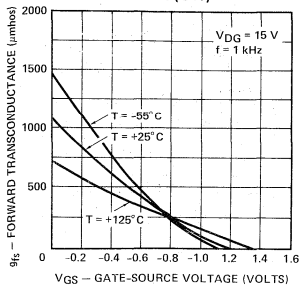
Transfer Characteristics
Medium $V_{GS(off)}$



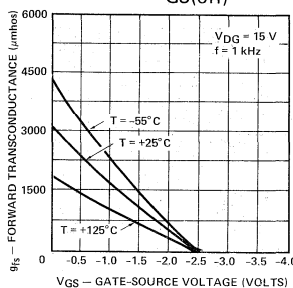
Transfer Characteristics
High $V_{GS(off)}$



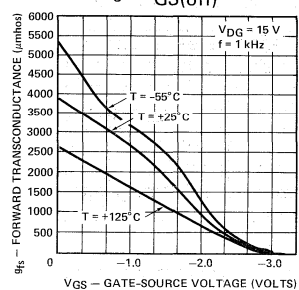
Transconductance Characteristics
Low $V_{GS(off)}$



Transconductance Characteristics
Medium $V_{GS(off)}$



Transconductance Characteristics
High $V_{GS(off)}$





n-channel JFET
designed for . . .

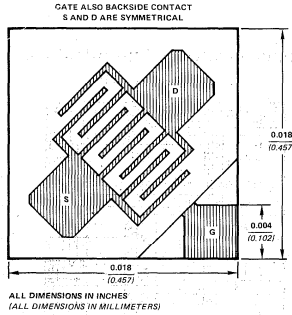
- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

BENEFITS:

- Wide Input Dynamic Range
- High I_G Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

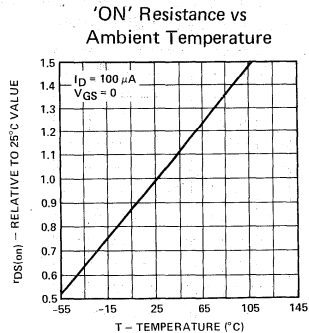
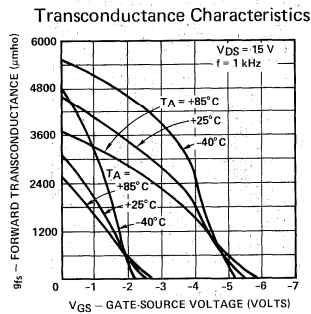
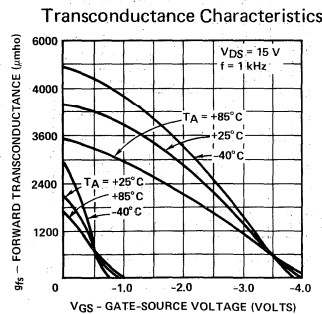
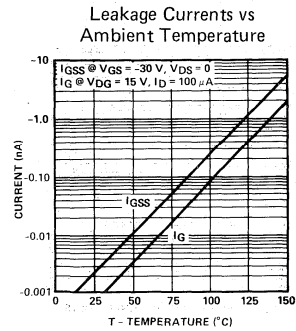
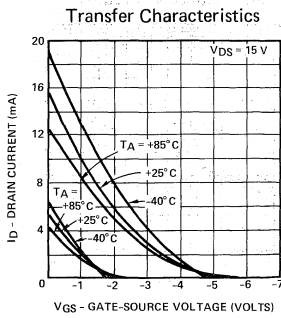
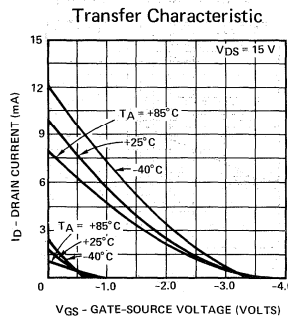
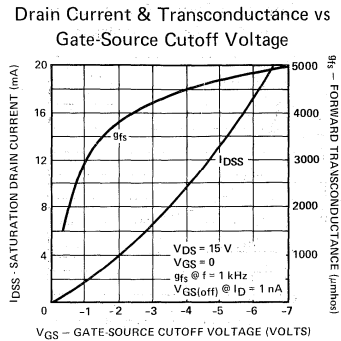
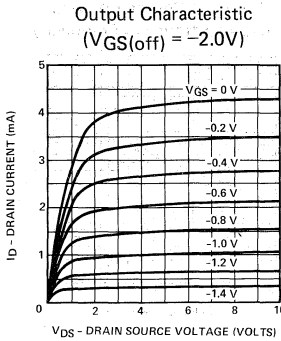
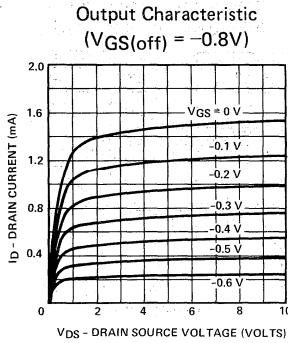
PRINCIPAL DEVICES

- 2N3821-4, 2N3921-22, 2N4220-2
- 2N4220A-2A, 2N4223-24
- 2N3819, 2N5457-9
- MPF109, MPF111
- 2N3819



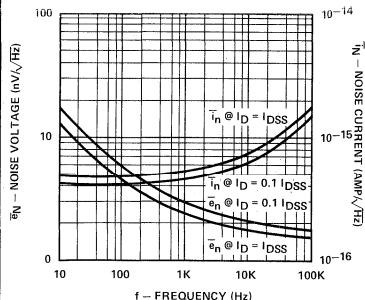
TYPE	PACKAGE
Single	TO-72
Single	TO-92
Dual	TO-71
Single	Chip

PERFORMANCE CURVES (25°C unless otherwise noted)

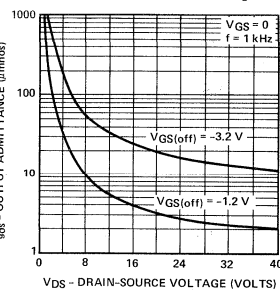


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

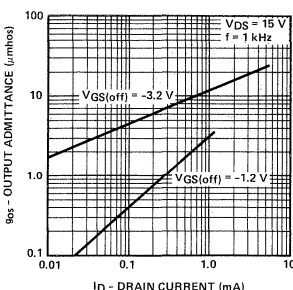
Equivalent Input Noise Voltage and Noise Current vs Frequency



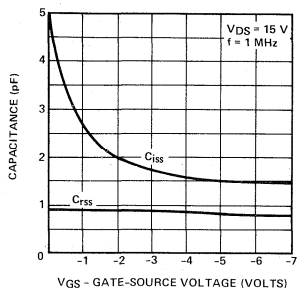
Common-Source Output Admittance vs Drain-Source Voltage



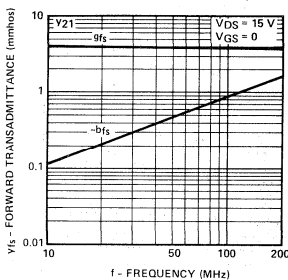
Common-Source Output Admittance vs Drain Current



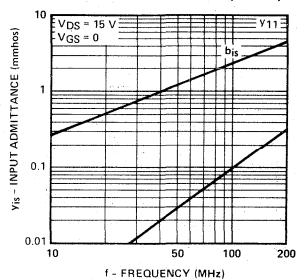
Common-Source Capacitances vs Gate-Source Voltage



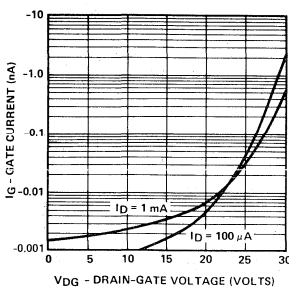
Common-Source Forward Transadmittance vs Frequency



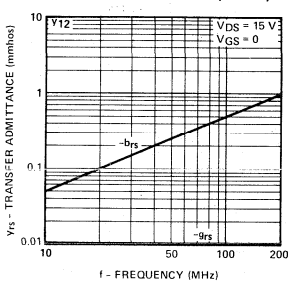
Common-Source Input Admittance vs Frequency



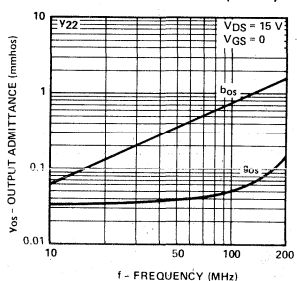
Gate Operating Current vs Drain-Gate Voltage



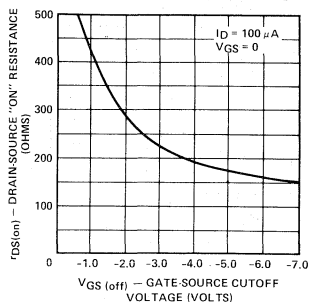
Common-Source Reverse Transfer Admittance vs Frequency



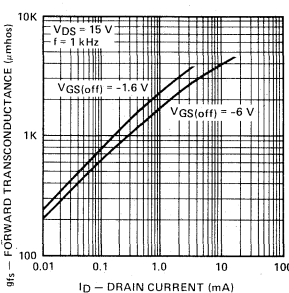
Common-Source Output Admittance vs Frequency



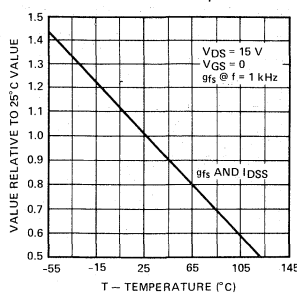
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature





n-channel JFET
designed for . . .

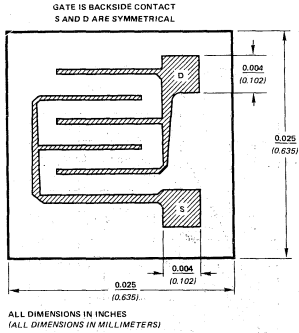
- Low Noise Amplifiers
- Single and Differential Amplifiers

- BENEFITS:**
- Simplifies Amplifier Design
 - Low Output Conductance
 - Low 1/f Noise

TYPE	PACKAGE
Dual	TO-71
Single	TO-72
Single	TO-92
Dual	Chip
Single	Chip

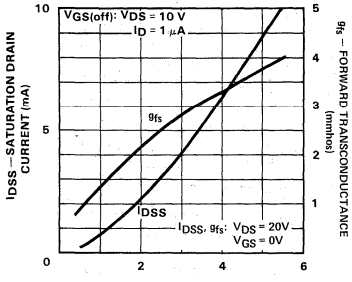
PRINCIPAL DEVICES

2N5515 24
 2N4867-9, 2N4867A-69A
 J230-32
 2N5518CHP-9CHP, 2N5523CHP-4CHP
 All of the above single devices

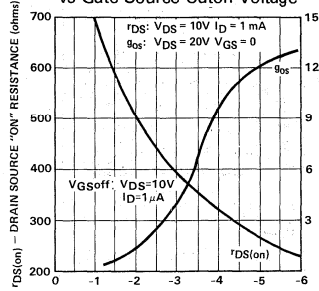


PERFORMANCE CURVES (25°C unless otherwise noted)

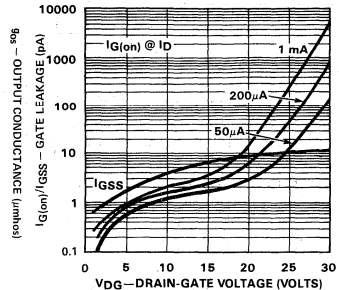
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



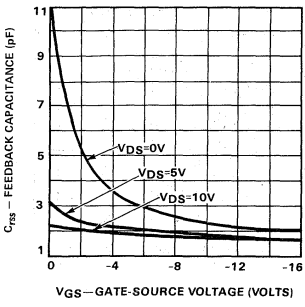
On Resistance and Output Conductance vs Gate Source Cutoff Voltage



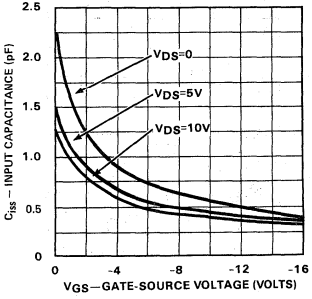
Gate Operating Current vs Drain-Gate Voltage



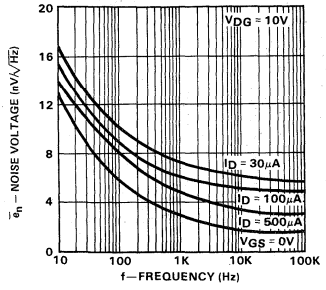
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



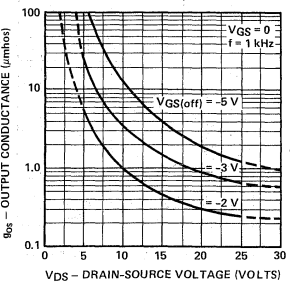
Common Source Input Capacitance vs Gate-Source Voltage



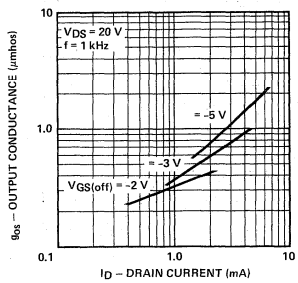
Noise Voltage vs Frequency



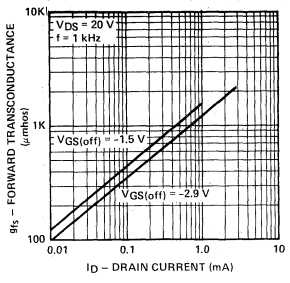
Common-Source Output Conductance vs Drain-Source Voltage



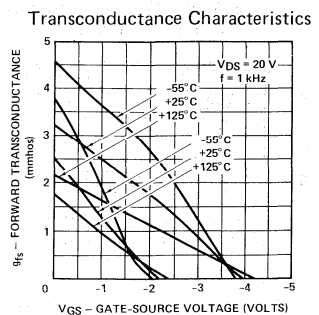
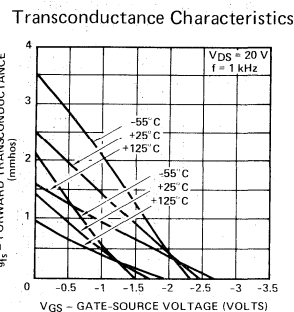
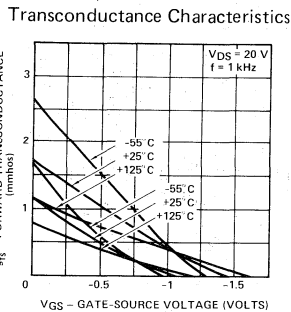
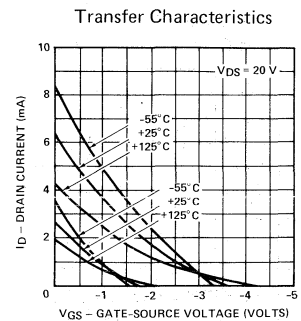
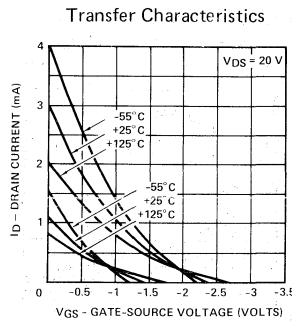
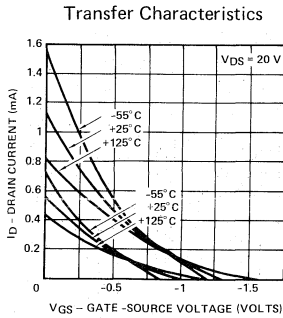
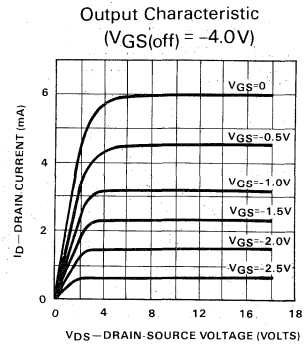
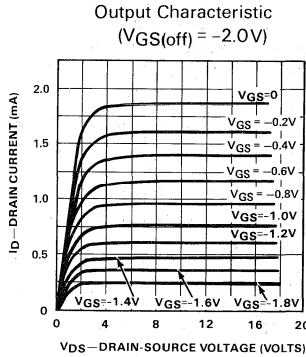
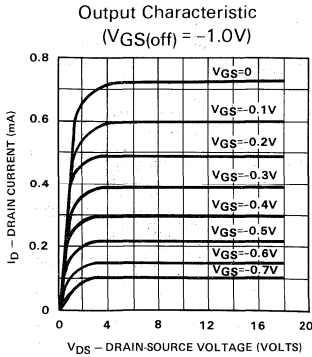
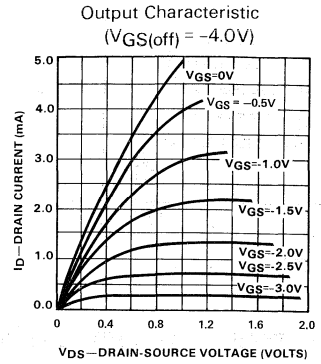
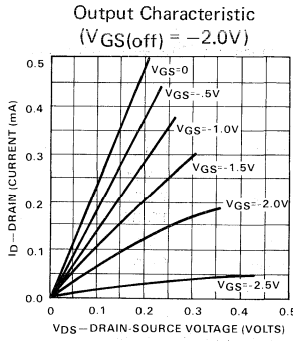
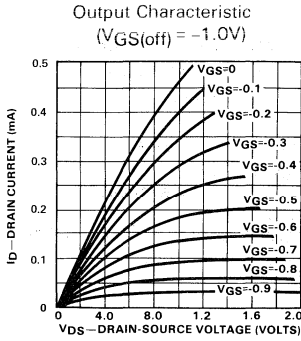
Common-Source Output Conductance vs Drain Current



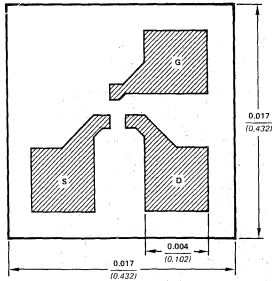
Common-Source Forward Transconductance vs Drain Current



PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)



GATE ALSO BACKSIDE CONTACT
S AND D ARE SYMMETRICAL



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET designed for . . .

- Ultra-High Input Impedance Amplifiers
- Electrometers
- pH Meters
- Smoke Detectors

TYPE	PACKAGE
Single	TO-72
Single	TO-92
Dual	TO-78
Single	Chip

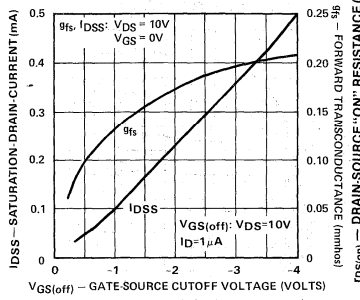


- BENEFITS:**
- Low Power
 $I_{DSS} < 90 \mu A$ (2N4117)
 - High Input Impedance
 $I_G < 1 pA$ (2N5906-09)

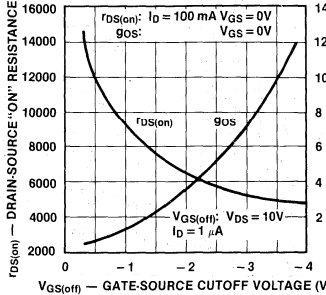
PRINCIPAL DEVICES
 2N4117-9, 2N4117A-9A,
 FN4117 18, FN4117A 18A, VCR7N
 PN4117 Thru PN4120
 PN4117A Thru 4120A
 2N5902-9
 2N4117CHP-9CHP, 2N4117ACHP-9ACHP,
 VCR7NCHP
 PN4117 Thru PN4120
 PN4117A Thru 4120A

PERFORMANCE CURVES (25°C unless otherwise noted)

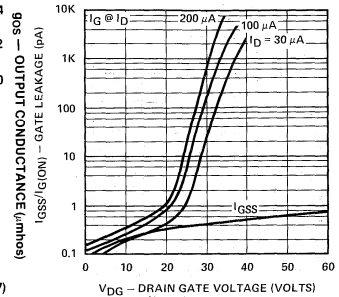
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



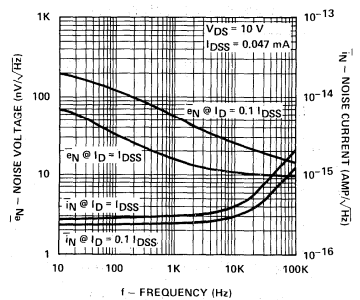
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



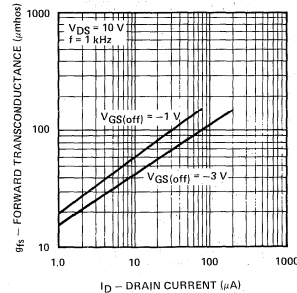
Gate Operating Current vs Drain-Gate Voltage



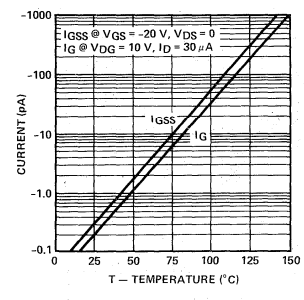
Equivalent Input Noise Voltage and Noise Current vs Frequency



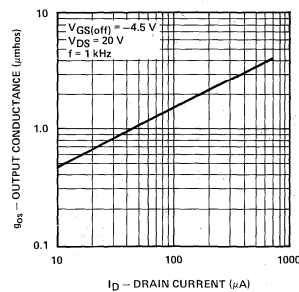
Common-Source Forward Transconductance vs Drain Current



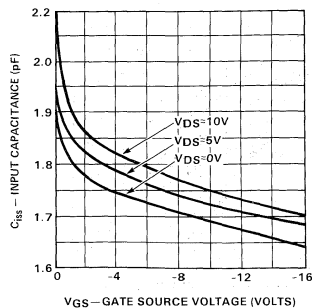
Leakage Currents vs Ambient Temperature



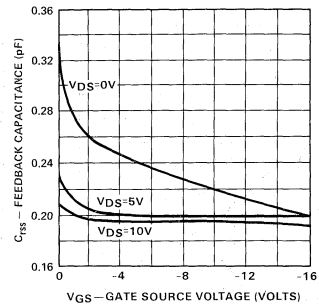
Common-Source Output Conductance vs Drain Current



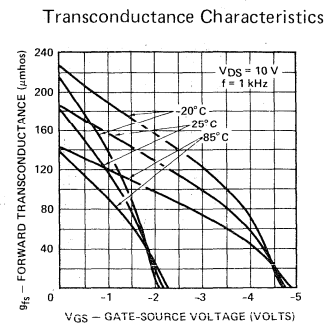
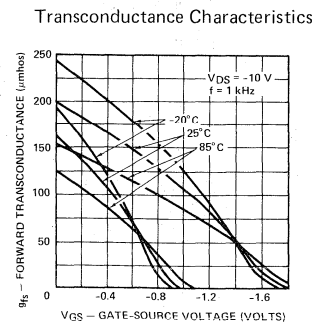
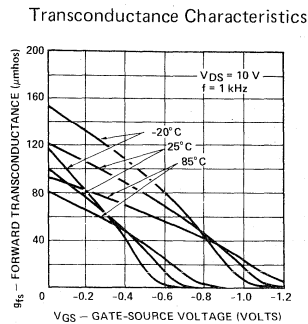
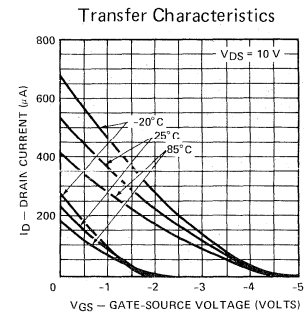
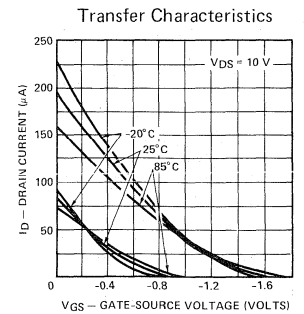
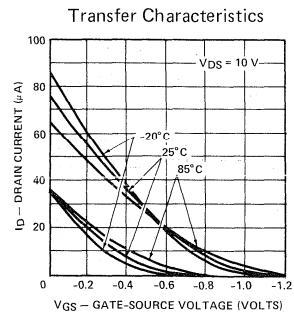
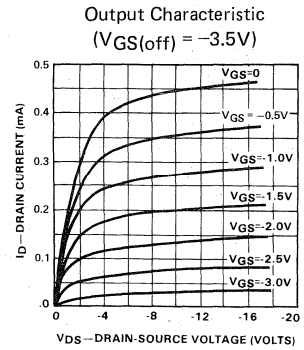
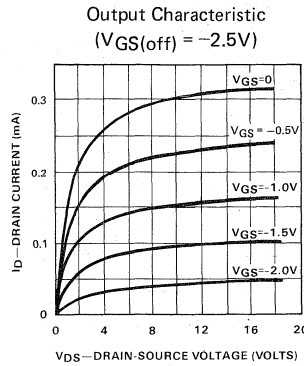
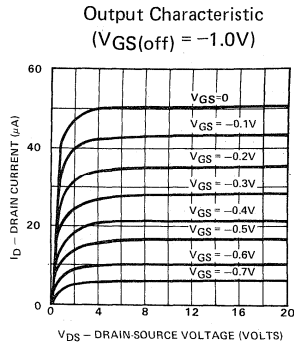
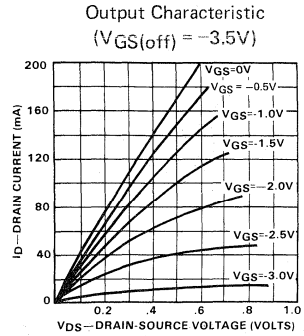
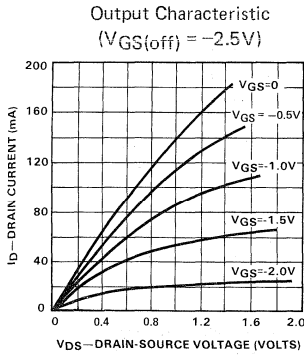
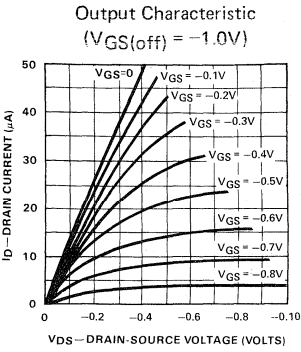
Input Capacitance vs Gate-Source Voltage

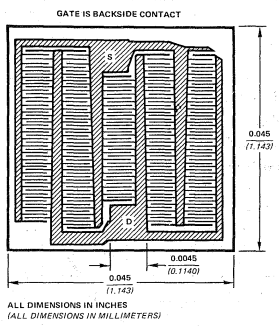


Reverse Feedback Capacitance vs Gate Source Voltage



PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)





n-channel JFET designed for . . .

- Analog Switches
- Commutators
- Choppers

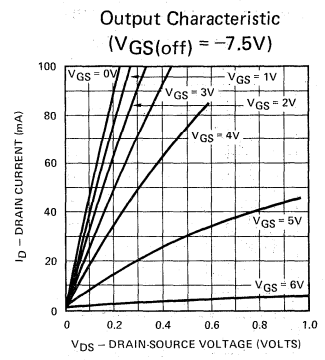
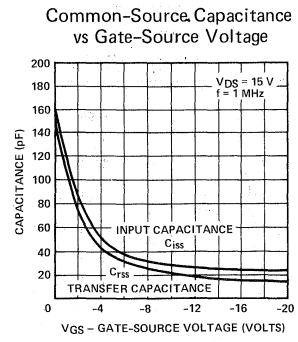
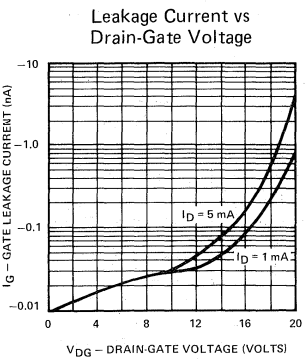
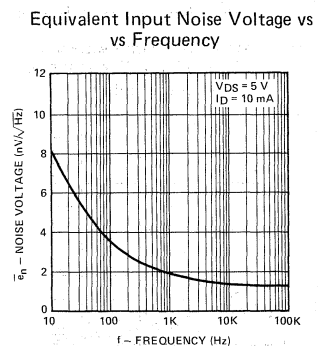
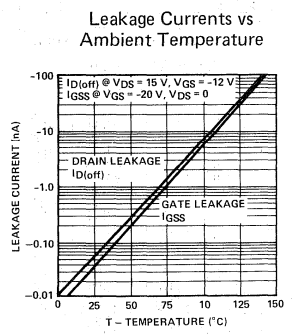
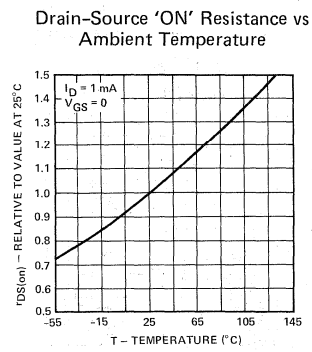
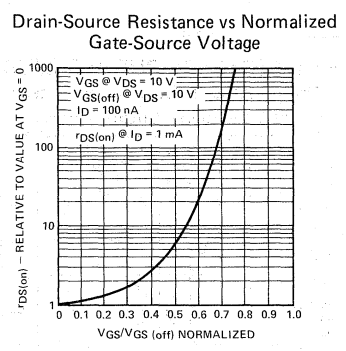
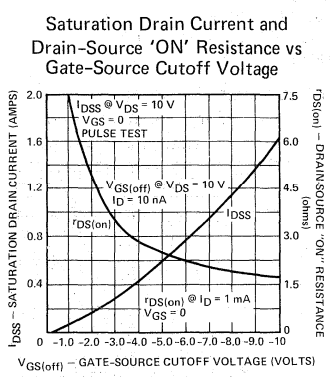
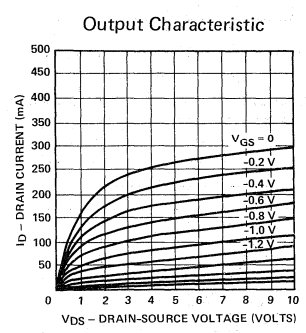
TYPE	PACKAGE
Single	TO-52
Single	TO-92
Single	Chip

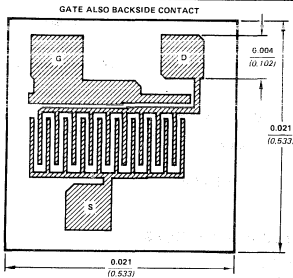
- BENEFITS:**
- Very Low Insertion Loss
 $r_{DS(on)} < 2.5 \text{ Ohms (U290)}$
 - High Off-Isolation

PRINCIPAL DEVICES

U290-1
J105-7
U290CHP-1CHP, J105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)





ALL DIMENSIONS IN INCHES
ALL DIMENSIONS IN MILLIMETERS

TYPE	PACKAGE
Single	TO-52
Single	TO-72
Single	TO-92
Dual	TO-99
Single	Chip
Dual	Chip

n-channel JFET designed for . . .

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

BENEFITS

- Industry Standard
- High Power Gain
16 dB at 100 MHz, Common Gate
11 dB at 450 MHz, Common Gate

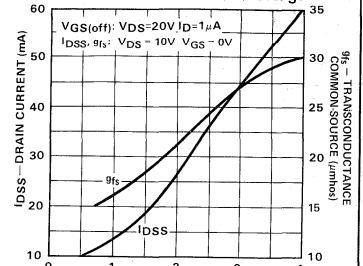
PRINCIPAL DEVICES

- U308-10
- U311
- J308-10
- U430-1
- J308CHP-10CHP,
- U308CHP-10CHP, U311CHP
- U430CHP-1CHP



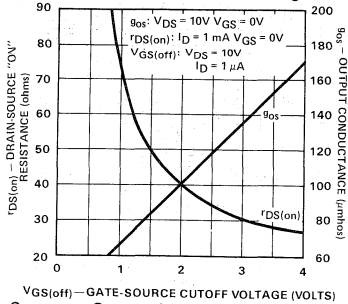
BENEFITS

- Low Noise
3 dB Noise Figure at 450 MHz
- Wide Dynamic Range
Greater Than 100 dB
- 75 Ohm Input Match Common Gate
Drain Current & Transconductance
vs Gate-Source Cutoff Voltage

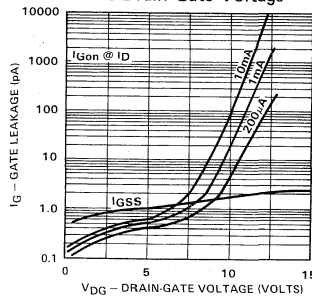


PERFORMANCE CURVES (25°C unless otherwise noted)

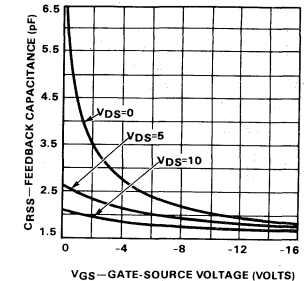
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



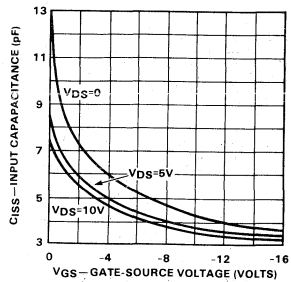
Gate Operating Current vs Drain-Gate Voltage



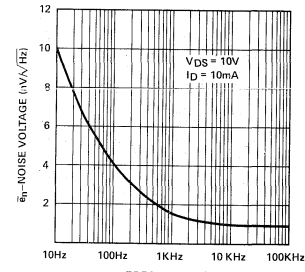
$V_{GS(off)}$ - GATE-SOURCE CUTOFF VOLTAGE (VOLTS)
Common Source Reverse Feedback Capacitance vs Gate Source Voltage



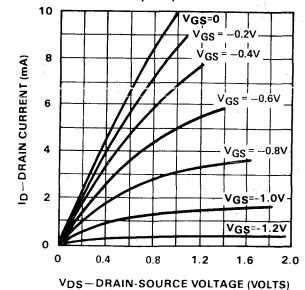
$V_{GS(off)}$ - GATE-SOURCE CUTOFF VOLTAGE (VOLTS)
Common Source Input Capacitance vs Gate-Source Voltage



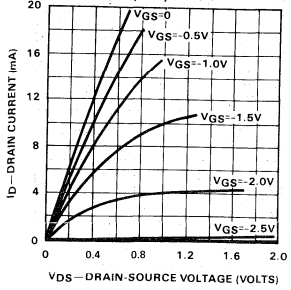
Noise Voltage vs Frequency



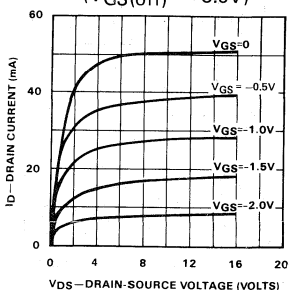
Output Characteristic ($V_{GS(off)} = -1.7V$)



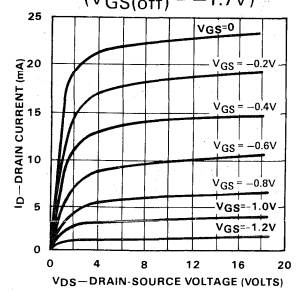
Output Characteristic ($V_{GS(off)} = -3.0V$)



Output Characteristic ($V_{GS(off)} = -3.0V$)

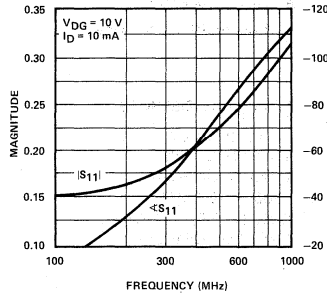


Output Characteristic ($V_{GS(off)} = -1.7V$)

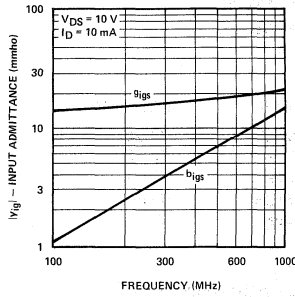


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

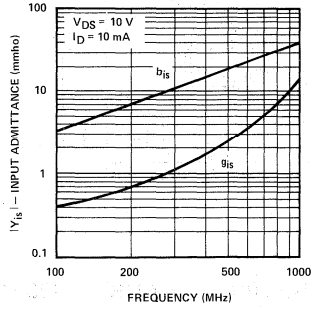
Forward Reflection Coefficient
Common Gate



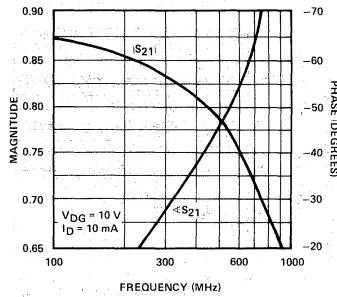
Input Admittance Common Gate



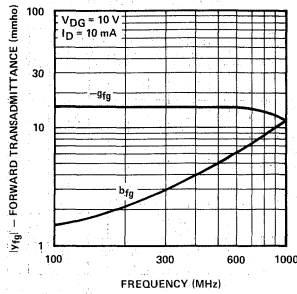
Input Admittance Common Source



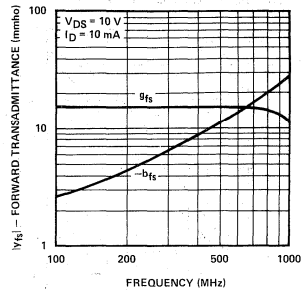
Forward Transmission Coefficient
Common Gate



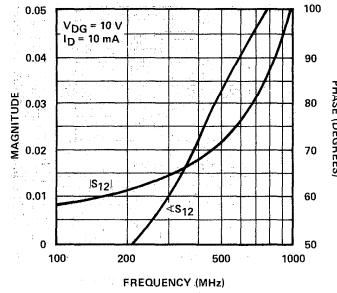
Forward Transfer Admittance
Common Gate



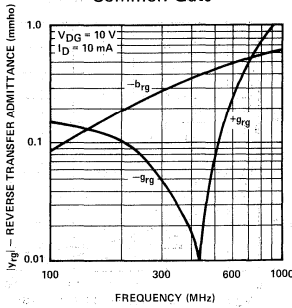
Forward Transfer Admittance
Common Source



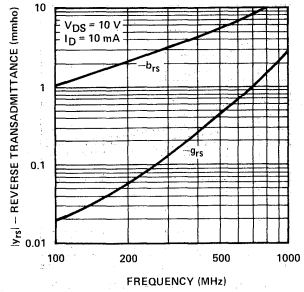
Reverse Transmission Coefficient
Common Gate



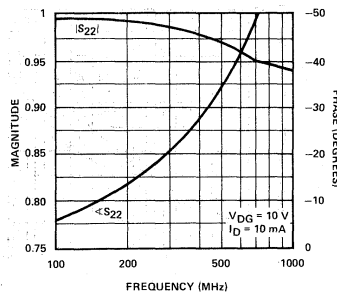
Reverse Transfer Admittance
Common Gate



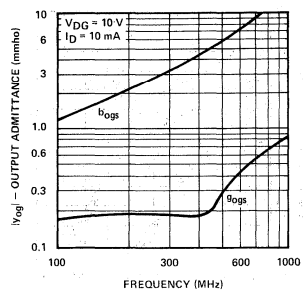
Reverse Transfer Admittance
Common Source



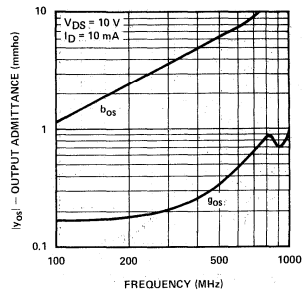
Reverse Reflection Coefficient
Common Gate

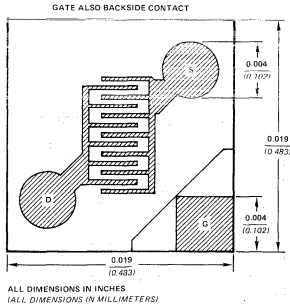


Output Admittance Common Gate



Output Admittance Common Source





n-channel JFET
designed for . . .

- High Frequency Amplifiers
- Mixers
- Oscillators



- BENEFITS:**
- High Power Gain
 - Low Input Capacitance

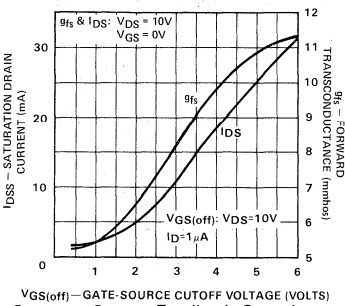
TYPE	PACKAGE
Single	TO-92
Dual	TO-78
Dual	TO-71
Single	Chip
Dual	Chip

PRINCIPAL DEVICES

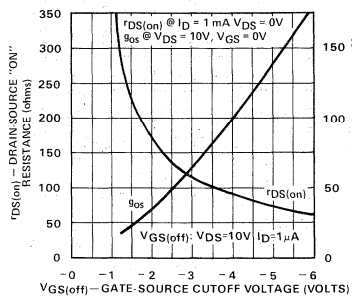
J300, J210-12
 2N5911-12, U257
 U440-41 U443-U444
 J300, J210-2CHP
 2N5912CHP, U257CHP
 U441CHP, U444CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

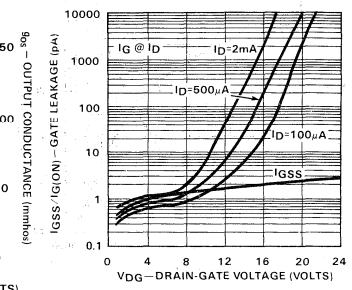
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



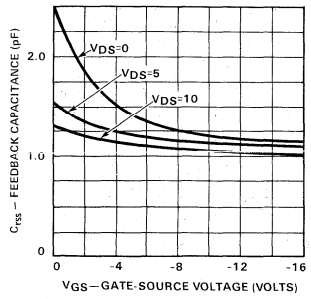
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



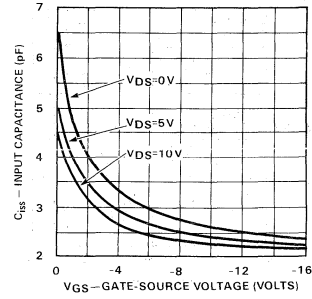
Gate Operating Current vs Drain-Gate Voltage



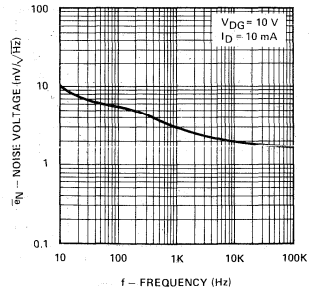
Common Source Feedback Capacitance vs Gate-Source Voltage



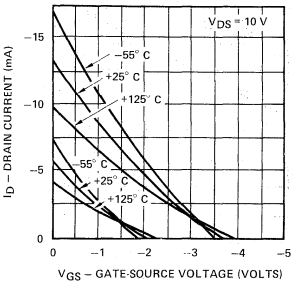
Common Source Input Capacitance vs Gate-Source Voltage



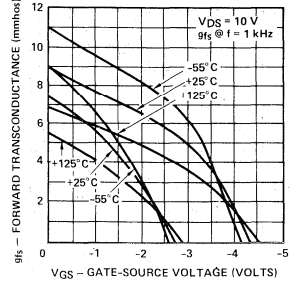
Equivalent Input Noise Voltage vs Frequency



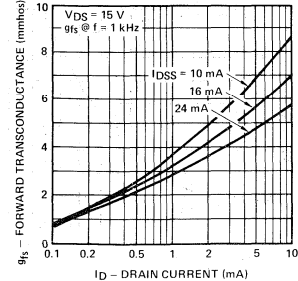
Transfer Characteristics



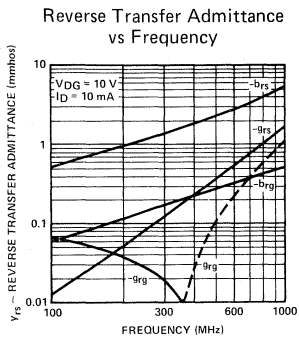
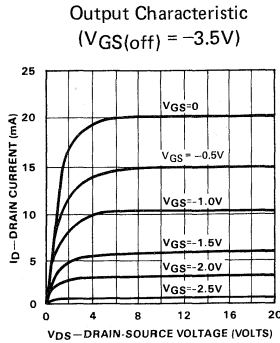
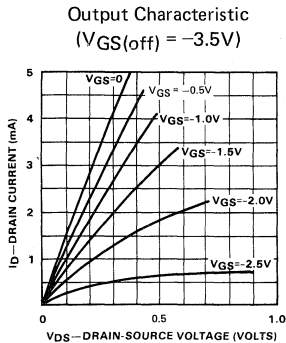
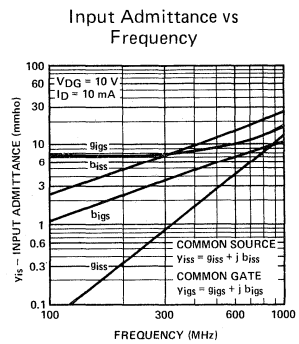
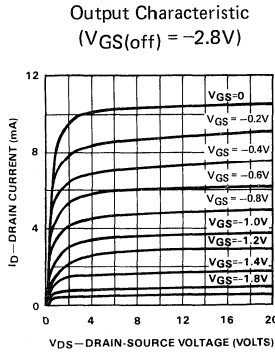
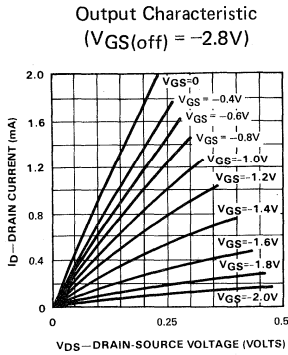
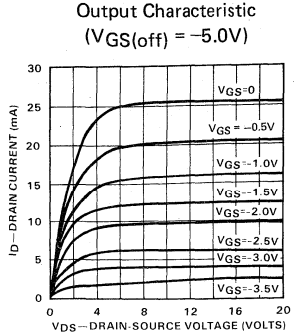
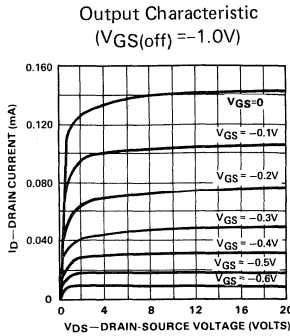
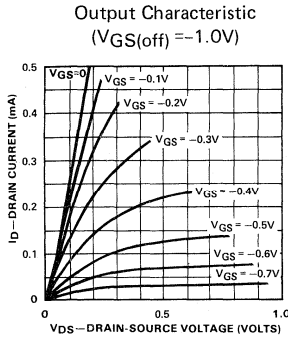
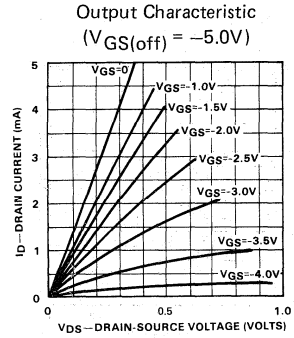
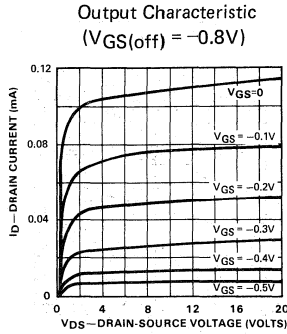
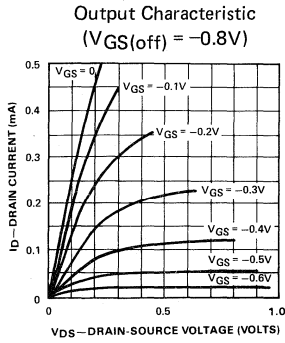
Transconductance Characteristics



Forward Transconductance vs Drain Current

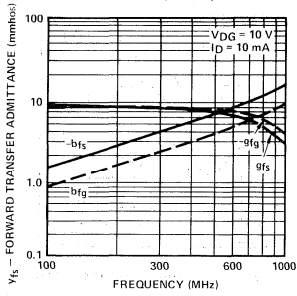


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

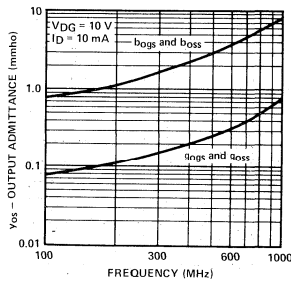


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

Forward Transfer Admittance vs Frequency



Output Admittance vs Frequency



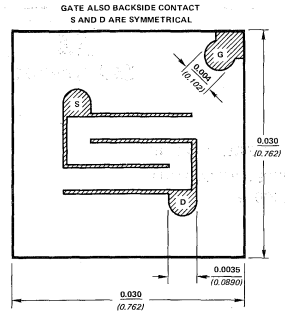


p-channel JFET designed for . . .

- General Purpose Amplifiers and Attenuators

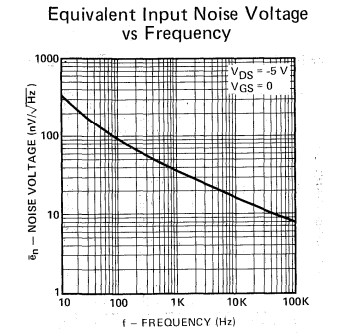
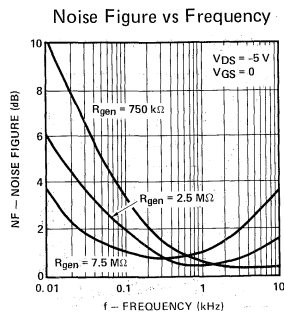
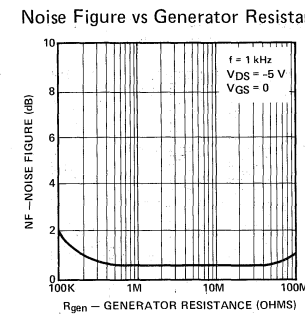
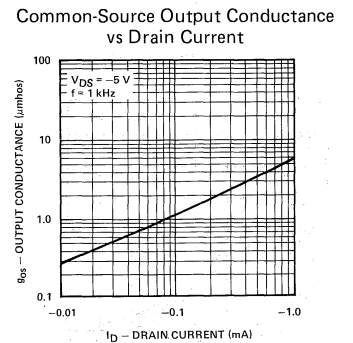
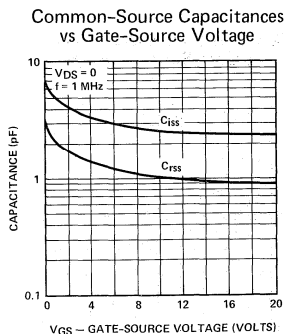
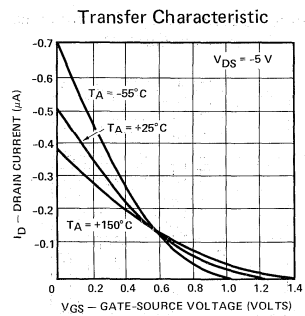
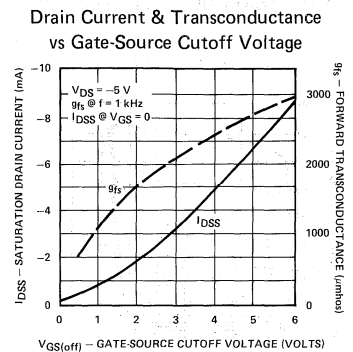
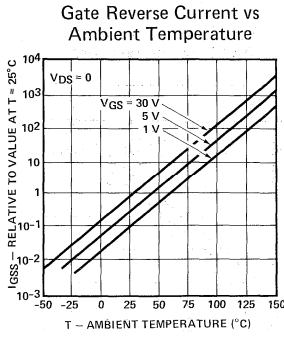
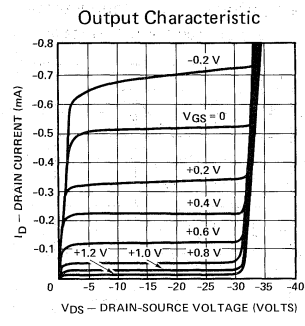
TYPE	PACKAGE
Single	TO-18
Single	TO-72
Single	Chip

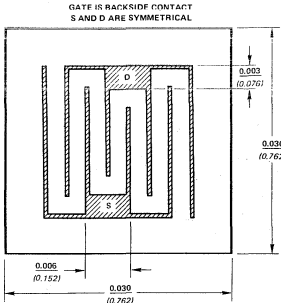
- PRINCIPAL DEVICES**
- 2N2608, 2N2608JAN,
 - 2N3329-32, 2N3909, VCR5P
 - 2N2608CHP,
 - 2N3329CHP-32CHP,
 - VCR5PCHP



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

PERFORMANCE CURVES (25°C unless otherwise noted)





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

p-channel JFET designed for . . .

- General Purpose Amplifiers

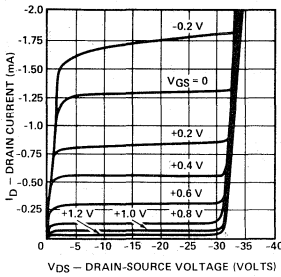
TYPE	PACKAGE
Single	TO-18
Single	Chip



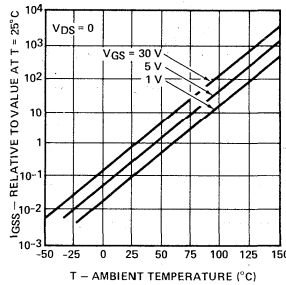
PRINCIPAL DEVICES
2N2609, 2N2609JAN
2N2609CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

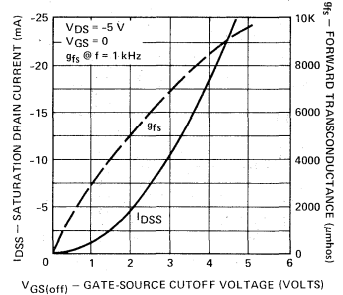
Output Characteristic



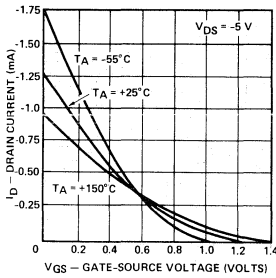
Gate Reverse Current vs Ambient Temperature



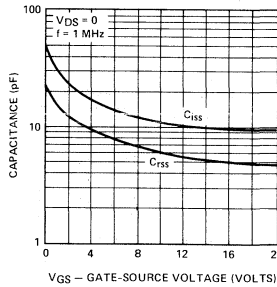
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



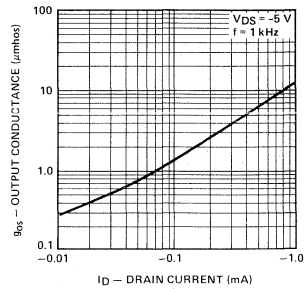
Transfer Characteristic



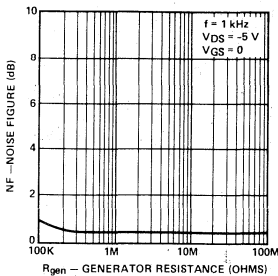
Common-Source Capacitance vs Gate-Source Voltage



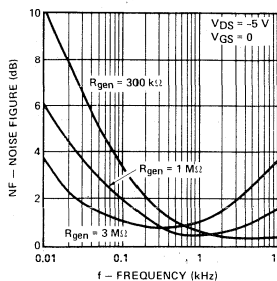
Common-Source Output Conductance vs Drain Current



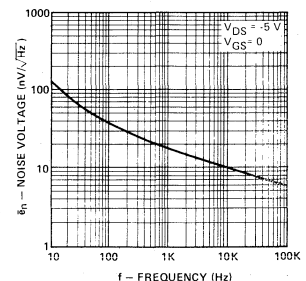
Noise Figure vs Generator Resistance

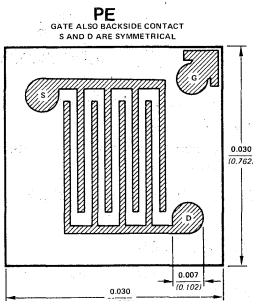


Noise Figure vs Frequency



Equivalent Input Noise Voltage vs Frequency





ALL DIMENSIONS IN INCHES
ALL DIMENSIONS IN MILLIMETERS

p-channel JFET designed for . . .

- General Purpose Amplifiers
- Switches

TYPE
Single
Single
Chip

PACKAGE
TO-72
Chip

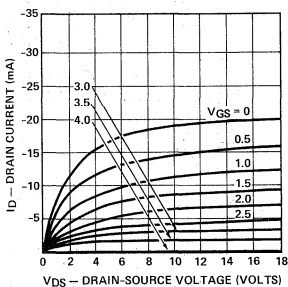


- BENEFITS:**
- Wide Range of Transconductance

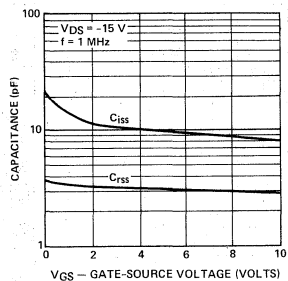
PRINCIPAL DEVICES
2N3382, 2N3384, 2N3386, VCR3P
2N3382CHP-86CHP, VCR3PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

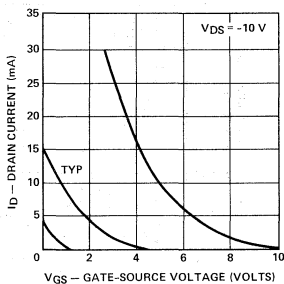
Output Characteristic



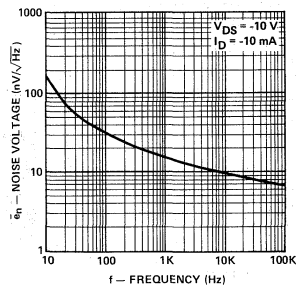
Common-Source Capacitances
vs Gate-Source Voltage



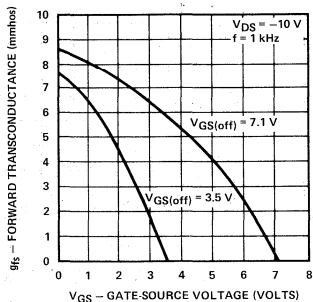
Transfer Characteristics



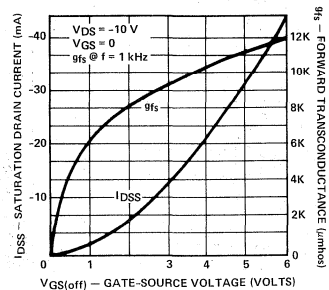
Equivalent Input Noise Voltage
vs Frequency

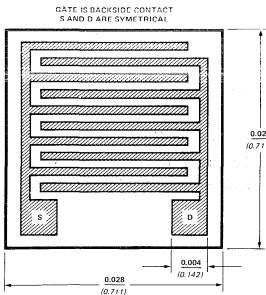


Transconductance Characteristics



Drain Current & Transconductance
vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

p-channel JFET designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

TYPE	PACKAGE
Single	TO-18
Single	TO-92
Single	Chip



BENEFITS:

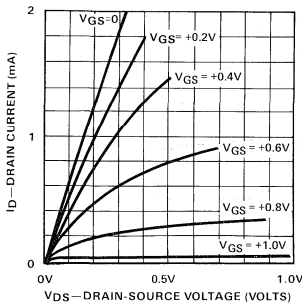
- Low Insertion Loss in Switching Systems
 $R_{ON} < 75 \Omega$ (2N5114)
- Short Sample and Hold Aperture Time
 $C_{RSS} < 7 \text{ pF}$
- High Off-Isolation $I_{D(off)} < 500 \text{ pA}$

PRINCIPAL DEVICES

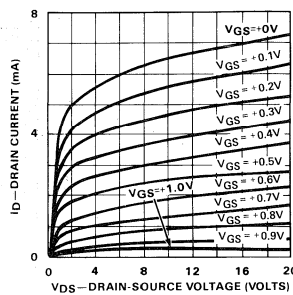
- 2N5018-19, 2N5114-16, U304-6
J174-7, J270-1, P1086-87
2N5018CHP-19CHP, 2N5114CHP-16CHP
U304CHP-6CHP, P1086CHP-87CHP
J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

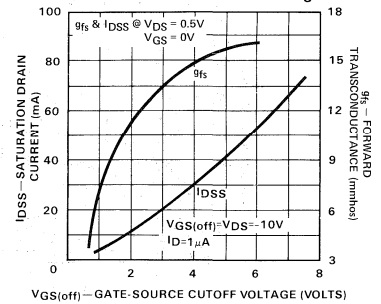
Output Characteristic
($V_{GS(off)} = +1.5\text{V}$)



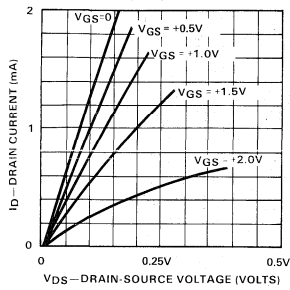
Output Characteristic
($V_{GS(off)} = +1.5\text{V}$)



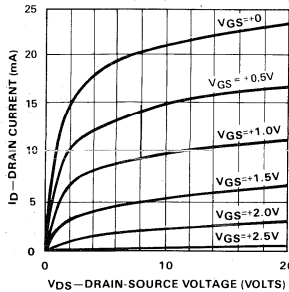
Drain Current & Transconductance
vs Gate-Source Cutoff Voltage



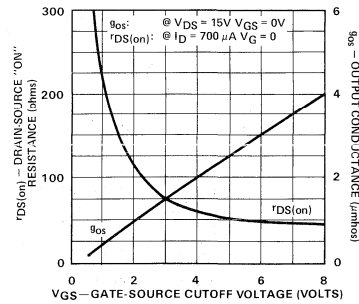
Output Characteristic
($V_{GS(off)} = +3.0\text{V}$)



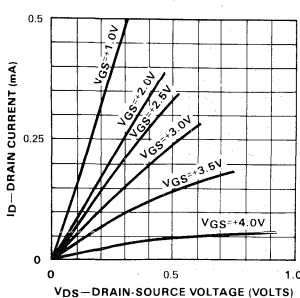
Output Characteristic
($V_{GS(off)} = +3.0\text{V}$)



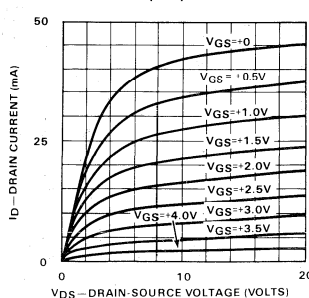
On Resistance and Output
Conductance vs Gate-Source
Voltage



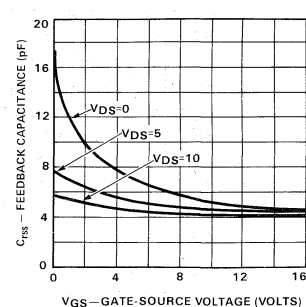
Output Characteristic
($V_{GS(off)} = +5.0\text{V}$)



Output Characteristic
($V_{GS(off)} = +5.0\text{V}$)

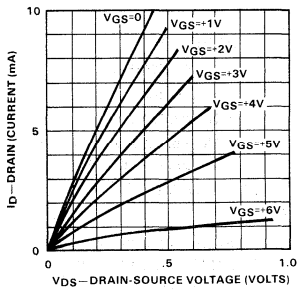


Common Source Reverse
Feedback Capacitance
vs Gate Source Voltage

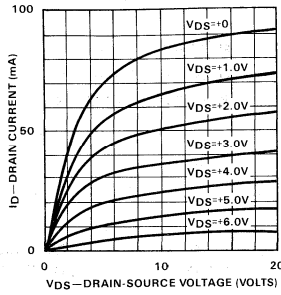


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

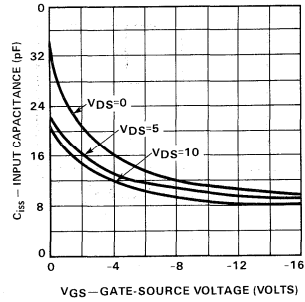
Output Characteristic (VGS(off) = +8.0V)



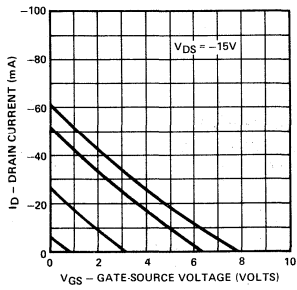
Output Characteristic (VGS(off) = +8.0V)



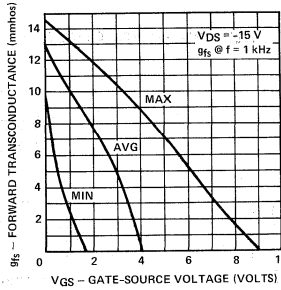
Common Source Input Capacitance vs Gate-Source Voltage



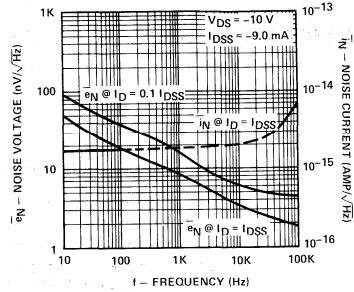
Transfer Characteristics

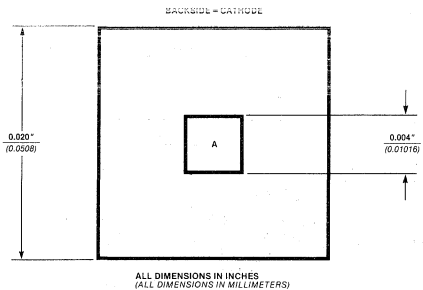


Transconductance Characteristics



Equivalent Input Noise Voltage and Noise Current vs Frequency





high voltage protection diode designed for . . .

- Limiting Current
- Voltage Protection
- Voltage Decoupling

BENEFITS

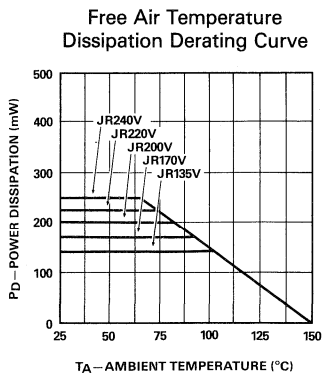
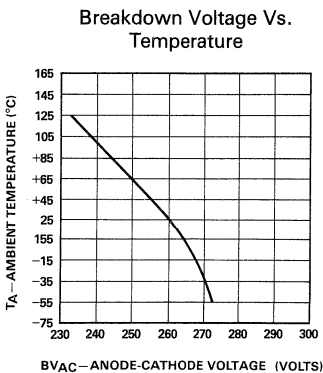
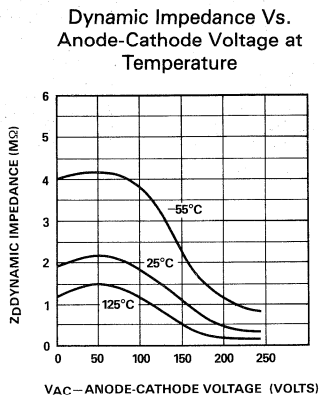
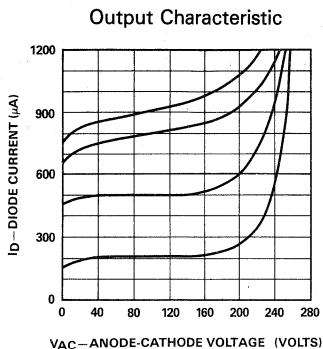
- Series element
- Two terminals
- Simple to use
- High breakdown voltage (JR240V – 240 volts)
- Low Cost

TYPE
Single

PACKAGE
TO-92

PRINCIPAL DEVICES
JR135V, JR170V, JR200V
JR220V, JR240V

PERFORMANCE CURVES (25°C unless otherwise specified)



Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

APPLICATION NOTE

An Introduction to FETs

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilienfeld's patent of 1925. The theoretical description of a FET made by Shockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

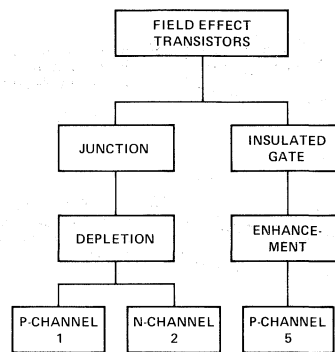
- | | | |
|-------------------|-----------------|---------------------------|
| <i>Amplifiers</i> | <i>Switches</i> | <i>Current Limiters</i> |
| Small Signal | Chopper-type | <i>Voltage-Controlled</i> |
| Low Distortion | Analog Gate | <i>Resistors</i> |
| High Gain | Commutator | <i>Mixers</i> |
| Low Noise | | <i>Oscillators</i> |
| Selective | | |
| D.C. | | |
| High-Frequency | | |

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics — which are very different from those of bipolar devices — can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits.

In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils; this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

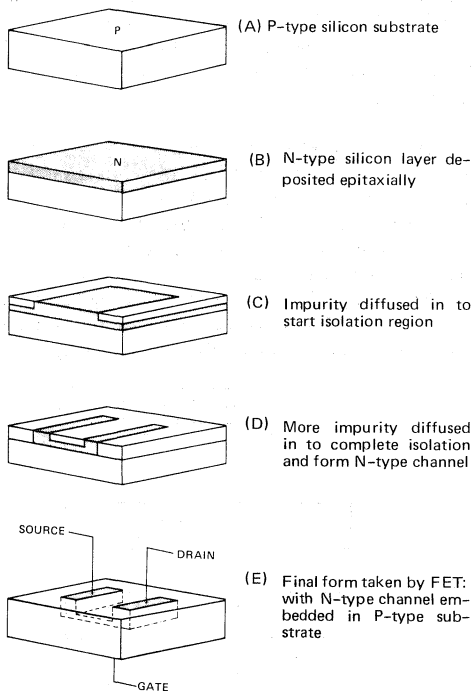


FET Family Tree
Figure 1

Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited



Idealized Manufacture of an N-Channel Junction FET
Figure 2

epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off*. The physical meaning of this term leads to one definition of *pinch-off voltage*, V_p , which is the value of V_{DS} at which the maximum I_{DSS} flows.

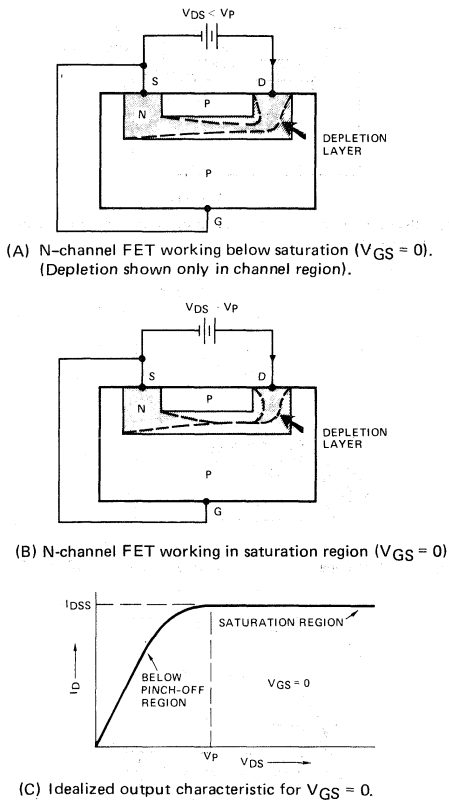
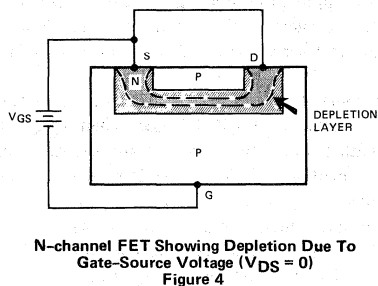


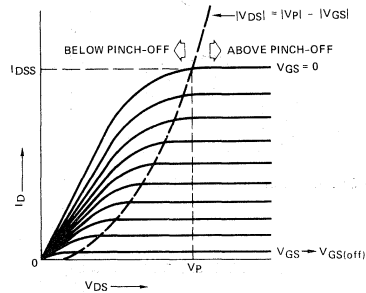
Figure 3

In Figure 4, consider the case where $V_{DS} = 0$, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for $V_{GS} = 0$. In fact, at a value of $|V_{GS}| \geq |V_p|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_p or by $V_{GS(off)}$. V_p has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_p , strictly speaking, are equal in magnitude but opposite in polarity.



The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D .

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS} . Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET

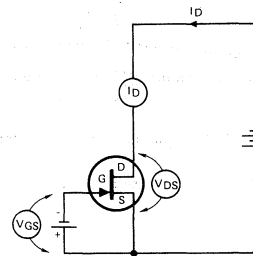
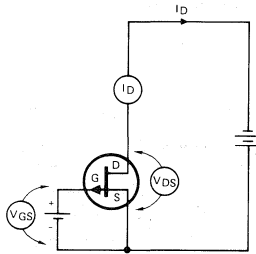


Figure 5

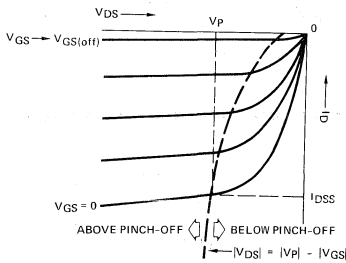
The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type chan-

nel. In the P-channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS} . When V_{DS} is greater than V_p , the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

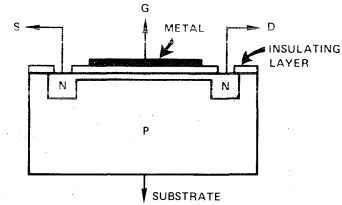


(B) Family of output characteristics for P-channel FET

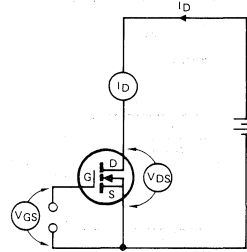
Figure 6

MOSFETs

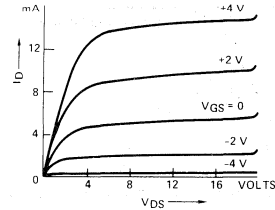
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the 2N3631 N-channel depletion MOSFET

Figure 7

in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.

Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS} . This mode of operation is represented by the higher members of the family of output characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons — thus reducing I_D — the device just described is called a *depletion-mode* MOSFET.

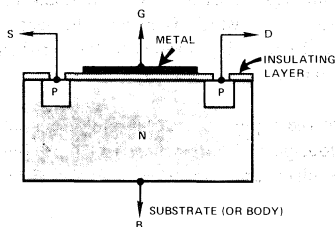
The foregoing has established that the depletion-mode MOSFET is a “normally-ON” device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a “normally-OFF” device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

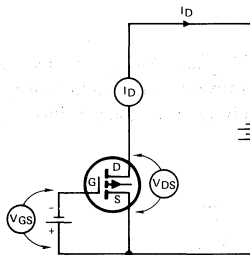
If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is

applied, then current, I_D , will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

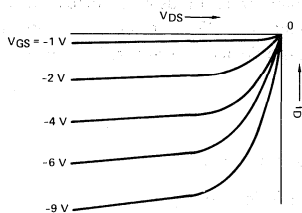
Different values of V_{GS} give rise to limiting values of I_D , so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.



(A) Idealized cross-section through a P-channel enhancement MOSFET

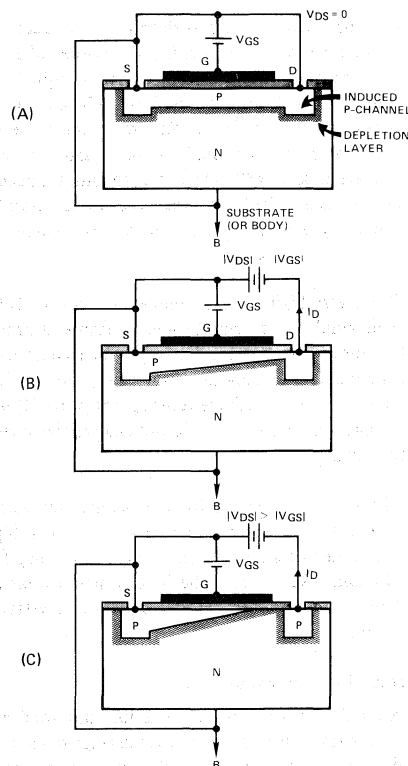


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off, (A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to $10^{12} \Omega$. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be $22K \Omega$ at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters — in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} — Drain current with the gate shorted to the source
- $V_{GS(off)}$ — Gate-source cutoff voltage
- I_{GSS} — Gate-to-source current with the drain shorted to the source
- BV_{GSS} — Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} — Common-source forward transconductance
- C_{gs} — Gate-source capacitance
- C_{gd} — Gate-drain capacitance

Special attention should be given to the subscript “s” because it has two different meanings and three possible uses. In FET notations, an “s” for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an “s” for the third subscript does not refer to the FET source terminal. It is an abbreviation for “shorted”, and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11} V_{11} + Y_{21} V_{22} \quad (1)$$

When Y_{11} , Y_{21} , Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$i_1 = y_i v_{11} + y_r v_{22} \quad (2)$$

$$i_2 = y_f v_{11} + y_o v_{22}$$

For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

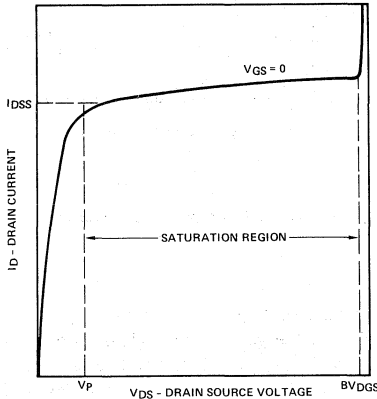
$$i_i = y_{is} v_{gs} + y_{rs} v_{ds} \quad (3)$$

$$i_o = y_{fs} v_{gs} + y_{os} v_{ds}$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

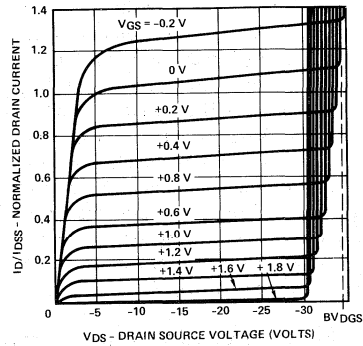
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

- ρ = resistivity
- L = length of the channel
- $A = W \times T$ = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS} , the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS} , approaches infinity. As earlier noted, this condition is referred to as “pinch-off” or “cutoff” because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D . Accordingly, the pinch-off region is also referred to as the pentode or “constant-current” region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D , with increases in V_{GS} resulting in lower values of constant I_D , and smaller values of V_{DS} necessary to reach the “knee” of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS} .



FET I_D vs V_D Output Characteristics
Figure 11

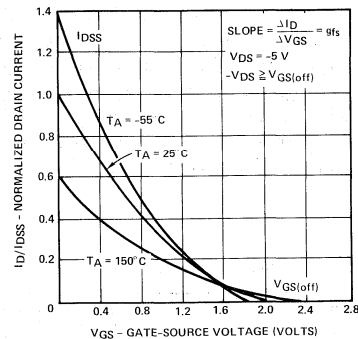
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P , defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P . Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P . However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

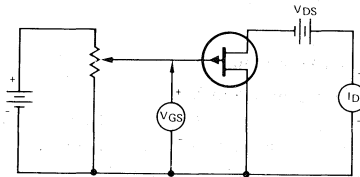
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \tag{4}$$



Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS} , V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS} , the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS} , the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS} . Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I
Typical Pinch-Off Voltage Specification

Characteristic	Min	Max	Units
$V_{GS(off)}$ Gate-source pinch-off voltage of: $V_{DS} = -5 \text{ V}$, $I_D = -1 \mu\text{A}$	1	4	Volts

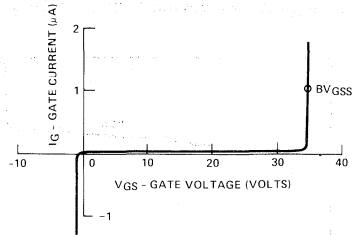
Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off) (min)}$ is to be specified.

Table II
Indication of Maximum V_p

Characteristic	Test Conditions	Min	Max	Unit
$I_{D(off)}$ Pinch-off drain current	$V_{DS} = -12 \text{ V}$, $V_{GS} = 8 \text{ V}$		-10	μA

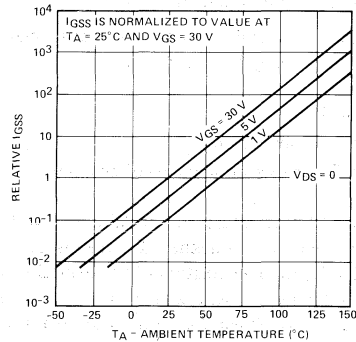
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω . The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS} .



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO} , I_{GSO} , and the combined measurement I_{GSS} . These measurement circuits are shown in Figure 16.

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO} .

In a circuit, V_{GD} may be biased between zero and BV_{GDS} , while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS} .

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also pos-

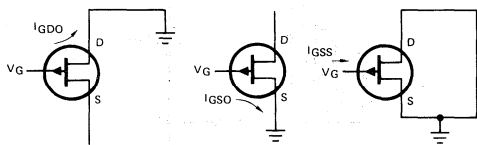
sible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1 . A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n , in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

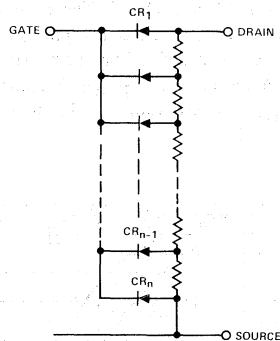
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

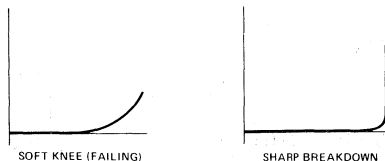
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17



Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

g_{fs} - Transconductance

Transconductance, g_{fs} , is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, V_{DS} = \text{constant} \quad (5)$$

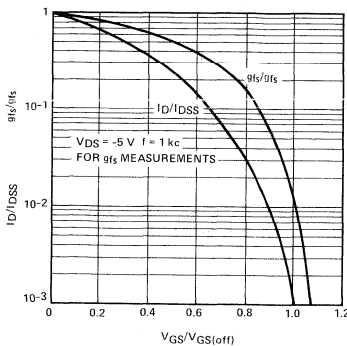
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso} \left(1 - \frac{V_{GS}}{V_{GS(OFF)}} \right) \quad (6)$$

$$g_{fso} = - \frac{2I_{DSS}}{V_{GS(OFF)}} \quad (7)$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(OFF)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until $V_{GS(OFF)}$ is approached. For these curves, $V_{GS(OFF)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_{D/triode} = I_{DSS} \left(\frac{V_{DS}}{V_{GS(OFF)}} \right)^{1/2} \quad (8)$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

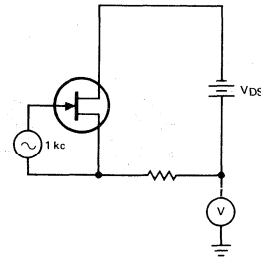
Table III (2N3823)

Characteristic	Test Conditions	Min	Max	Unit
g_{fs} Small-signal common-source forward transconductance	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ kHz}$	3,500	6,500	μmho

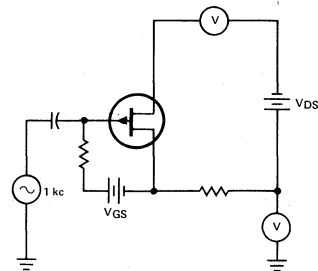
Table IV (2N3329)

Characteristic	Test Conditions	Min	Max	Unit
Y_{fs} Common-source forward transfer admittance	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$, $f = 1 \text{ kHz}$		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (-1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS} . Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with $V_{GS} = 0$
Figure 20



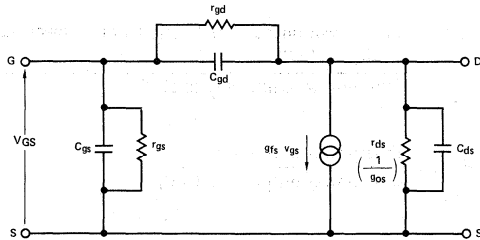
Test Circuit for g_{fs} with I_D Specified
Figure 21

Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS} . Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd} , exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds} , also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS} , V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the $-2.2 \text{ mV}/^\circ\text{C}$ change in junction potential difference.

Assuming that the FET is properly biased — that is, that the d-c conditions are met by the external circuitry — it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



NOTE: $C_{gss} = C_{iss} = C_{gs} + C_{gd}$
 $C_{oss} = C_{gd} + C_{ds} \cong C_{gd} = C_{rss}$

Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs} , is shunted by a very large input resistance, r_{gs} , with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd} . (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} — which stems from the header material — is shunted by the incremental channel resistance, r_{ds} . This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs} , multiplied by the incremental gate voltage. For the small signal, v_{gs} , this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a “positive” direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} and r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd} .

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \cong C_{gd} \tag{10}$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss} , which refers to the “reverse” capacitance.

In data sheets, it is customary to state $(= C_{iss}) C_{gss}$ and $C_{dss} (= C_{oss})$. C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$. Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd} , as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix J202 N-channel FET. They are given as

$$C_{iss} \text{ (at } V_{DS} = 20 \text{ V and } f = 1 \text{ MHz)} = 5 \text{ pF max.}$$

and

$$C_{rss} \text{ (at } V_{DS} = 20 \text{ V and } F = 1 \text{ MHz)} = 2 \text{ pF max.}$$

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, $C_{gs} = 5 - 2 = 3 \text{ pF}$ maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

APPLICATION NOTE

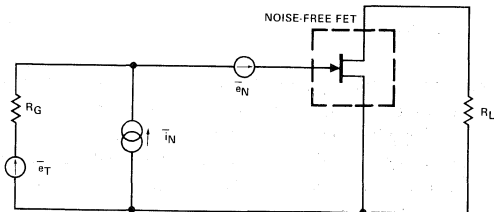
Audio-Frequency Noise Characteristics of Junction FETs

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, e_N and i_N . These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise

factor, a source resistor R_G , with a thermal noise voltage e_T , is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is⁽¹⁾

$$e_T = \sqrt{4kTR_GB} \quad (1)$$

where $k = 1.380 \times 10^{-23}$ Joules/ $^{\circ}$ K (Boltzmann's Constant), T = temperature in $^{\circ}$ K, and B = bandwidth in Hz. Therefore noise power due to R_G is

$$\frac{e_T^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \quad (2)$$

The noise power of the FET referred to the input is

$$\frac{\bar{e}_N^2}{R_G} + i_N^2 \cdot R_G \quad (3)$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_{GB}} \quad (4)$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G :

$$NF = 10 \log_{10} [F] \quad (5)$$

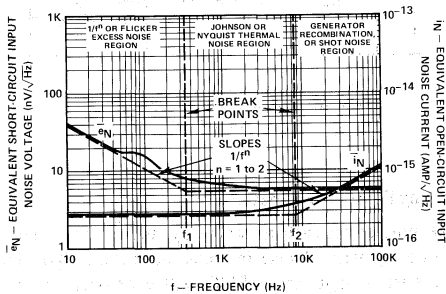
The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_{GB}} \right] \text{ dB} \quad (6)$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance, R_G . Therefore, the \bar{e}_N, \bar{i}_N method remains as the best way to quantitatively express the noise characteristics of the FET itself.

Describing Junction FET Noise Characteristics

Junction FET \bar{e}_N and \bar{i}_N characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise
Figure 2

\bar{e}_N , the equivalent short circuit input noise voltage (with the exception of the $1/f^n$ region), is defined as⁽²⁾

$$\bar{e}_N = \sqrt{4kTR_{NB}} \quad (7)$$

where $R_{NB} \cong 0.67/g_{fs}$, the equivalent resistance for noise. The \bar{e}_N , except in the $1/f^n$ region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called $1/f^n$ region, \bar{e}_N is expressed as

$$\bar{e}_N = \sqrt{4KR_{NB}(1 + f_1/f^n)} \quad (8)$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in \bar{e}_N in the $1/f^n$ region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), \bar{e}_N is inversely proportional to the square root of the transconductance of the FET ($\bar{e}_N \propto 1/\sqrt{g_{fs}}$). \bar{e}_N can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \quad (9)$$

let

$$\bar{e}_{N1} = \bar{e}_{N2} \quad (10)$$

and let

$$g_{fs1} = g_{fs2} \quad (11)$$

Thus,

$$g_{fs \text{ TOTAL}} = 2 g_{fs1} \text{ or } 2 g_{fs2} \quad (12)$$

From Equation (7)

$$\bar{e}_{N1} = \sqrt{4kT(0.67/g_{fs1})B} \quad (13)$$

and

$$\bar{e}_{N \text{ TOTAL}} = \sqrt{4kT(0.67/2g_{fs1})B} \quad (14)$$

Thus,

$$\bar{e}_{N \text{ TOTAL}} = \frac{1}{\sqrt{2}} \bar{e}_{N1} \quad (15)$$

A second way to achieve low \bar{e}_N is to use a device with a large gate area. Empirically, \bar{e}_N is inversely proportional to the square of the gate area ($\bar{e}_N \propto 1/A_G^2$), independent of g_{fs} . This large gate area philosophy has been followed in the

design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that \bar{e}_N is significantly lowered and \bar{i}_N also remains at a low value.

The equivalent open-circuit input noise current, \bar{i}_N , with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\bar{i}_N = \sqrt{2qI_G B} \quad (16)$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured DC operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, \bar{i}_N can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:⁽³⁾

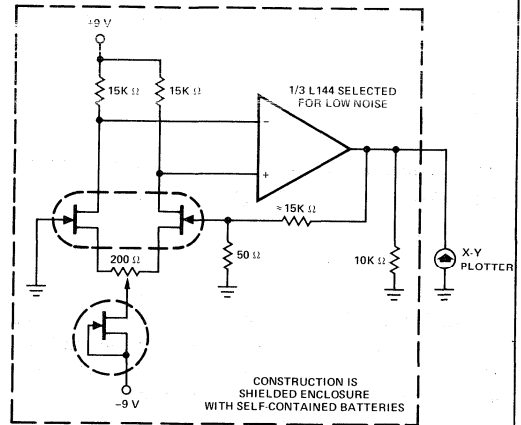
$$\bar{i}_N = \sqrt{\frac{4kTB}{R_p}} \quad (17)$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

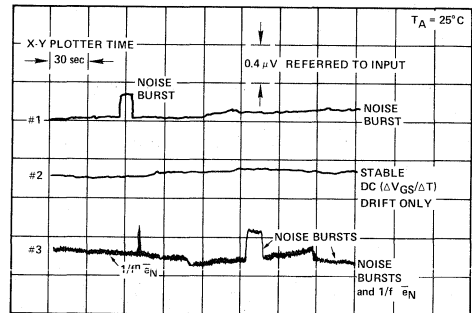
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between $1/f^{1/2}$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^{1/2}$ noise voltage (\bar{e}_N) is masked and difficult to evaluate at 10 Hz.



Test Circuit to Measure Popcorn Noise
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



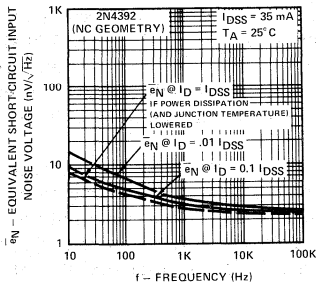
Popcorn Noise in Differential Amplifiers
Figure 4

Operating Point Considerations

Unlike bipolar transistors, where \bar{e}_N and \bar{i}_N characteristics vary directly with change in collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

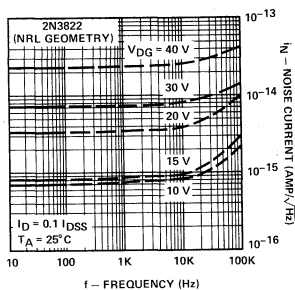
The \bar{e}_N in junction FETs will be lowest when the devices are operated at $V_{GS} = 0$ ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

The curves in Figure 5 illustrate changes in \bar{e}_N as the operating drain current (I_D) is varied. Note that the lowest \bar{e}_N did not occur at $V_{GS} = 0$, because of high power dissipation and a resultant rise in junction temperature at the operating point.



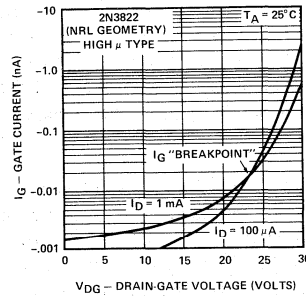
\bar{e}_N Changes vs I_D Variations
Figure 5

The optimum (lowest) \bar{i}_N in depletion-mode junction FETs should occur at $V_{GS} = 0$ ($I_D = I_{DSS}$). In practice, very little change will be seen in \bar{i}_N when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate \bar{i}_N characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

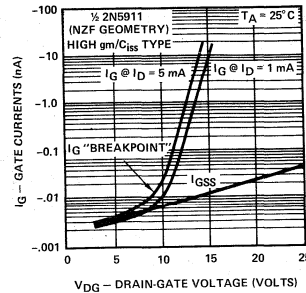


\bar{i}_N Characteristics as Function of Drain-Gate Voltage
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.⁽⁴⁾ Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at $V_{DG} = 10$ V, whereas high μ devices ($\mu = r_{ds} \cdot g_{fs}$) have much higher I_G breakpoints, typically $V_{DG} = 20 - 30$ V.



Gate Operating Current vs Drain-Gate Voltage
Figure 7

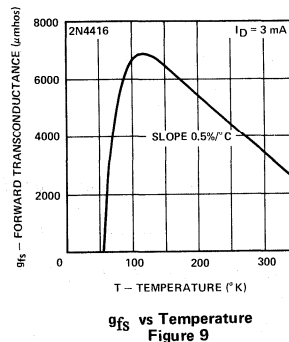


Gate Currents vs Drain-Gate Voltage
Figure 8

Characteristics of \bar{e}_N and \bar{i}_N at Low Temperature

Three equations presented earlier ((7), (16) and (17)) show that \bar{e}_N and \bar{i}_N are temperature dependent. \bar{e}_N and \bar{i}_N are proportional to \sqrt{T} , and both will be reduced if the temperature is lowered. In Equation (16), \bar{i}_N is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11°C. \bar{e}_N is also proportional to $\sqrt{R_N}$, where $R_N \approx 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, \bar{e}_N will also lower.

In Figure 9, g_{fs} has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in g_{fs} is clearly shown.



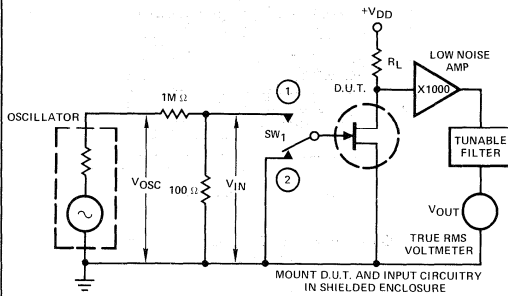
g_{fs} vs Temperature
Figure 9

In connection with the plot of \bar{e}_{fs} vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The \bar{e}_{fs} slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to I_{DZ} , the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.⁽⁵⁾ For best performance in this type of application, a high g_{fs}/C_{iss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

Test Measurements

By definition, \bar{e}_N and \bar{i}_N are referred to the input of the device under test. To measure \bar{e}_N , the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure \bar{e}_N
Figure 10

The following procedure should be used to make the \bar{e}_N test:

1. Set tunable filter to required f_{low} and f_{high} . Adjust oscillator to mean center frequency ($f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$).
2. Set V_{osc} to 100 mV with Switch 1 in position ①. Compute $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5} V = 10 \mu V$.
3. Measure V_{out1} . Compute overall gain as $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10 \mu V}$.
4. Set Switch 1 to position ② and measure V_{out2} . Compute V_{in2} , the equivalent short-circuit input noise voltage (\bar{e}_N), using A_v from Step 3. $V_{in2} = \frac{V_{out2}}{A_v} = \bar{e}_N$ in volts over bandwidth f_{low} to f_{high} .

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring \bar{e}_N and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure \bar{e}_N at certain frequencies over certain bandwidths in the $1/f^n$ region. The rms noise over a bandwidth from f_{low} to f_{high} , where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\bar{e}_N = [\bar{e}_N \text{ known}] \cdot \left[f_{\text{known}} \cdot \ln \left(\frac{f_{\text{high}}}{f_{\text{low}}} \right) \right]^{1/2n} \quad (18)$$

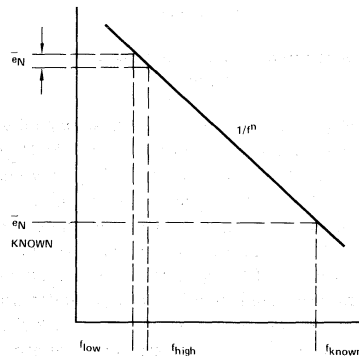
Figure 11 represents this equation graphically. For example, \bar{e}_N known = $70 \times 10^{-9} V/\sqrt{Hz}$ at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\bar{e}_N = \left[70 \times 10^{-9} \right] \cdot \left[10 \cdot \ln \left(\frac{5.5}{4.5} \right) \right]^{1/2} \text{ Volts} \quad (19)$$

or

$$\bar{e}_N = 99.16 \times 10^{-9} V/\sqrt{Hz} @ 4.975 \text{ Hz}, \quad (20)$$

4.975 Hz is the mean center frequency where $f_{\text{mean}} = (f_{\text{low}} \cdot f_{\text{high}})^{1/2}$.



Computing rms Noise Over a Bandwidth
Figure 11

\bar{i}_N measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, \bar{i}_N is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G . From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resultant gate current and the computed \bar{i}_N due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by(6)

$$\bar{e}_{ni}^2 = \bar{e}_T^2 + \bar{e}_N^2 + \bar{i}_N^2 \cdot R_G^2 \quad (21)$$

where \bar{e}_T^2 is the thermal noise of the generator resistance R_G and \bar{e}_{ni}^2 is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that \bar{i}_N^2 can be calculated if \bar{e}_N^2 , \bar{e}_T^2 and total noise \bar{e}_{ni}^2 are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of \bar{i}_N . However, when R_G is very large \bar{e}_T^2 is much greater than $\bar{i}_N^2 \cdot R_G^2$. For example, over a 1 Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\bar{e}_T^2 = 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = 1.63 \times 10^{-12} \text{ V}/\sqrt{\text{Hz}} \quad (22)$$

Anticipated \bar{i}_N is

$$\bar{i}_N \approx 10^{-15} \text{ Amperes}/\sqrt{\text{Hz}} \quad (23)$$

and

$$\bar{i}_N^2 = 10^{-30} \text{ Amperes}/\sqrt{\text{Hz}} \quad (24)$$

Thus

$$\bar{i}_N^2 \cdot R_G^2 = 10^{-30} \cdot 10^{16} = 10^{-14} \text{ V}/\sqrt{\text{Hz}} \quad (25)$$

Therefore, $\bar{i}_N^2 \cdot R_G^2$ is much less than \bar{e}_T^2 , which renders this method of finding \bar{i}_N impractical for most common MOS FETs or junction FETs.

An improved method of measuring \bar{i}_N is to substitute a low-loss mica capacitor for resistor R_G . The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\bar{e}_{ni}^2 = \bar{e}_N^2 + \bar{i}_N^2 \cdot X_C^2 \quad (26)$$

(where X_C = capacitive reactance)

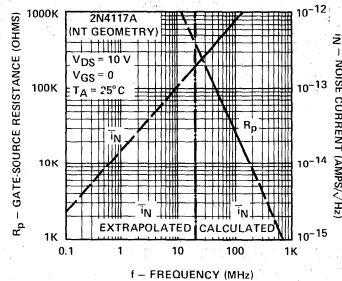
or

$$\bar{i}_N = \frac{(\bar{e}_{ni}^2 - \bar{e}_N^2)^{1/2}}{X_C} \quad (27)$$

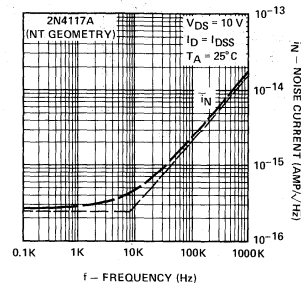
When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to \bar{i}_N^2 computed from measured gate current readings.

At frequencies above 100 Hz direct computation of \bar{i}_N via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating \bar{i}_N at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET.(7) When R_p is measured at various frequencies, the equivalent short-circuit input noise current (\bar{i}_N) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure R_p accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for \bar{i}_N computed via direct measurement of R_p for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz, \bar{i}_N must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) \bar{i}_N can be computed down to 2 MHz, and hence extrapolated \bar{i}_N between 100 Hz and 100 kHz is more accurate.

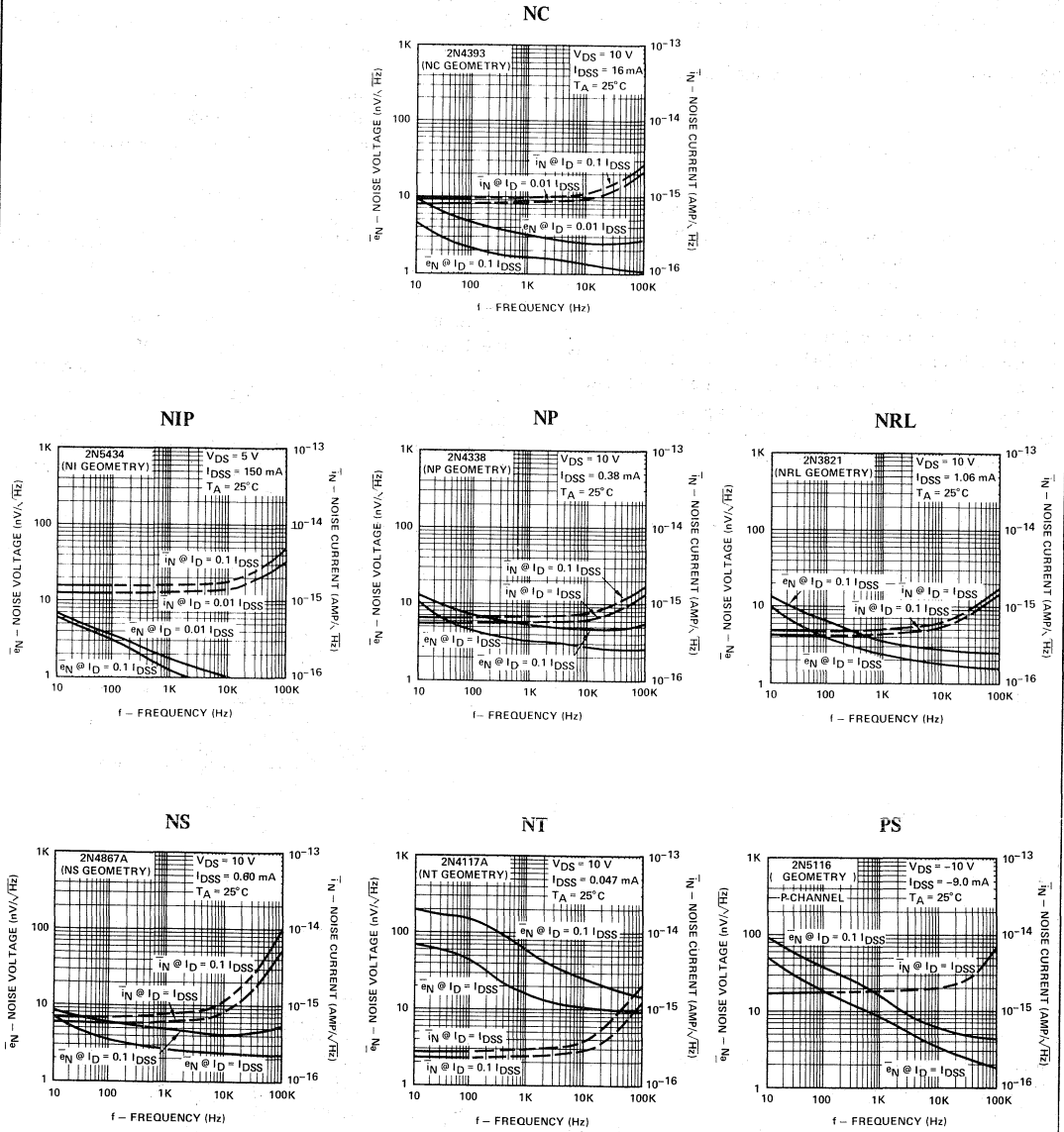


Low Frequency Limit for Calculated \bar{i}_N
Figure 12



Extrapolated \bar{i}_N vs Frequency
Figure 13

The following are representative \bar{e}_N , \bar{i}_N curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.



FET Noise Characteristics by Geometry
Figure 14

CONCLUSION

Contemporary junction FETs have noise voltages (\bar{e}_N) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current (\bar{i}_N) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high g_{fs} junction FETs can be realized.

The curves shown in Figure 14 are representative of \bar{e}_N and \bar{i}_N performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct \bar{e}_N measurements can readily be made. \bar{i}_N can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current (I_G). When I_G is

known, \bar{i}_N can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

REFERENCES

- (1) Nyquist, H., "Thermal Agitation of Electric Charge in Conductors," *Phys. Review* 32 (1928), p 110.
- (2) Van der Ziel, A., "Thermal Noise in Field-Effect Transistors," *Proceedings of the IRE*, Vol. 50, August 1962, pp 1808-1812.
- (3) Fitchen, F.C. and Motchenbacher, C.D., *LOW NOISE ELECTRONIC DESIGN*, 1st Edition, John Wiley & Sons, New York, 1973, pp 103-107.
- (4) MacDonald, Charles L., "Behavior of FET Gate Current," Siliconix incorporated Application Note, April, 1969.
- (5) Radeka, V., "Field-Effect Transistors in Charge-Sensitive Amplifiers," National Academy of Sciences, National Research Council Publication 1184.
- (6) Op. cit., *LOW NOISE ELECTRONIC DESIGN*, pp 30-31.
- (7) Op. cit., *LOW NOISE ELECTRONIC DESIGN*, pp 103-107.

APPLICATION NOTE

FETs for Video Amplifiers

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_g and the FET input impedance Z_{in} form a frequency sensitive attenuation network. The larger the R_g , the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
 C_{gs} and C_{gd} = bulk series gate capacitance
 G_{oss} = output conductance

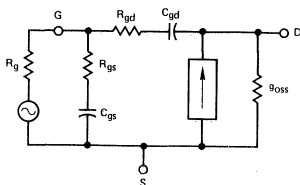


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

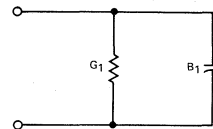


Figure 2

where

$$G_1 = \text{Re } |Y_{in}| = \frac{\omega^2 [T_1 C_1 (1 + \omega^2 T_2^2) + T_2 C_2 (1 + \omega^2 T_1^2)]}{1 - (\omega^2 T_1 T_2)^2 + \omega^2 (T_1^2 + T_2^2)} \quad (1)$$

and

$$B_1 = \text{Im } |Y_{in}| = \frac{\omega [C_1 (1 + \omega^2 T_2^2) + C_2 (1 + \omega^2 T_1^2)]}{1 - (\omega^2 T_1 T_2)^2 + \omega^2 (T_1^2 + T_2^2)} \quad (2)$$

where

$$T_1 = C_{gd} R_{gd} \\ T_2 = C_{gs} R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

In common-source circuits, $1/G_1$ will typically fall to $< 2K$ ohms at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

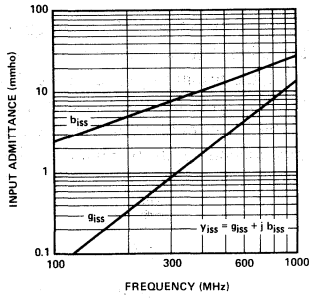
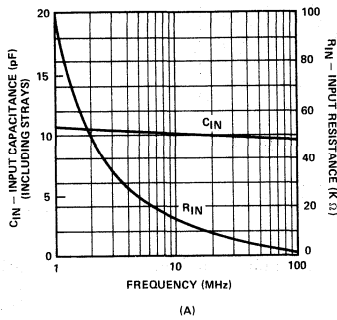
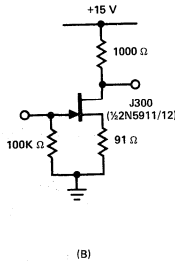


Figure 3



(A)

Figure 4



(B)

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of R_g on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

Circuits to Consider

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascade Amplifier
- FET and Bipolar Cascade

Common-Source Circuit¹

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560 \Omega \tag{4}$$

$$C_T = C_{gd} + C_D + C_S \tag{5}$$

$C_{gd} = 2.0$ pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7 \text{ pF} \tag{6}$$

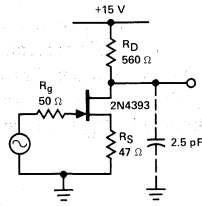


Figure 5

The 3-dB frequency ω_3 is given by:

$$\omega_3 = \frac{1}{C_T R_D} \tag{7}$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \tag{8}$$

$$\omega_3 = 255 \times 10^6 \tag{9}$$

$$f_3 = 39 \text{ MHz} \tag{10}$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \tag{11}$$

$$A_V = 4.9 \tag{12}$$

where

$$g_{fs} = 15 \text{ mmho when } I_D = 12 \text{ mA, the quiescent current} \tag{13}$$

$$R_D = 560 \Omega \tag{13}$$

$$R_S = 47 \Omega \tag{14}$$

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

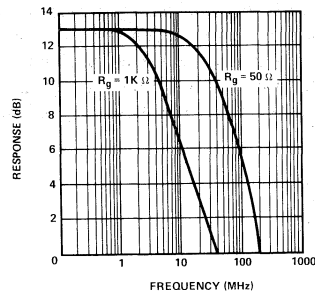


Figure 6

Effect of Increasing Generator Impedance

If the generator resistance R_g is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance ($R_g = 1K$ ohm) shunted by C_{in} (see Figure 7).

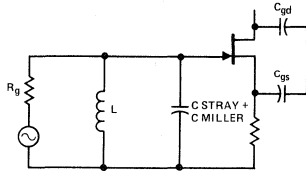


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S}\right) C_{gd} + \left(1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \quad (15)$$

$$C_{in} = 30 \text{ pF} \quad (16)$$

where

$$C_{gd} = 3.5 \text{ pF} \quad (17)$$

$$C_{gs} = 10 \text{ pF} \quad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_g} \quad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \quad (20)$$

$$f_3 = 5.3 \text{ MHz} \quad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_o = \frac{1}{2\pi\sqrt{LC_{in}}} \quad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \quad (23)$$

The response of an input signal of frequency f_o will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L, R_g and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

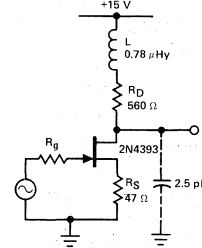


Figure 8

The required value of L is:

$$L = \frac{R_D^2 C}{2}, \text{ and for the circuit in Figure 8.} \quad (24)$$

$$= 0.78 \mu\text{H} \quad (25)$$

where

$$R_D = 560 \Omega \quad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM \text{ PROBE}} \quad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5 \text{ pF} \quad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 = 281 \text{ MHz} \quad (29)$$

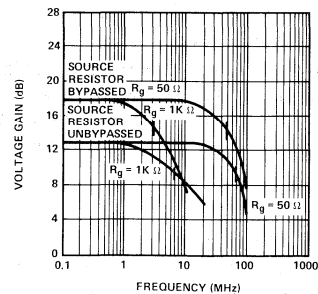


Figure 9

When R_S is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs} R_D \quad (30)$$

$$= 15 \times 10^{-3} \times 560 \quad (31)$$

$$= 8.4 \text{ (18.5 dB)} \quad (32)$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not and this effect is shown in Figure 9.

Source-Follower Circuit²

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high g_{fs} which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs} (1 - A_V)$ which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_O .

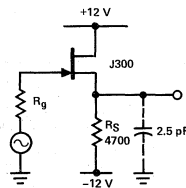


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs} R_S}{1 + g_{fs} R_S} \quad (33)$$

Thus A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or $\frac{1}{2}$ 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mmho and R_S 4700 ohms,

$$A_V = 0.96$$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_O = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200 \Omega \quad (34)$$

and in this circuit, R_O was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

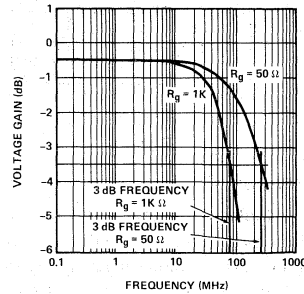


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers² mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V) C_{dg} \quad (35)$$

$$C_{in} = C_{iss} + C_{gd} \quad (36)$$

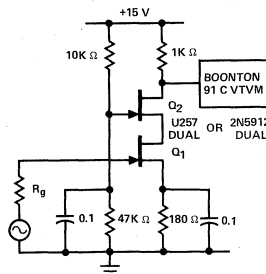


Figure 12

where A_V is the voltage gain from Q_1 gate to Q_1 drain which is essentially unity. C_{iss} for the U257 dual FET is 5 pF and C_{dg} is 1 pF, therefore

$$C_{in} = 5 + 1 = 6 \text{ pF, excluding strays of 4 pF}$$

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

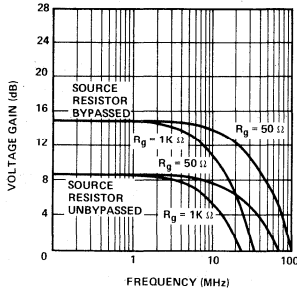


Figure 13

FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base.

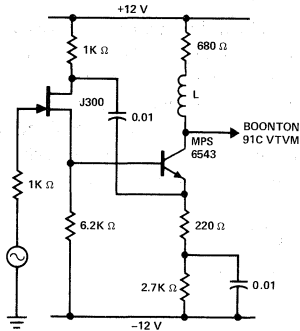


Figure 14

This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET, $v_g \cong v_s \cong v_d$ and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

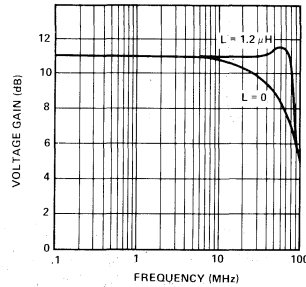


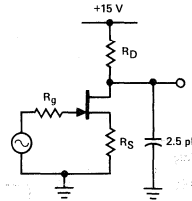
Figure 15

APPENDIX

Selection of Video Amplifier Designs with Performance Summary

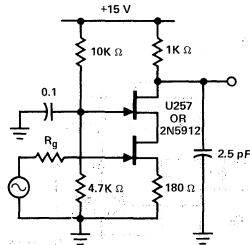
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



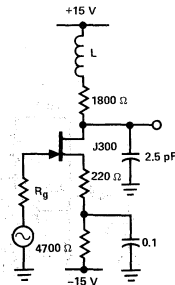
Device	R _g Ω	R _S Bypassed	R _S Ω	R _D Ω	Gain	dB	C _{in} pF	BW MHz	GBW MHz
2N4393	50		47	560	4.5	13.0	44	197	
	50	x	47	560	7.5	17.5	40	300	
	1K		47	560	4.5	13.0	5.0	22	
	1K	x	47	560	7.5	17.5	3.5	26	
J300	50		91	1K	3.8	11.6	11.0	27.5	103
	1/2	x	91	1K	6.3	16.0	14.5	30.0	189
2N5912	1K		91	1K	3.8	11.6	11.0	9.5	36
	1K	x	91	1K	6.3	16.0	6.5	41	
2N4416	50		120	1.5K	3.9	11.8	11.5	25	98
	50	x	120	1.5K	6.2	15.8	13	19	118
	1K		120	1.5K	3.9	11.8	11.5	8	31
	1K	x	120	1.5K	6.2	15.8	13	7	44

Cascode



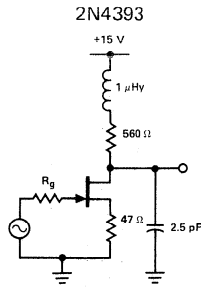
R _g Ω	R _S Bypassed	Gain	dB	C _{in} pF	BW MHz	GBW MHz
50		2.7	8.5	9	27	73
50	x	5.6	15	11.5	27	151
1K		2.7	8.5	9	9.5	73
1K	x	5.6	15	11.5	9.0	51

Common-Source Circuit

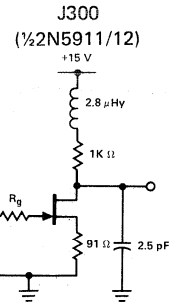


R _g Ω	L μH	Gain	dB	C _{in} pF	BW MHz	GBW MHz
50	0	3.5	11	2	20	70
1K	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1K	15	3.5	11	2	17	60

Shunt-Peaked Common-Source Stage

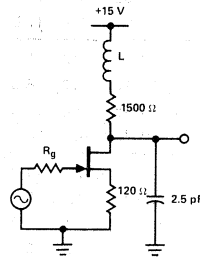


R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		4.2	12.5	66	277
50	x	7.5	17.5	54	405
1K		4.2	12.5	6.0	25
1K	x	7.5	17.5	3.5	26



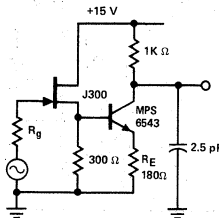
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		3.9	11.8	67	262
50	x	6.3	16.0	67	421

2N4416

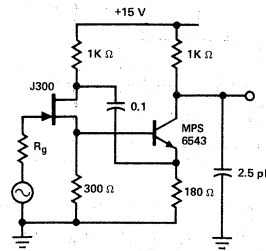


R_g Ω	L μ H	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50	4		3.9	11.8	45	175
50	4	x	6.2	15.8	40	248
50	5	x	6.2	15.8	45	279

Common-Drain Common-Emitter Stage

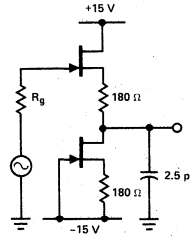
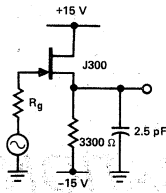


R_g Ω	R_E Bypassed (0.1 μ F)	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		3	9.5	2.0	39	117
50	x	25	28	2.0	21	525
1K		3	9.5	2.0	13	39
1K	x	25	28	2.0	11	275



R_g Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	5.6	15	1.0	32	179
1K	5.6	15	1.0	15	84

Source-Follower Circuit



R _g Ω	Gain	C _{in} Stray pF	C _{in} Total pF	R _o Ω	BW MHz	GBW MHz
50	0.92	2.2	2.7	165	350	326
1K	0.92	2.2	2.7	165	55	50

Note. R_o = output resistance of the source follower.

Dual FET	R _g Ω	Offset (Max) (Input to Output) mV	Gain	BW MHz	GBW MHz
U257	50	100	0.98	70	69
2N5912	1K	100	0.98	15	14.7
U232	50	10	0.98	85	83
	1K	10	0.98	13	12.7

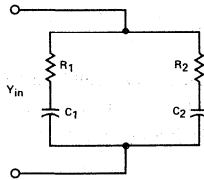
Derivation of Input Admittance Terms

where

$$R_1 = R_{gs} \quad C_1 = C_{gs} \quad (1)$$

$$R_2 = R_{gd} \quad C_2 = C_{gd} \quad (2)$$

$$s = j\omega$$



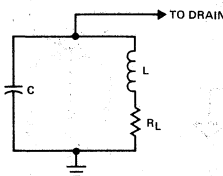
$$Y_{in} = \frac{sC_1}{R_1 C_1 s + 1} + \frac{sC_2}{R_2 C_2 s + 1} \quad (3)$$

$$= \frac{-\omega^2 C_1 C_2 (R_1 + R_2) + s(C_1 + C_2)}{(1 - \omega^2 R_1 R_2 C_1 C_2) + s(C_1 R_1 + C_2 R_2)} \quad (4)$$

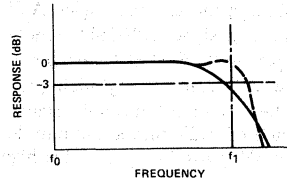
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L^2 + \omega^2 L^2}{(1 - \omega^2 LC)^2 + \omega^2 C^2 R_L^2} \right]^{1/2} \quad (5)$$



The response below shows the "normal" 3-dB frequency without peaking - f₁. It is now required to raise the response at f₁ by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f₁ must equal the impedance seen by the drain at f_o. Also at f₁, X_C = R_L. Substituting for X_C in Equation 5:



$$R_L^2 = \frac{R_L^2 + \omega^2 L^2}{\left(1 - \frac{\omega L}{R_L}\right)^2 + 1} \quad (6)$$

$$R_L^2 - 2\omega L R_L + \omega^2 L^2 + R_L^2 = R_L^2 + \omega^2 L^2 \quad (7)$$

$$R_L^2 = 2\omega L R_L \quad (8)$$

$$R_L = 2\omega L \quad (9)$$

$$L = \frac{R_L}{4\pi f_1} \quad (10)$$

and

$$f_1 = \frac{1}{2\pi R_L C}, \therefore L = \frac{R_L^2 C}{2} \quad (11)$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascode Circuits Reduce Feedback Capacitance," August 1970.



APPLICATION NOTE

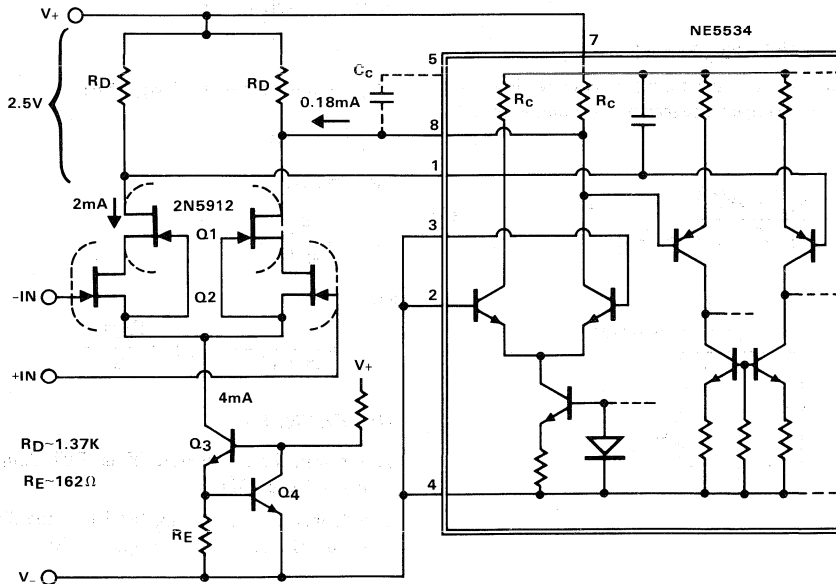
Composite Op Amp for High Performance

For op amp applications requiring the best possible performance, consider a composite op amp that takes advantage of differing process technologies. A JFET dual can be combined with a Signetics NE5534 bipolar op amp for outstanding performance. Input bias current can be reduced, yet slew rate can be very high ($20V/\mu\text{sec}$ to $40V/\mu\text{sec}$) and the circuit is unity-gain stable. Output swing is a minimum of $\pm 12V$ into a 600 ohm load when operating from $\pm 15V$ power supplies. This high output

capability combined with a JFET input stage makes this an excellent amplifier for high-speed integrators, SAMPLE/HOLD circuits, peak detectors, and log amplifiers.

The input portion of the circuit is shown in Figure 1. The NPN input stage of the NE5534 IC op amp is biased into cut-off by connecting both inverting and non-inverting inputs to the negative rail. A JFET preamplifier input stage

High Performance Op Amp Using The Siliconix 2N5912



is then connected into the PNP second stage of the NE5534 and the currents that formerly flowed through the NE5534 NPN input pair are now diverted into the JFET input pair. Drain resistors R_D effectively parallel the collector resistors R_C from within the IC op amps and the JFET drain currents will then be the sum of the currents through R_D and R_C . The voltage across the parallel combination of R_D and R_C is nominally 2.5V due to the internal biasing of the NE5534. Going directly into the second stage of the IC op amp rather than into the NE5534 NPN input stage has two distinct advantages:

1. Frequency response is better in that the phase shift of the bipolar input stage is avoided. A high-current JFET input stage, such as the 2N5912 when operated in the 1mA to 8mA drain current range, has excellent frequency response in comparison to an NPN stage operating in the 150 μ A to 200 μ A range.
2. The operating level at the JFET drains is only 2.5V below the positive supply rail, therefore the common-mode input range for the JFET input stage can be relatively high. The combination of low input bias current with high frequency response is useful for SAMPLE/HOLD circuits, high-speed integrators, photo-multiplier tube amplifiers, and high-speed data conversion circuits.

Although more expensive than a single monolithic op amp, the combination of a JFET preamp with a bipolar IC second stage can provide substantially better performance than any monolithic alternatives.

A Siliconix 2N5912 JFET dual was chosen for the input stage in this example because of its high operating current range, high gain, and excellent frequency response. The saturation drain current I_{DSS} has a specified range of 7mA to 40mA, but is typically 10mA to 24mA. Gate source cutoff voltage $V_{GS(off)}$ is in the range of -1V to -5V with a typical value of approximately -2V to -4V. The 2N5912 characterization curves indicate that any drain current from 1mA to 8mA will provide good performance, and 2mA was chosen for this application.

The current diverted from the bipolar input stage to the JFET input stage is nominally 180 μ A on each side; therefore a drain current on each side of 1.82mA is needed from the drain resistors R_D to make up a total drain current of 2.0mA. The drain resistor R_D therefore needs to be approximately 2.5V/1.82mA, or 1370 ohms on each side.

Gain of the JFET input stage can now be calculated. From the 2N5912 characterization curves, forward transconductance g_{fs} will be in the range of 2.6mmhos to 5mmhos for units having I_{DSS} of 10mA to 24mA and when operated at a drain current of 2mA. The differential gain can be approximated by the product $g_{fs} R_D$. Using a center value of 4.3mmhos and 1230 ohms, (R_D and R_C in parallel), then the gain will be approximately 6.5, or 16dB. Total

amplifier gain was found to closely approximate the gain curve for a 5534 being operated alone.

The cascode configuration using two input pairs as shown has several advantages. Most importantly, the input gate current is dramatically reduced due to the lower drain-to-gate voltage on the input pair. In the cascode configuration, the gate-to-source voltage on the upper pair will be the drain-to-source voltage of the input pair even with the common-mode input variations. All of the common-mode swing is taken up by variations in V_{DS} of the upper pair. Gate leakage of the input pair is primarily dependent on drain-to-gate voltage V_{DG} , which will be a constant $-2V_{GS}$ in this cascode configuration. Drain-to-gate voltage on the input pair will be low, typically in the 3V to 6V range, which is well below the "IG breakpoint". From the characterization curves on the 2N5912, gate current leakage will be under 2pA for drain-to-gate voltages under 6V. The cascode configuration is very effective in reducing input bias current for JFET input stages. Another advantage of the cascode configuration is a reduction of input capacitance. The input pair drains are "bootstrapped" to the common source point and both must follow the gate voltage. The effective capacitance from gate-to-drain and from gate-to-source is reduced. In addition, output conductance is reduced by the cascode configuration which also helps CMR. Adding the second JFET pair significantly improves both input bias current and common-mode rejection without degrading other parameters.

The constant current source consisting of Q3 and Q4 primarily improves common-mode rejection and rejection of power supply variation. It also establishes the nominal operating voltage at the input (pins 1 and 8) of the 5534 op amp. The current will be a constant V_{BE}/R_E independent of fluctuations in power supply voltage or input voltage level. This current source has very high impedance, therefore common-mode inputs are heavily attenuated.

Common-mode-rejection-ratio (CMRR) is very high due to the use of a constant current source, but can be further improved by matching of drain resistance. The parallel combination of R_D and R_C is the effective drain resistance for this design. The transconductance ratio between the two sides of the input pair also directly affects CMRR. The drain resistors should be well-matched to minimize the CMRR adjustment range since it also affects offset and drift.

Each 1% mismatch in drain resistance will cause approximately 11 μ V/ $^{\circ}$ C of input offset voltage drift. CMRR can be readily trimmed to over 100dB. CMRR vs. frequency is excellent due to the use of the 2N5912, a wide-bandwidth FET, in a cascode configuration.

A high performance op amp should also have good output characteristics, low noise, and high slew rate. The NE5534 op amp is rated for \pm 14V minimum output swing into a 600 ohm load when operating from \pm 15V power supplies. Output resistance is typically 0.3 ohms. The Siliconix

2N5912 characterization curves show a typical equivalent input noise voltage of only $10\text{nV}/\sqrt{\text{Hz}}$ at 10Hz. There is also a component of noise from the second stage, but its effect is divided by the input stage gain and its contribution is small. Input current noise of this composite op amp is very low due to the typical operating level of 1pA input bias current. For slew rate, this circuit is capable of $50\text{V}/\mu\text{sec}$ when going negative. Positive slew rate is $50\text{V}/\mu\text{sec}$ without use of a compensation capacitor, but drops to $25\text{V}/\mu\text{sec}$ with a 20pF compensation capacitor. Compensation capacitance will generally be needed only when driving capacitive loads. Even the lower value of slew rate,

$25\text{V}/\mu\text{sec}$, corresponds to a full-power ($\pm 10\text{V}$) frequency of 400KHz.

While the vast majority of op amp applications can be satisfied through use of conventional IC op amps, there are applications in high-performance instrumentation systems that require superior performance. This composite op amp, which makes use of precision dual JFET input pairs and a high performance IC op amp, provides a unique combination of low input bias current, high CMR, low noise, excellent frequency response, and high output swing.

APPLICATION NOTE

FETs in Balanced Mixers

Ed Oxner

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

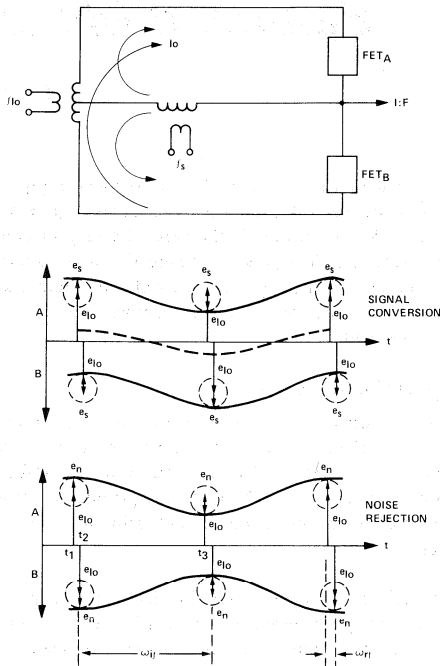
DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors

Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{if}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{10}); and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2 , the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving

ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° ($\omega_{if}t$) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.⁽¹⁾

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2 , the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{10} . The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

- (1) Intermodulation and Cross-Modulation
- (2) Conversion Gain
- (3) Noise Figure
- (4) Selecting the Proper FET
- (5) Local Oscillator Injection
- (6) Designing the Input Transformer
- (7) Designing the IF Network

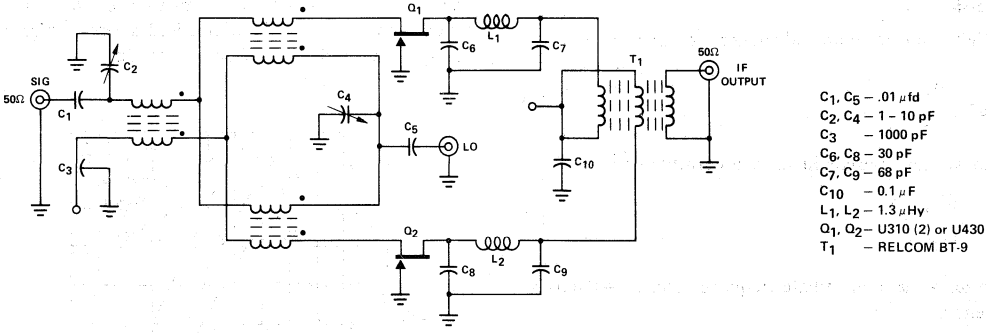
Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.⁽²⁾

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c , is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs} , of the FET when used as an amplifier.



Prototype Active Balanced Mixer
Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_v , as:

$$A_v = g_c R_L \quad (1)$$

where g_c is the conversion transconductance and R_L is the FET drain load.

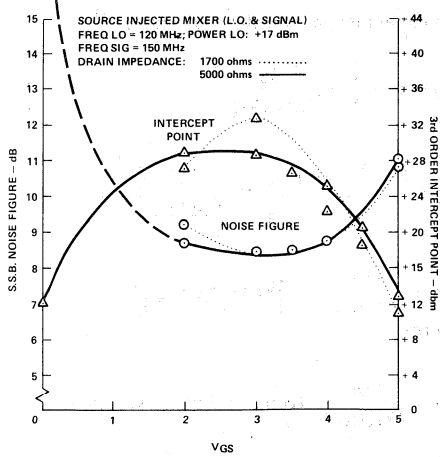
An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion – particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called “varactor effect.”

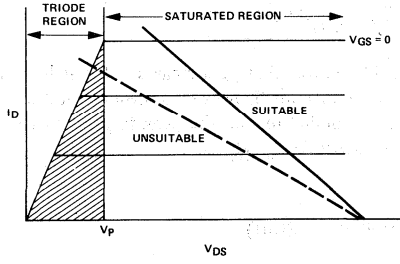
The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.⁽³⁾ A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated (“triode”) region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the “varactor effect” is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance, C_{rss} , and give rise to harmonics.⁽⁴⁾ A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain

load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics
Figure 3



Plotting Drain Load Lines
Figure 4

Conversion Gain

In a FET, forward transconductance is defined as⁽⁵⁾

$$g_{fs} = \frac{dI_D}{dV_{gs}} \quad (2)$$

and conversion transconductance is defined as⁽⁶⁾

$$g_c = \frac{dI_D(\omega_i)}{dV_{gs}(\omega_r)} \quad (3)$$

where ω_i = the intermediate frequency and ω_r = the signal frequency.

The effects of time-varying local oscillator voltage, V_2 , and the much smaller signal voltage, V_1 , must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \quad (4)$$

For square law operation⁽⁷⁾

$$V_2 + V_{GS} \leq V_{GS(off)} \quad (5)$$

Drain current is approximately defined by⁽⁸⁾

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2 \quad (6)$$

or⁽⁹⁾

$$I_D \approx \frac{g_{fso}}{2} \frac{V_{GS(off)}}{2} \left[1 - \frac{v_{gs}}{V_{GS(off)}} \right]^2 \quad (7)$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \left[V_{GS(off)} - v_{gs} \right]^2 \quad (8)$$

then⁽¹⁰⁾

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \quad (\text{complex Taylor expansion}) \quad (9)$$

which can be reduced to

$$I_D(IF) \approx \frac{g_{fso}}{2V_{GS(off)}} V_1 V_2 \cos(\omega_1 - \omega_2)t \quad (10)$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}} |V_2| \quad (11)$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

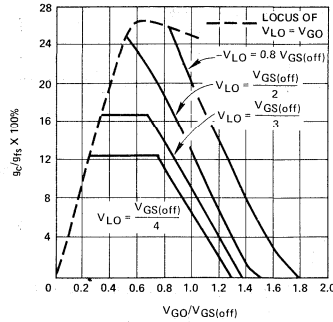
Thus

$$2 V_2 \text{ peak} \leq V_{GS(off)} \quad (12)$$

or

$$V_2 \text{ peak} \leq \frac{V_{GS(off)}}{2} \quad (13)$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.



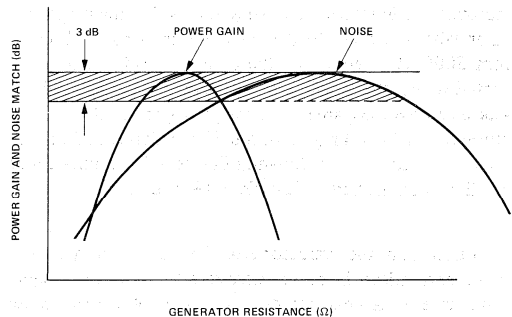
Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$
 (from "FET RF Mixer Design Technique", S.P. Kwok,
 WESCON Convention Record (1970) 8/1, p.2.)

Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g .⁽¹¹⁾ A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs} , which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching

Figure 6

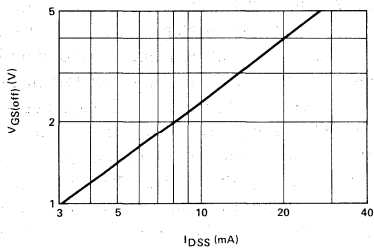
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c , which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS} , and the gate cutoff voltage, $V_{GS(off)}$:

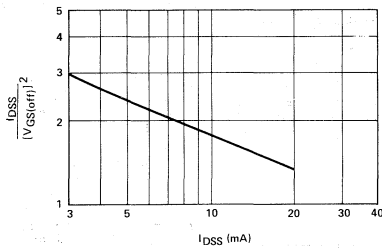
$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2} |V_2| \quad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \quad (15)$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c .



a.



b.

Relationship of I_{DSS} and $V_{GS(off)}$

Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS} , for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μ mhos max at $V_{DS} = 10$ V, $I_D = 10$ mA, and $f = 1$ kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach — the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember,

however, that conversion transconductance, g_c , can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

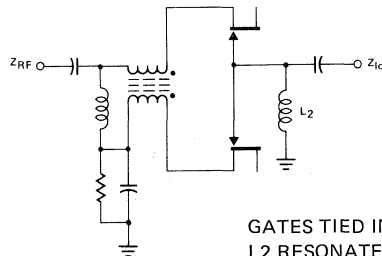
*Similar devices are also available in plastic packages:

- U310 (J310)
- 2N4416 (2N5486, J304-18)

Local Oscillator Injection

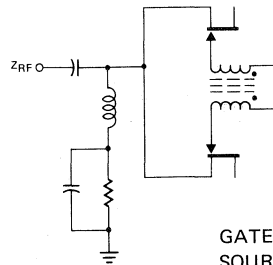
Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing. Two circuits to obtain direct gate coupling are suggested in Figure 8.



**GATES TIED IN PARALLEL
L2 RESONATES WITH C_g**

a.



**GATES DRIVEN PUSH-PULL
SOURCES TIED TOGETHER**

b.

Alternate Forms of L.O. Injection

Figure 8

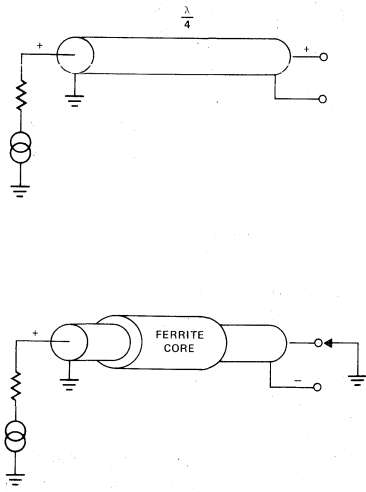
The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

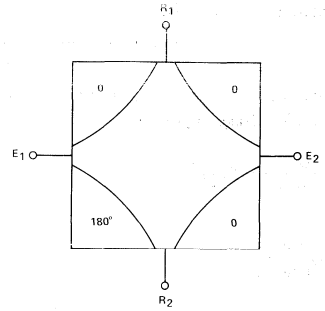
Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

- (1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B
- (2) Offer a match between either input to a symmetrical balanced load
- (3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)
- (4) Maintain a differential phase of 180° across the symmetrical balanced loads
- (5) Introduce the least possible amount of loss



Hybrid Input Coupling Transformer

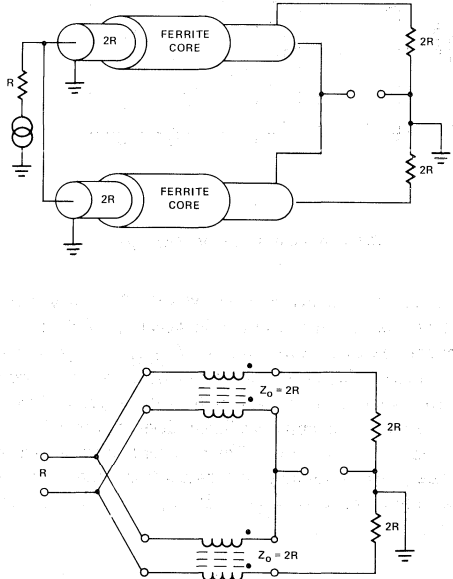
Figure 10



4-Port Hybrid with Phase and Isolation

Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.⁽¹²⁾ The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.⁽¹³⁾



Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.⁽¹⁴⁾ The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{\text{upper}}} \quad (\text{inches}) \quad (16)$$

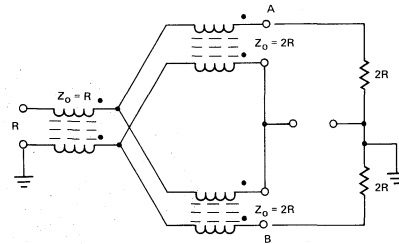
$$\text{min length} = \frac{20 R_L}{(1 + \mu/\mu_0) f_{\text{lower}}} \quad (\text{inches}) \quad (17)$$

where R_L = the load impedance, μ/μ_0 = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

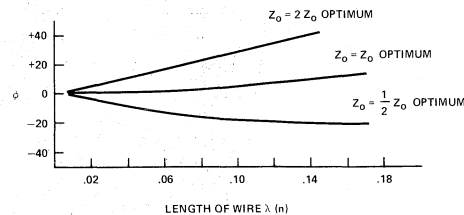
Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q .

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.⁽¹⁵⁾ A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line conductors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_0 , is to be preferred over a higher Z_0 . Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide $Z_0 = 100$ ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4 , Figure 2).⁽¹⁶⁾ A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ± 2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) — but phase track beyond 250 MHz *may* show too much deterioration.



a.



b.

Toroid Coil Winding Data

Figure 11

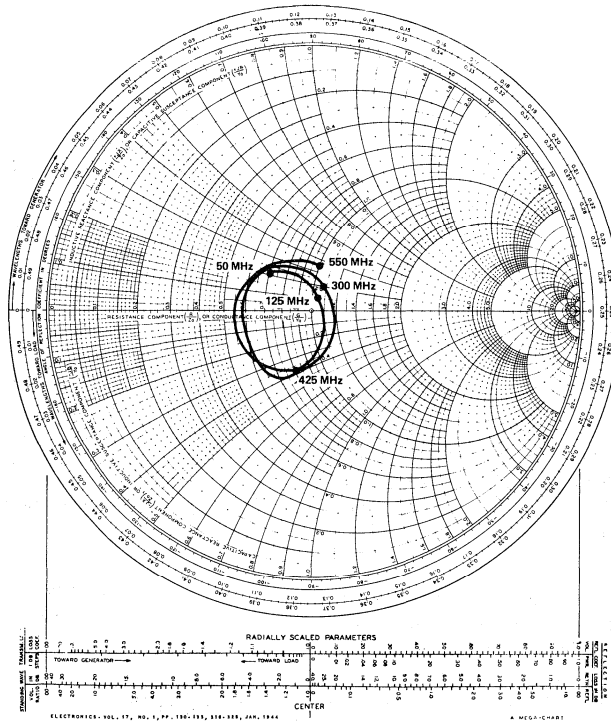
Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.⁽¹⁷⁾ This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_0 .^(18, 19) This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω — 200Ω Balun
Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.⁽²⁰⁾ If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2 V_{GS(off)}}{i_d} \quad (18)$$

where

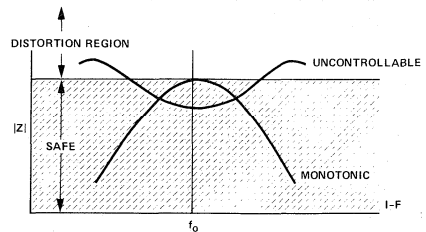
$$i_d = I_{DSS} \left[1 - \frac{v_{gs}}{V_{GS(off)}} \right]^2 \quad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \quad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function
Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.⁽²¹⁾ With two signals 300 kHz apart, the balanced mixer suppressed third-order products -89 dB with both signals at -10 dBm, representing an intercept point of +32 dBm.

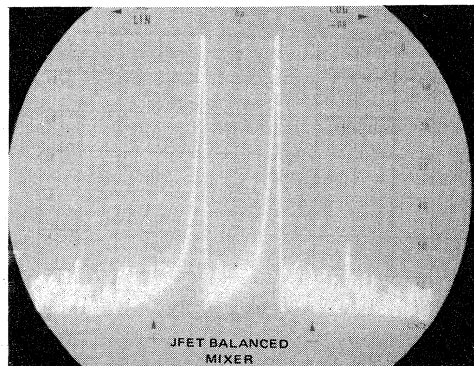
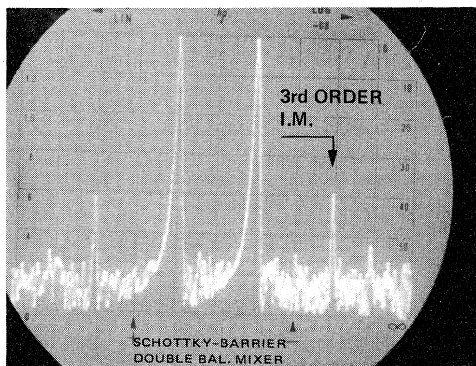
Table IV
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	-6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

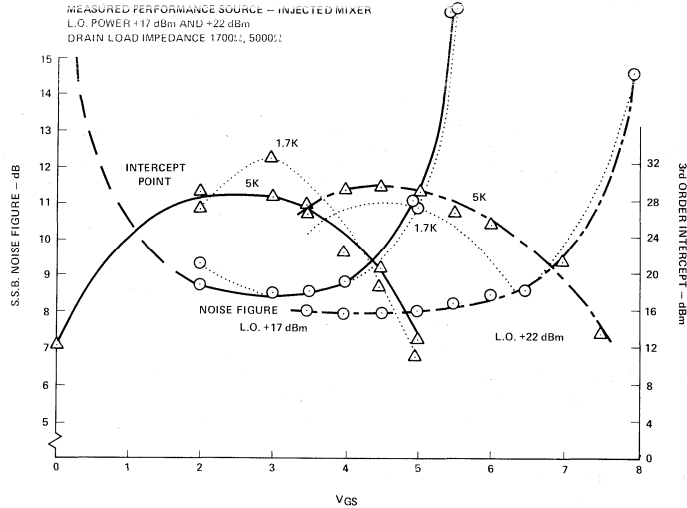
†Estimated *Conservative minimum

Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products
Figure 14



Noise Figure and Intercept Point Performance

Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

REFERENCES

- (1) Pound, R.V., MICROWAVE MIXERS, MIT Rad. Lab. Series, Vol. 16, Figure 6.14, p. 274 (1948).
- (2) "High-Frequency JFET Characterization and Applications," J.B. Compton, DESIGN ELECTRONICS, March, 1970.
- (3) "The Solid State Receiver," W. Sabin, QST, July 1970, pp. 35-43.
- (4) Penfield, P., and Rafuse, R., VARACTOR APPLICATIONS, MIT Press, Cambridge, Mass., (1962), pp. 73ff.
- (5) "Non-Linear Distortion and Mixing Processes in FETS," J.S. Vogel, Proc. of IEEE, Vol. 55, No. 12 1967, pp. 2109-2116.
- (6) "UHF FET Mixer of High Dynamic Range," ECOM-0503-P005-G821 (1969). (Available from U.S. Army)
- (7) Op. cit., ECOM-0503-P005-G821.
- (8) J. Watson, INTRODUCTION TO FIELD-EFFECT TRANSISTORS, Siliconix, Inc., Santa Clara, Ca., 95054 (1970). p. 18.
- (9) Op. cit., ECOM-0503-P005-G821.
- (10) Op. cit., "Non-Linear Distortion and Mixing Processes in FETS," p. 2112.
- (11) Op. cit., "High-Frequency JFET Characterization."
- (12) O. Pitzalis and T. Couse, "Broadband Transformer Design for RF Transistor Power Amplifiers," ECOM-2989, July 1968. Also in Proc. Electronic Component Conference (1968).
- (13) "Some Broadband Transformers," C.L. Ruthroff, Proc. IRE, Vol. 47, Aug. 1969, pp. 1337-1342 (Figure 7(b)).
- (14) Op. cit., ECOM-2989, July 1968.
- (15) Op. cit., ECOM 2989, p. 6.
- (16) Op. cit., ECOM 2989, p. 7.
- (17) ARRL HANDBOOK, American Radio Relay League, Newington, Conn. (1970) p. 49.
- (18) "Reactive Loads - The Big Mixer Menace," P. Will, MICROWAVES, April 1971, pp. 38-42.
- (19) Op. cit., "The Solid State Receiver."
- (20) "Distortion in FET Amplifiers," J. Sherwin, ELECTRONICS, Dec. 12, 1966.
- (21) "Don't Guess The Spurious Level," F.C. McVay, ELECTRONIC DESIGN, Feb. 1, 1967, pp. 70-73.

APPLICATION NOTE

FETs As Voltage-Controlled Resistors

INTRODUCTION

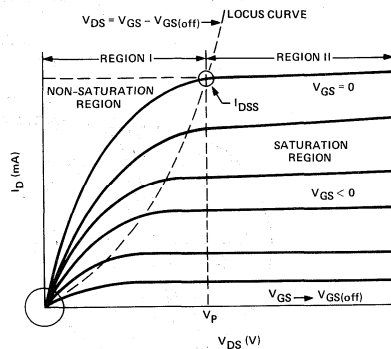
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS} , and the net drain-source voltage, V_{DS} .

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.⁽¹⁾ Maximum drain-source current, I_{DSS} , and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.⁽²⁾ The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

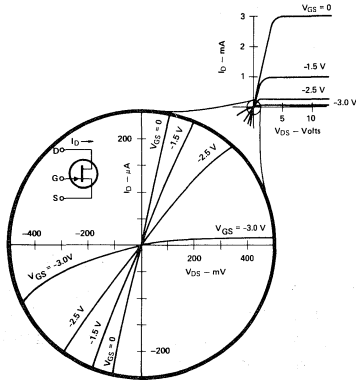


Typical N-Channel JFET Operating Characteristics
Figure 1

Resistance Properties of FETs

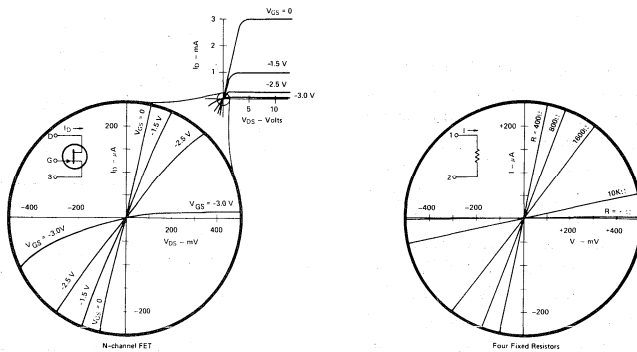
The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{DS} , is essentially the same as that of d.c. resistance, r_{DS} , and is a function of V_{GS} .⁽³⁾

Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D / \Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS} , usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS} . Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



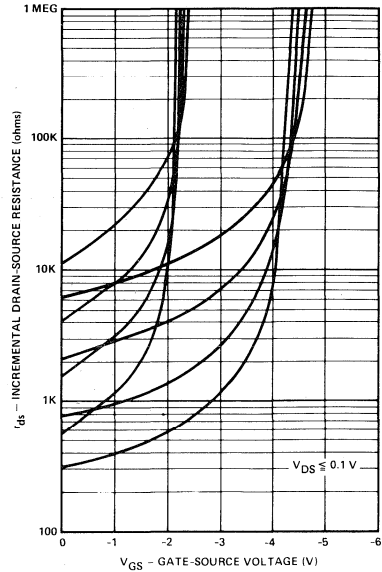
N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

Figure 3 extends the r_{DS} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.



Comparison of FET and Resistor Characteristics
Figure 3

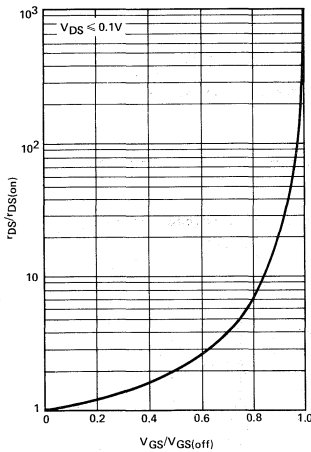
Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.⁽⁴⁾ The graphs are useful in estimating r_{DS} values at any given value of V_{GS} . All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefore desirable to convert Figure 4 to a normalized plot. This



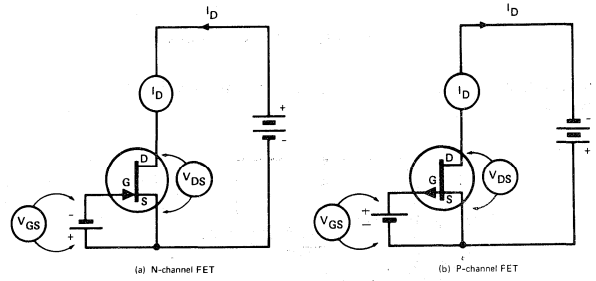
Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

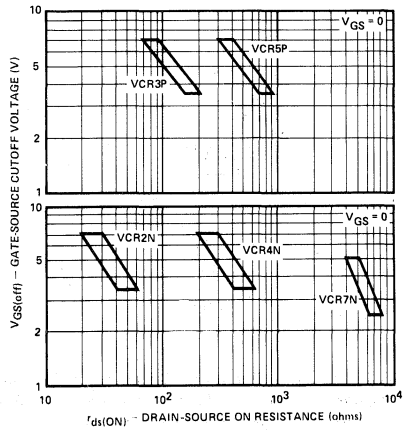
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



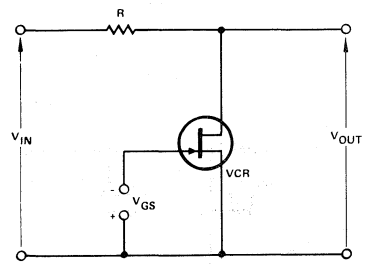
Normalized r_{ds} Data
Figure 5



Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.⁽⁵⁾

The output voltage is

$$V_{OUT} = \frac{V_{in} r_{DS}}{R + r_{DS}} \tag{1}$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which V_{OUT} can assume is

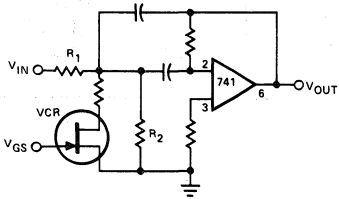
$$V_{OUT(min)} = \frac{V_{in} r_{DS(on)}}{R + r_{DS(on)}} \tag{2}$$

The highest value is

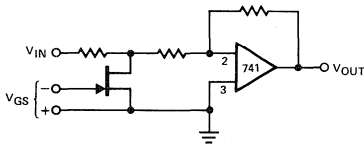
$$V_{OUT(max)} = v_{in} \quad (3)$$

since r_{DS} can be extremely large.

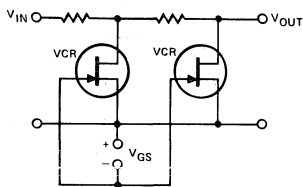
A number of other FET VCR applications are shown in Figures 9-16.



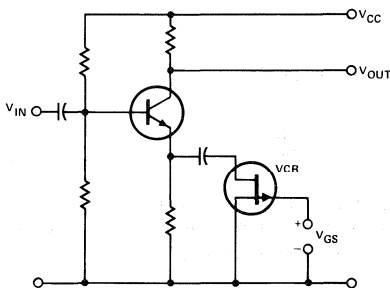
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2 . Upper Frequency is Controlled by R_1
Figure 9



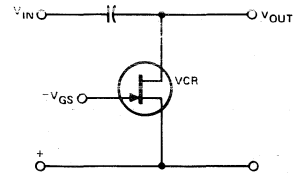
Electronic Gain Control
Figure 10



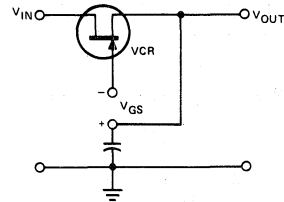
Cascaded VCR Attenuator
Figure 11



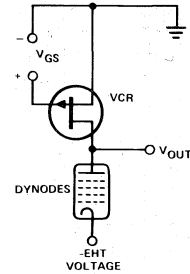
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



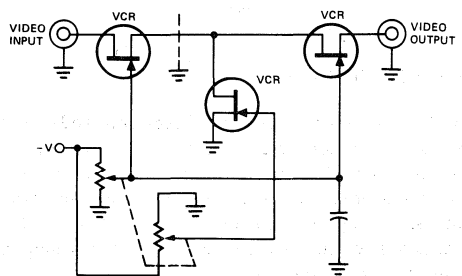
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



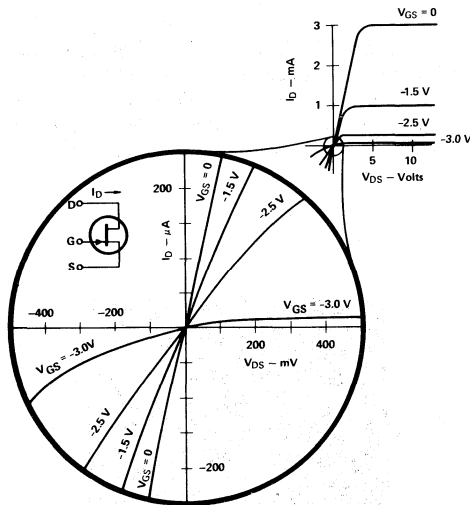
P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually $< 1 \mu A$) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS} , and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 17A

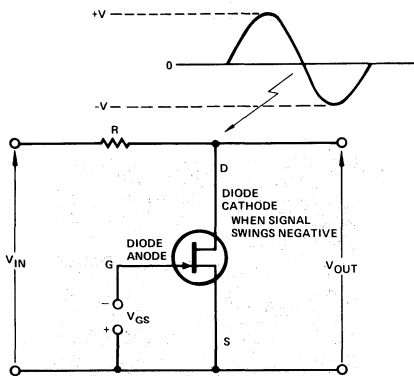


Figure 17B

in the third quadrant, rising negatively with an increasingly negative V_{DS} . This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

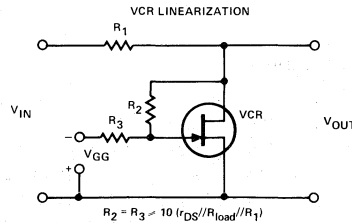


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10 [R_1 \parallel r_{DS}(\text{max}) \parallel R_L] \quad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)} \parallel R_L$ to $[(r_{DS(on)} \parallel R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \frac{r_{DS(on)} \parallel R_L}{(r_{DS(on)} \parallel R_L) + R_1} \quad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG} , be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

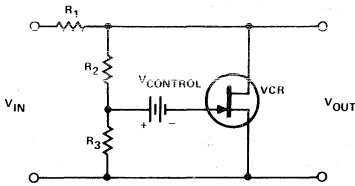


Figure 19

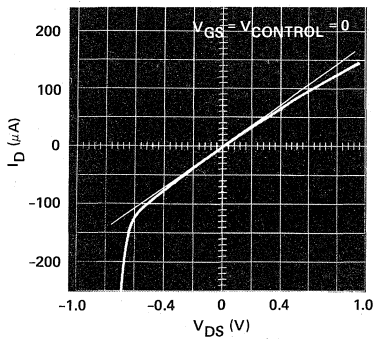
Experimental Results

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the $V_{GS} = 0$ V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

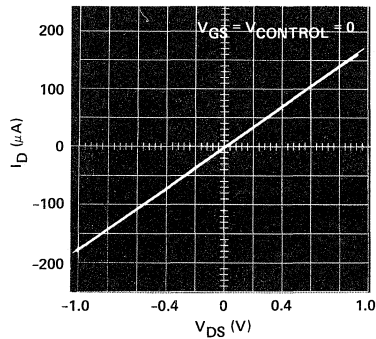
The forward-biased gate-drain PN junction may be seen at approximately -0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

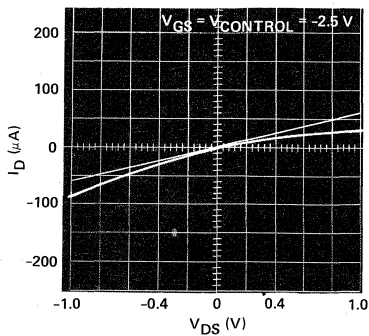
In Figures 22 and 23, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS} . No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



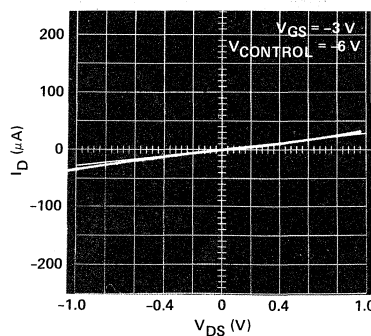
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21

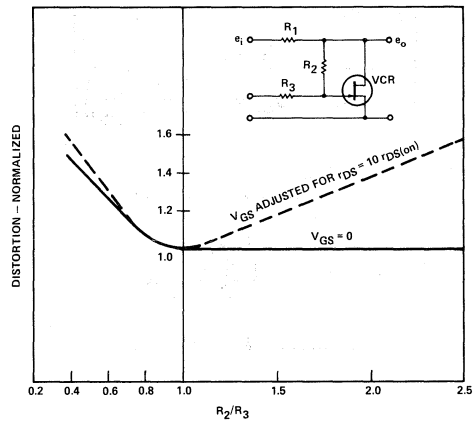


VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23

Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs R_2/R_3 , in both quadrants.



Distortion vs R_2/R_3
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. r_{DS} will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

Temperature (°C)	Without Feedback		With Feedback	
	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10 r_{DS(on)}$	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10 r_{DS(on)}$
+125	>13%	>6%	<0.5%	<0.5%
+ 25	>10%	>5%	<0.5%	<0.5%
- 55	3.9%	3.2%	<0.5%	<0.5%

SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

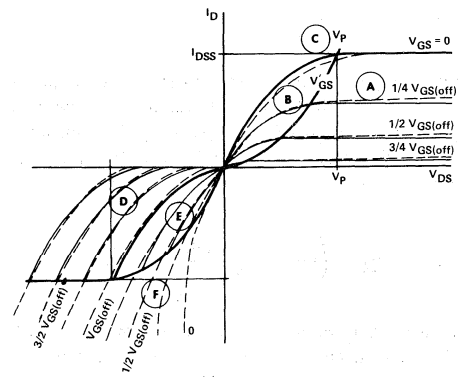
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired r_{DS} value) if large signal levels are to be encountered.

APPENDIX A — From proceedings of the IEEE, October, 1968, pp. 1718-1719.

Abstract — An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.^(6,7) The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) I_D is independent of V_{DS} .⁽⁸⁾

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \tag{1}$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, -) will be valid for N-Channel FETs.) The characteristics can be

approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS} \left[\left(1 - \frac{V_{GS}}{V_P} \right)^2 - \left(1 - \frac{V_{GS} - V_{DS}}{V_P} \right)^2 \right] \quad (2)$$

$$= \frac{2I_{DSS}}{(V_P)^2} V_{DS} \left(V_{GS} - V_P - \frac{V_{DS}}{2} \right)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction (V_{GS} , V_{GD}) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If V_{GD} were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V_P^2} V_{DS} \left(V_{GD} - V_P + \frac{V_{DS}}{2} \right) \quad (3)$$

Since the controlling voltage for both regions (B and E) is V_{GS} ,

$$V_{GD} = V_{GS} - V_{DS} \quad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS} \left(1 - \frac{V_{GS} - V_{DS}}{V_P} \right)^2 \quad (5)$$

The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

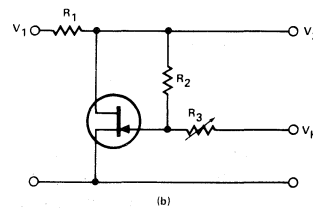
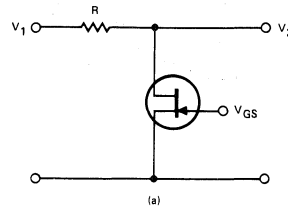
$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P} \right)$$

$$-\frac{I_{DSS}}{(V_P)^2} V_{DS} = g_{DS} + \frac{g_{DSS} V_{DS}}{2V_P} \quad (6)$$

where g_{DS} is the differential conductance at the origin; when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1 + Rg_{DS}} \quad (7)$$

$$= \left[1 + Rg_{DS} + \frac{Rg_{DSS} V_1}{2V_P \left(1 + Rg_{DS} + \frac{2Rg_{DSS} V_1}{2V_P (1 + Rg_{DS})} \right)} \right]^{-1}$$



(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1 Rg_{DSS}}{2V_P [1 + Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

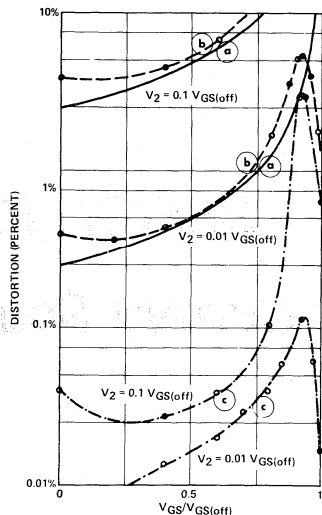
$$V_2 = \frac{V_1}{1 + g_{DS}R} \left(1 - \frac{Rg_{DS} V_1}{2V_P [1 + Rg_{DS}]^2} + \dots \right) \quad (8)$$

Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1 Rg_{DSS}}{4|V_P| [1 + Rg_{DS}]^2} \quad (9)$$

If V_2 is held constant,

$$d = \frac{V_2 Rg_{DS}}{4|V_P| [1 + Rg_{DS}]} \approx \frac{V_2}{4|V_P - V_{GS}|} \quad (10)$$



Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b) Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If V_{GS} approaches V_P , the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of V_{GS} :

$$V_{2max} = 4d_{max} |V_P - V_{GS}| \quad (11)$$

For a given d_{max} and V_{2max} the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + R_g D_{SS}}{1 + R_g D_{SS} \frac{V_{2max}}{4d_{max} |V_P|}} \approx \frac{4d_{max} |V_P|}{V_{2max}} \quad (12)$$

valid only for $m > 1$. Note that the maximum distortion is reached only for minimum attenuation. Examples:

$$\begin{aligned} d_{max} = 10 \text{ percent } & V_{2max} = 0.001 V_P & m = 400 \\ d_{max} = 1 \text{ percent } & V_{2max} = 0.01 V_P & m = 4 \end{aligned}$$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to V_P . FETs with high V_P are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low V_P for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseriess, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if V_{GD} were the control voltage in the third quadrant. By adding $0.5 V_{DS}$ to the control voltage, the two voltage V_{GS} and V_{GD} interchange when V_{DS} changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5 V_{DS} \\ V_{GD} &= V_H - 0.5 V_{DS} \end{aligned} \quad (13)$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V_P^2} V_{DS} (V_H - V_P) \quad (14)$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1 V_P$ at $V_{GS} = 0.8 V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal V_H to keep the direct interference of V_H on V_2 small. R_3 is set for minimum distortion. If V_2 and V_H are in the same frequency range, a high impedance amplifier must be used. V_2 is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with V_2 occurs.

REFERENCES

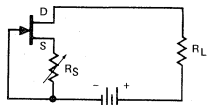
- (1) J. Watson, INTRODUCTION TO FIELD-EFFECT TRANSISTORS, Siliconix, Inc. Santa Clara, Calif. 95054 (1970), p. 58.
- (2) "FETs As Voltage-Variable Resistors," Carl D. Todd, ELECTRONIC DESIGN, Sept. 13, 1965, pp. 66-69.
- (3) Op. cit., AN INTRODUCTION TO FIELD-EFFECT TRANSISTORS, p. 22.
- (4) "FETs As Voltage-Controlled Resistors," Siliconix, inc., Santa Clara, Calif., 1966.
- (5) Op. cit., AN INTRODUCTION TO FIELD-EFFECT TRANSISTORS, p. 61.
- (6) W. Gosling, "Voltage Controlled Attenuators Using Field-Effect Transistors," IEEE Trans Audio, Vol. AU-13, pp. 112-120, Sept.-Oct., 1965.
- (7) J.S. Sherwin, "Voltage Controlled Resistors (FET)," Solid State Design, pp. 12-14, Aug. 1965.
- (8) L.J. Sevin, "Field-Effect Transistors," New York, McGraw-Hill, 1965.

DESIGN IDEA

The FET Constant Current Source

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.¹



Field-Effect Transistor Current Source
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current I_{DSS} .

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)} \left[1 - \left(\frac{I_D}{I_{DSS}} \right)^{1/k} \right] \quad (1)$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage, or change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss} .

$$\Delta I_D = \Delta V_{DS} g_{oss} \quad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant current source. As g_{oss} may range from less than $1 \mu\text{mho}$ to more than $50 \mu\text{mho}$ according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of $1 \mu\text{A}$ to $50 \mu\text{A}$ per volt. The value of g_{oss} depends also on the operating point, being highest at I_{DSS} and at low V_{DS} . Output conductance g_{oss} decreases approximately linearly with I_D , becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

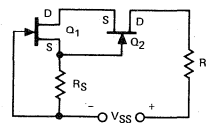
$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as $V_{GS} \gg V_{GS(off)}$, $g_{oss} \gg \text{zero}$. For best regulation, I_D must be considerably less than I_{DSS} .

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs as shown in Figure 2.



Cascade FET Current Source
Figure 2

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The d-c value of I_D is controlled by R_S and Q_1 . However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.

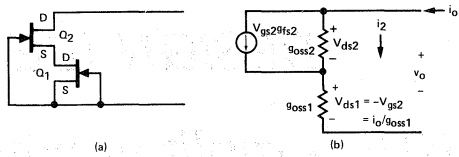


Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o \frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2} \frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \quad (13)$$

When

$R_S \neq 0$ as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \quad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}(1 + R_Sg_{fs})} \quad (16)$$

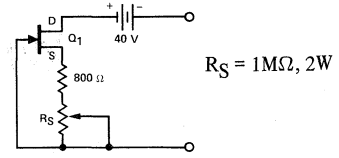
In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG} . That is,

$$V_{DG} > V_{GS(off)}, \text{ preferably } V_{DG} > 2 V_{GS(off)} \quad (17)$$

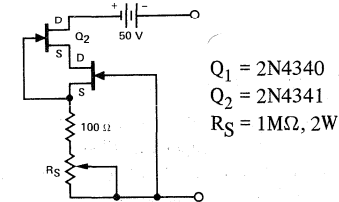
If $V_{DG} < 2V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A 2N4340 has typical $g_{oss} = 4 \mu\text{mho}$ at $V_{DS} = -20 \text{ V}$ and $V_{GS} = 0$. At $V_{DS} \approx -V_{GS(off)} = 2 \text{ V}$, $g_{oss} \approx 100 \mu\text{mho}$.

The best FETs for current sources are those having long gates and consequently very low g_{oss} . The Siliconix 2N4869 exhibits typical $g_{oss} = 1 \mu\text{mho}$ at $V_{DS} = 20 \text{ V}$. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from $5 \mu\text{A}$ to 1 mA with internal impedance greater than 2 megohms.



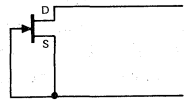
Adjustable Current Source Figure 4

The cascade circuit of Figure 5 provides a current adjustable from $2 \mu\text{A}$ to 1 mA with internal resistance greater than 10 megohms.

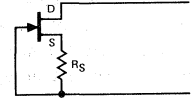


Cascade FET Current Source Figure 5

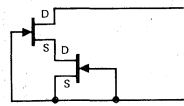
For each circuit discussed, g_{oss} is represented by the following equations:



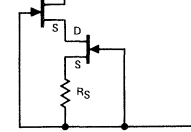
$$g_o = g_{oss}$$



$$g_o \approx \frac{g_{oss}}{1 + R_S g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}(1 + R_S g_{fs})}$$

REFERENCES

(1) "Biasing FETs for Zero DC Drift," Evans, L., *Electrotechnology*, August 1964.

DESIGN IDEA

Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

INTRODUCTION

A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.⁽¹⁾

Additionally, the high common-gate forward transconductance of the U310 (20,000 μmho maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit (g_m/C) of the FET is 2.35×10^9 typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

Forward Transconductance		14 mmhos
Input Admittance at 225 MHz	g_{igs}	13 mmhos
	b_{igs}	4 mmhos
Output Admittance at 225 MHz	g_{ogs}	0.27 mmhos
	b_{ogs}	2.6 mmhos

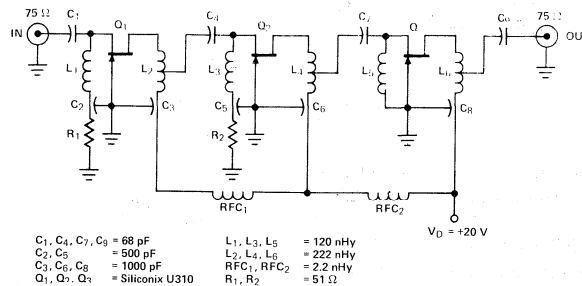


Figure 1

Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s \sqrt{\frac{R_{ig}}{R_s}} - 1 = X_s = 75 \sqrt{\frac{77}{75}} - 1 = 11.85 \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68 \text{ pF}$$

$$X_p = \frac{R_s R_p}{X_s} = \frac{75 \times 77}{11.85} = 488 \Omega$$

$$C_p = 1.47 \text{ pF}$$

$$C_T = 4.4 \text{ pF} (C_T = C_p + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120 \text{ nHy}$$

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:⁽²⁾

$$\frac{B/W}{f} = \frac{1}{Q} \sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}^{(3)}}{\text{Bandwidth of 1 Stage}} = \sqrt{2^{1/3} - 1}$$

and

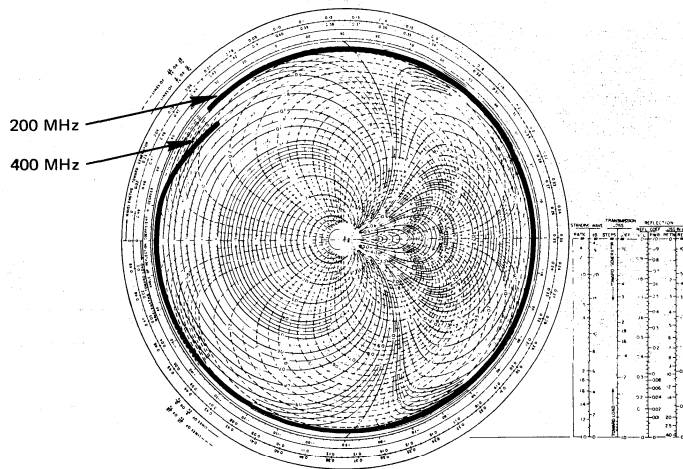
$$\left(\frac{E_o}{E}\right) = 1.122 \text{ (1 dB)}$$

giving

$$B/W \text{ (1 dB)} = 98 \text{ MHz}$$

$$Q = 1.15$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.



Blanchard Chart (Inverted Circle Impedance Chart)
Figure 2

With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega CR_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330 \Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222 \text{ nHy}$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately $g_{fs} R_t/n$ or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at I_{DSS} , and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.⁽⁴⁾ The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

REFERENCES

- (1) "Don't Guess the Spurious Level," ELECTRONIC DESIGN, February 1, 1967, pp. 70-73.
- (2) REFERENCE DATA FOR RADIO ENGINEERS, 4th ed., p. 242, ITT Corp., New York, N.Y.
- (3) Valley and Wallman, VACUUM TUBE AMPLIFIERS, MIT Rad. Lab. Series, Vol. 18, pp. 172-173.
- (4) Op. cit., "Don't Guess the Spurious Level."

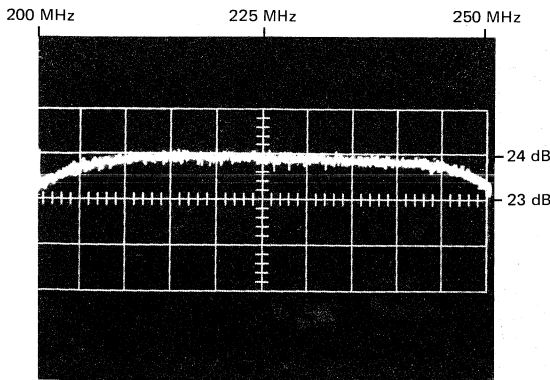


Figure 3

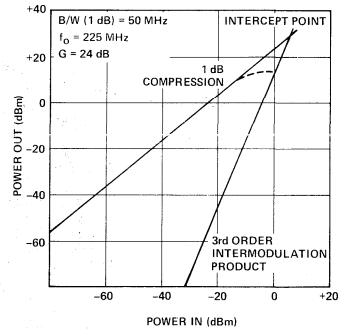


Figure 4

DESIGN IDEA

High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

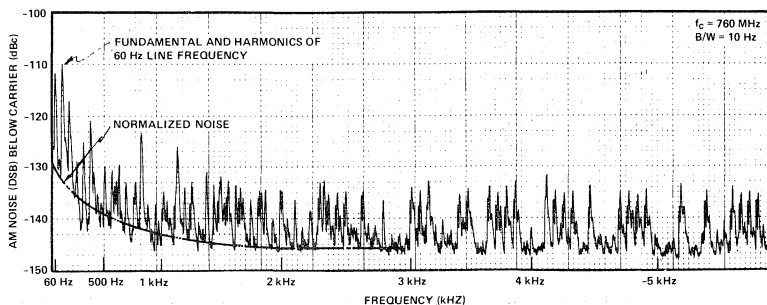
Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise ($1/f$); (2) thermal noise ($4kTRB$); and "shot" noise (i_n). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the $1/f$ decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic $(4kTBR)^{1/2}$. Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

Origins of Oscillator AM Noise

Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise ($1/f$). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to $1/f$. A graph of AM noise vs frequency removed is shown in Figure 1.

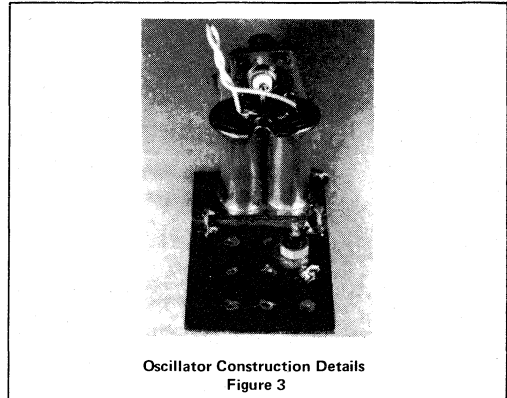
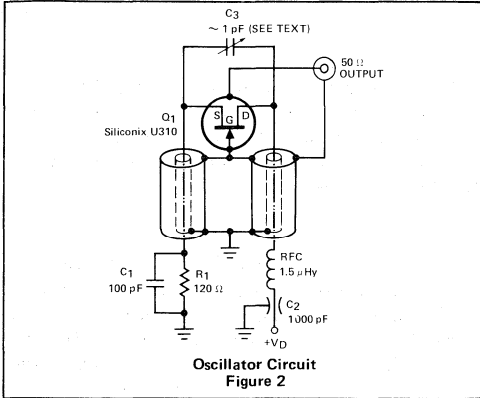


AM Noise vs Frequency Removed from the Carrier
Figure 1

Design of a VHF Oscillator

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ($V_{GS} = 0$). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short-circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known, X_C can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta l \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

Frequency of oscillation	= 760 MHz
FET b_{igs} (from data sheet)	= 16 mmho
Capacitance from b_{igs}	$C_{gs} = 3.4 \text{ pF}$
Allow for stray capacitance and the feedback network	$C_s = 1.5 \text{ pF}$
	<u>4.9 pF</u>

Thus $X_C = j 0.57$ (normalized to 75 Ω)

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081 λ . Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm (1.26 inches)} \tag{4}$$

In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

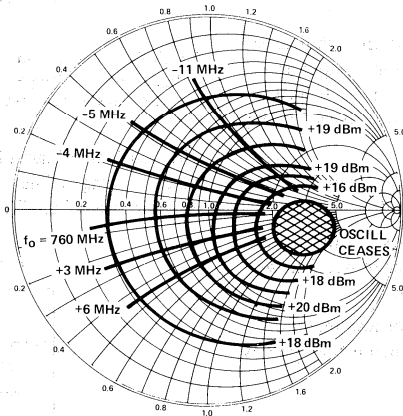
Conclusions

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

TABLE IA Oscillator Measured Performance @ 25°C				
V _{DD} (V)	+10	+15	+20	+25
I _D (mA)	15	16.2	18.2	21
P _{out} (dBm)	+6.6	+15.2	+18.3	+20
Frequency (MHz)	725	742.7	754.7	762.9

TABLE IB AM Noise Measurement	
Frequency Displaced From Carrier	dBc
50 Hz	-130
500 Hz	-139
1 kHz	-143.5
5 kHz	-146

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram
Figure 4

TECHNICAL ARTICLE

FET Biasing

James Sherwin

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the $V_{GS} = -0.4$ V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD} , of 30 V and a drain resistance, R_D , of $39\text{K}\ \Omega$ are being used.

The quiescent drain-to-source voltage, V_{DSQ} , is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ± 0.2 V will produce output voltage swings of ± 7.0 V — a voltage gain of 35.

Reprinted From ELECTRONIC DESIGN, May 24, 1970, June 7, 1970.

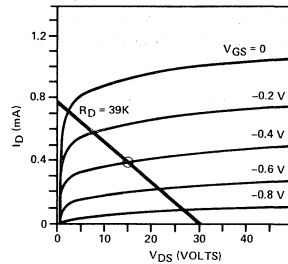


Figure 1. A large dynamic range is provided by the operating point at $V_{DSQ} = 15$ V, $I_{DQ} = 0.39$ mA and $V_{GSQ} = -0.4$ V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for $V_{GG} = \text{constant}$ on the transfer characteristic of the FET.

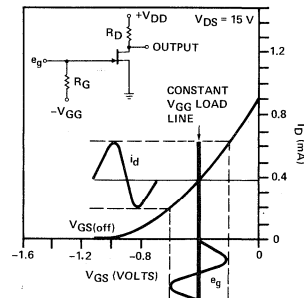


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical 2N4339 transfer curve. Input signal e_g moves the load line horizontally.

The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS} . Since the curve doesn't change much with changes in V_{DS} , it is quite useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at $V_{GS} = -0.4$ V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g , combine in series with V_{GS} so that they add algebraically to the fixed value of -0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled differential amplifiers, and to ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

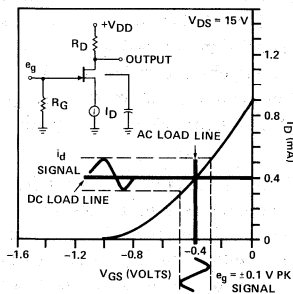


Figure 3. Constant-current bias fixes the output voltage for any R_D . Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

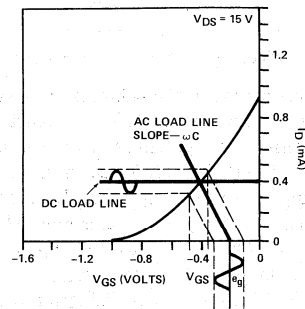


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g .

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g , is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_s = e_g - i_s X_C \quad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{gs} , the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S , to the gate. Since no voltage is dropped across R_S when $I_D = 0$, the self-bias load line passes through the origin. Its slope is given by $-1/R_S$. Therefore, the desired Q-point is established by setting $-1/R_S = I_{DQ}/V_{GSQ}$.

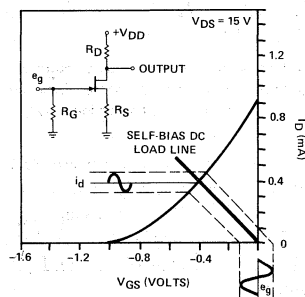


Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S . The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG} . (The bias line intercepts the V_{GS} axis at V_{GG} .) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

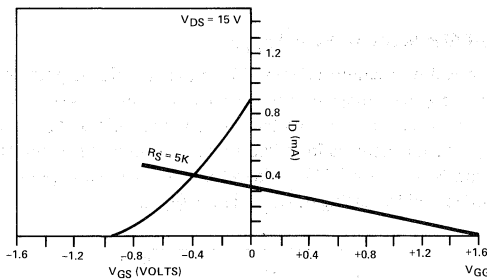
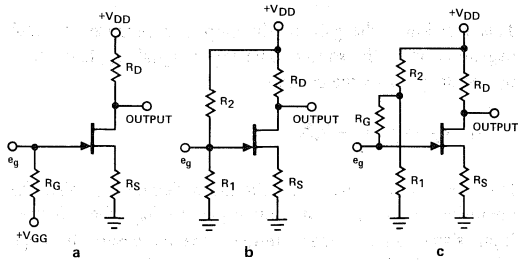


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore with low V_{DD} , there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7

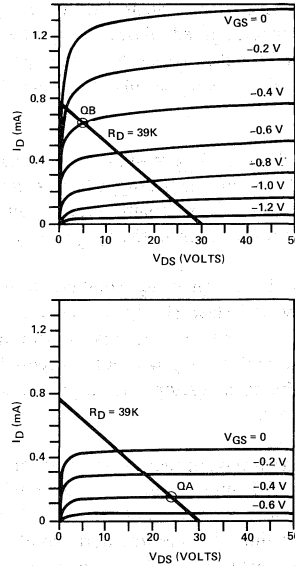


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance — for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At $V_{GS} = -0.4$ V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{DSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with $R_D = 39K \Omega$ and $V_{DD} = 30$ V, V_{DSQ} varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate $I_{DQ} = \text{constant}$ for all devices. For the constant-current bias plot of Figure 8, with $I_{DQ} = 0.39$ mA, V_{GS} would range from -0.11 to -0.67 V.

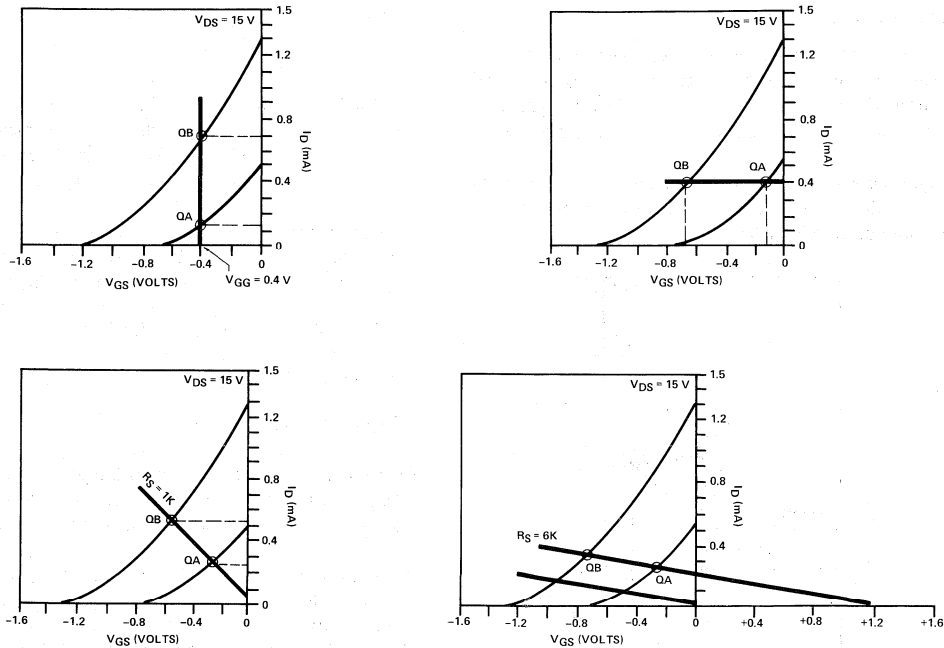


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS} . With $R_D = 39K \Omega$ and $V_{DD} = 30 V$, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs} , of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S .

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for $R_S = 1K \Omega$, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D . Clearly, for $R_D = 39K \Omega$, the maximum-limit device (device B) would operate with $V_{DSQ} = 9.8 V$ and the minimum-limit device (device A) would operate with $V_{DSQ} = 20.6 V$. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with $V_{GG} = 1.2 V$. The range of I_{DQ} for

this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with $R_S = 6K \Omega$ and $V_{GG} = 0$, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows $v_{gs} = \pm 1.8 V$ (limited by I_{DSSA}), while the lower line allows a v_{gs} of only $\pm 0.7 V$ (limited by $V_{GS(off)A}$). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with $R_D = 62K \Omega$, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of $(V_{DD} - 2V_{GS(off)typ})$ or 14 V, yields $R_D = (14 V / 0.285 mA) = 49K \Omega$.

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize the Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

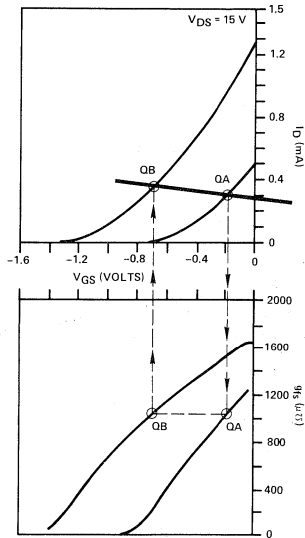


Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

- Step 1. Select a desired I_{DQA} below I_{DSSA} . A good value, allowing for temperature variations, is 60% of I_{DSSA} . This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.
- Step 2. Enter the transfer curves at $I_{DQA} \cong 0.6 I_{DSSA}$ (0.3 mA) to find V_{GSQA} . This $V_{GSQA} \cong 0.2$ V for the 2N4339.
- Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA} . The value as read from the plot is approximately 1000 μ mho.
- Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs} . This is $V_{GSQB} \cong -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB} . This is $I_{DQB} \cong 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG} .

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB}) / (I_{DQB} - I_{DQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_D(\text{intercept}) / -V_{GS}(\text{intercept}) \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B .

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ} . However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

- Step 1. Establish R_S and limiting values of I_{DQ} , V_{GSQ} and g_{fsQ} from the transfer curve.
- Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous V_{dg} be allowed to fall below $2 \times V_{GS(off)}$ if minimum distortion is to be achieved.
- Step 3. Set V_{DSQ} approximately midway between V_{DD} and $2 \times V_{GS(off)}$; lower if large output signals will not be handled.
- Step 4. Select R_D to give the appropriate V_{DSQ} . The formula is:

$$R_D = [(V_{DD} - V_{DSQ}) / 0.5 I_{DQA} + I_{DQB}] - R_S \quad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30-3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5$ $(0.52 + 0.24)$ mA $- 1K \Omega = 42.5K \Omega$.

- Step 5.** Check to ensure that with this R_D , device B is not in a saturated condition $- V_{DQB} = V_{DD} - I_{DBQ} R_D > 2V_{GS(off)} + R_S I_{DBQ}$.
Decrease R_D if this condition is not met.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

- Step 3.** Determine required stage gain, A_v , and set $R_D = A_v/g_{fsQ}$.
Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S) I_{DQ} \quad (6)$$

- Step 5.** If necessary, change I_{DQ} , V_{DD} , A_v and/or R_D to obtain an optimum compromise. ■

FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G . Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G .

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower cut-off voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS} , than Q_1 .
- Circuits e, g, h and k employ a source resistor, R_S , which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

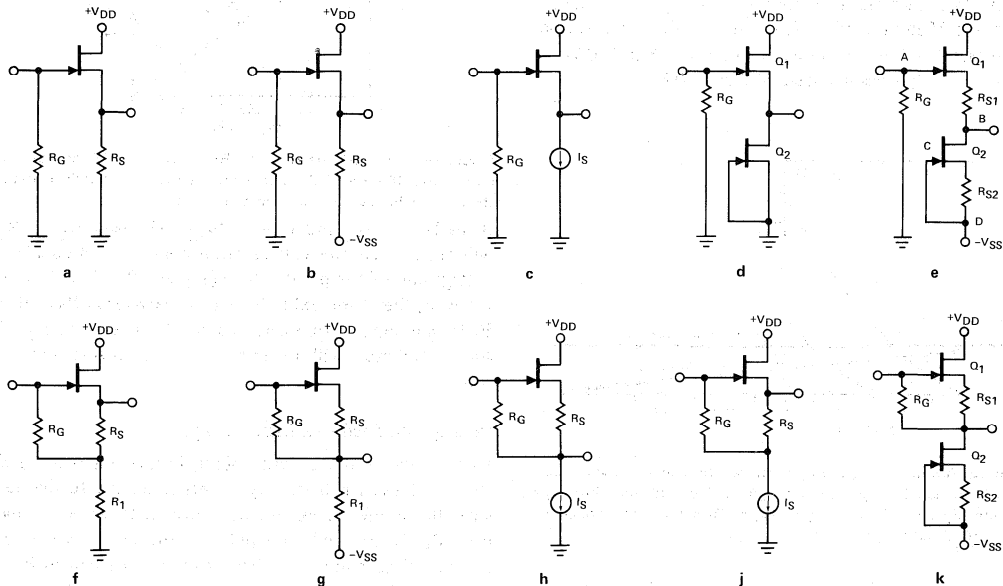


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e)) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G . Since no gate-to-source voltage, V_{GS} , can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K Ω source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

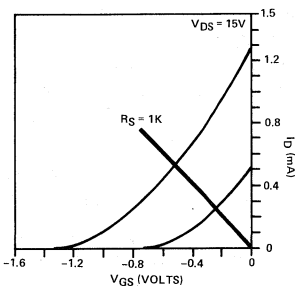


Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

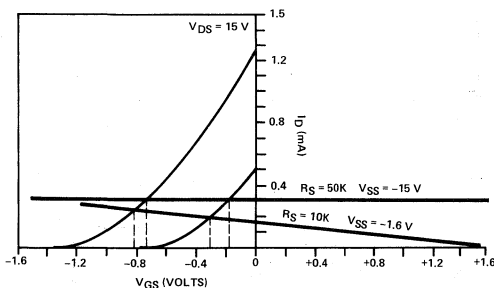


Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS} -axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

The bias load line for circuit 10(c) is just a horizontal line ($I_D = \text{constant}$). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 10(d) is similar to 10(c) except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(\text{off})}$ is significantly higher than the equivalent $V_{GS(\text{off})}$ of the current-source FET diode.

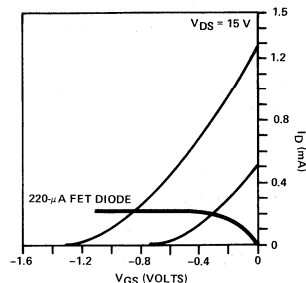


Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(\text{off})}$ than Q_2 does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2} , as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

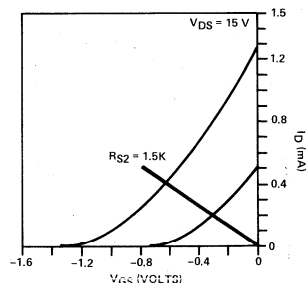


Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D , the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G . If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S .

Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB} , measured at the junction of R_S and R_1 , is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

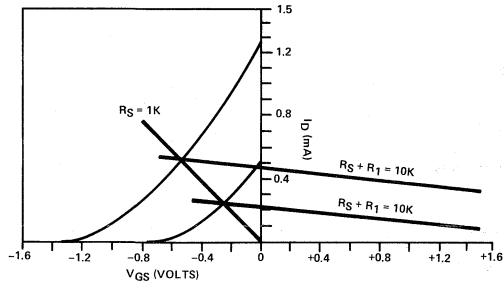


Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{fb} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 ohms and 2.5K Ω . R_S is much less than R_1 . The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

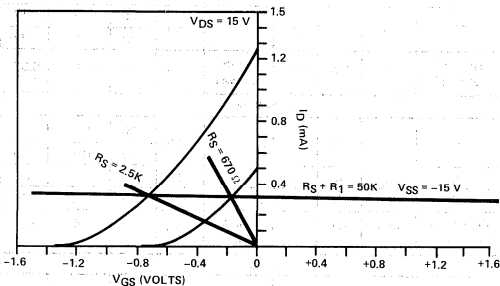


Figure 16. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5K Ω (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of $-1/50K$, because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of

circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of $-1/50k$.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K Ω source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For $R_S = 1K \Omega$, V_{FB} will be between -0.1 V and $+0.45$ V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

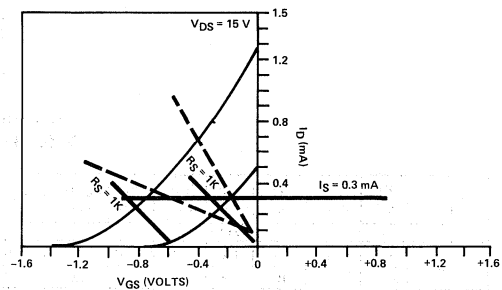


Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming R_S , as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

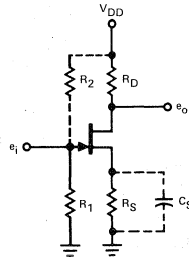
Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance. ■■

REFERENCES

- 1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design*, May 17, 1966, p. 94.
- 2) Sherwin, J.S., "Knowing the Cause Helps to Cure Distortion in FET Amplifiers," *Electronics*, Dec. 12, 1966, pp. 99-105.

Amplifier Charts

For convenience this chart offers the designer circuit values for a variety of commonly used J-FET amplifiers.



Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

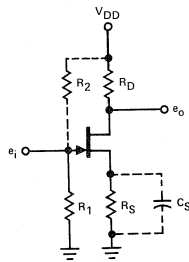
V _{DD} (V)	R _S (Ω)	R ₁ (MΩ)	R ₂ (MΩ)	C _S (μF)	I _{DD} (mA)	R _D (Ω)	e _o Max (V)	A _v
J111								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V _{DD} = 15 V _{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
V _{DD} = 15 V _{SS} = -15	7.5K	1	Source Follower		6	0	8.5	0.96
V _{DD} = 15 V _{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
J112								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V _{DD} = 15 V _{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
J113								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-65
V _{DD} = 15 V _{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
V _{DD} = 15 V _{SS} = -15	7.5K	1	Source Follower		1.5	0	13	0.98

V _{DD} (V)	R _S (kΩ)	R ₁ (MΩ)	R ₂ (MΩ)	C _S	I _{DD} (μA)	R _D (kΩ)	e _o Max (pK V)	A _v
2N4117								
10	10	1M	∞		45	120	1	5.7
20	10	1M	∞		45	270	1.5	12
						360	1	15
30	10	1M	∞		45	420	4	17
						620	1	22
V _{DD} = +15 V _{SS} = -15	510	1M	∞	Source Follower	35	0	8	0.97
2N4118								
10	8.2	1M	∞		120	36	0.6	2.2
						50	0.2	3.5
20	8.2	1M	∞		120	120	1	7.5
30	8.2	1M	∞		120	180	2	10
V _{DD} = +15 V _{SS} = -15	510	1M	∞	Source Follower	35	0	8	0.97
2N4119								
20	56	1	∞	5 μF* at 5 V	70	150	1	10
30	56	1	∞		70	240	3	17
					330	1	17-23	
20	6.8	1	∞		300	27	1	1.8
30	6.8	1	∞		300	68	2	4.5
V _{DD} = +15 V _{SS} = -15	510	1	∞	Source Follower	40	0	10	0.97

*AC Amplifier



APPLICATIONS (Cont'd)



Amplifier Design Chart

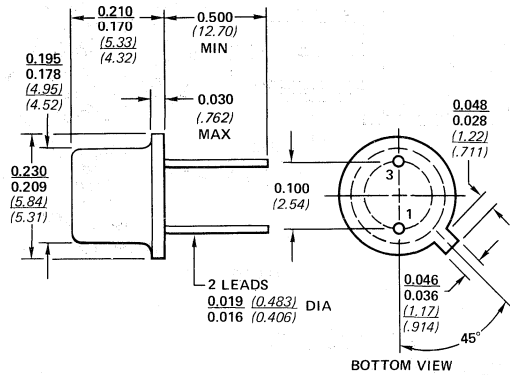
V _{DD} (V)	R _S (Ω)	R ₁ (Ω)	R ₂ (Ω)	C _S (μF)	I _{DD} (mA)	R _D (KΩ)	e _o Max (pk V)	A _V	
2N4338									
15	1500	1M	∞	0	0.25	36	2.5	9-12	
				30		36	1.5	16-24	
				47		2.0	20-30		
	5100	1M	∞	0	0.12	82	3.0	10-10.5	
				25		82	1.5	24-37	
				30		0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4.0	21.5-27	
				30		82	2.5	32-49	
				100		3.0	43-64		
	5100	1M	∞	0	0.12	150	4.5	14.5-16	
				25		150	2.5	38-54	
				30		200	1.5	40-50	
45	1500	1M	∞	0	0.25	120	6.5	27-33	
				30		120	4.0	45-68	
				25		270	10	28-31	
	5100	1M	∞	0	0.12	270	5.0	76-105	
				25		120	14	2.8	
				30		120	7.0	54-76	
V _{DD} = +15 V _{SS} = -15									
2N4339									
15	1800	1M	∞	0	0.42	20	3.0	7-7.5	
				40		20	2.0	17-22	
				27		2.0	23-27		
	9100	1M	6.8M	35	0.32	18	2.0	17-19	
				25		30	2.5	26-28	
				0.2		22	1.0	16-18	
30	1800	1M	∞	0	0.42	47	6.5	15-17	
				40		47	4.0	38-47	
				51		4.5	40-50		
	9100	1M	13M	35	0.32	43	8.0	4.5	
				25		43	5.0	40-43	
				0.2		68	4.5	53-60	
45	1800	1M	∞	0	0.42	68	4.0	49-52	
				40		100	7.0	66-70	
				25		75	7.5	23-25	
	9100	1M	22M	35	0.32	75	5.0	58-70	
				25		100	7.0	73-77	
				0.2		68	7.0	7.0	
27K	1M	12M	25	0.2	120	7.0	80-85		
					100	12	3.3		
					100	5.0	65-68		
	V _{DD} = +15 V _{SS} = -15								
	2N4341								
	15	1000	1M	∞	70	2.7	2	1.0	3-3.5
80					2.7		2.0	4-4.5	
3.5					1.2		2.0	2.5	
1200		1.2M	7.5M	80	1.8	2.2	3.0	3-4.5	
				65		3	2.0	4-4.5	
				0		4.7	1.5	6-6.5	
30	1000	1M	∞	70	2.7	6.2	7.0	4.0	
				80		6.2	3.5	10	
				3.5		9.1	1.5	11-13	
	1200	1.1M	15M	80	1.8	3.9	4.0	7.5-8	
				65		9.1	6.0	3.0	
				0		9.1	4.0	12	
45	15K	1M	3.3M	50	0.7	15	1.0	13-19	
				70		18	3.0	16-21	
				3.5		6.8	7.0	13	
	1000	1M	∞	70	2.7	10	8.5	6.3	
				80		10	6.0	16	
				1.8		6.8	7.0	13	
1200	1M	22M	80	0.7	15	8.5	5.5		
			65		15	5.0	20-21		
			0		30	9.0	28-35		
V _{DD} = +15 V _{SS} = -15									
2N4340									
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4	
				65		5.1	1.5	7-8.5	
				1.1		6.8	2.0	9-10.5	
				0		7.5	2.5	3.5-4	
				60		7.5	2.0	9-11	
				0		10	2.0	11-13	
	1200	1M	∞	0	0.4	18	4.0	3.5-4	
				40		18	1.5	15-18	
				1.1		22	1.0	19-22	
				0		12	6.0	9.5-10	
				65		12	3.0	17-22	
				0		18	1.0	24-26	
30	680	1M	∞	0	1.5	18	6.0	9-9.5	
				65		18	6.0	9-9.5	
				1.1		18	4.0	21-26	
				0		24	2.0	29	
				60		39	7.0	7.5-8	
				0.4		39	7.0	30-36	
	1200	1M	∞	0	0.4	62	0.5	34-45	
				40		30	3.0	25-27	
				1.1		56	6.5	40	
				0		20	10.5	14-15.5	
				65		20	8.0	27-32	
				0		27	4.0	35	
20K	1M	6.8M	35	0.35	27	12.5	16-18		
					60	27	5.0	30-37	
					0.4	39	2.0	39-42	
					0	68	12	12-13	
					1.0	68	7.0	52-61	
					0	91	3.0	56-63	
V _{DD} = +15 V _{SS} = -15									

V _{DD} (V)	R _S (Ω)	R ₁ (Ω)	R ₂ (Ω)	C _S (μF)	I _{DD} (mA)	R _D (KΩ)	e _o Max (pk V)	A _V
2N4340								
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4
				65		5.1	1.5	7-8.5
				1.1		6.8	2.0	9-10.5
				0		7.5	2.5	3.5-4
				60		7.5	2.0	9-11
				0		10	2.0	11-13
	1200	1M	∞	0	0.4	18	4.0	3.5-4
				40		18	1.5	15-18
				1.1		22	1.0	19-22
				0		12	6.0	9.5-10
				65		12	3.0	17-22
				0		18	1.0	24-26
30	680	1M	∞	0	1.5	18	6.0	9-9.5
				65		18	6.0	9-9.5
				1.1		18	4.0	21-26
				0		24	2.0	29
				60		39	7.0	7.5-8
				0.4		39	7.0	30-36
	1200	1M	∞	0	0.4	62	0.5	34-45
				40		30	3.0	25-27
				1.1		56	6.5	40
				0		20	10.5	14-15.5
				65		20	8.0	27-32
				0		27	4.0	35
20K	1M	6.8M	35	0.35	27	12.5	16-18	
					60	27	5.0	30-37
					0.4	39	2.0	39-42
					0	68	12	12-13
					1.0	68	7.0	52-61
					0	91	3.0	56-63
V _{DD} = +15 V _{SS} = -15								
2N4341								
15	1000	1M	∞	70	2.7	2	1.0	3-3.5
				80		2.7	2.0	4-4.5
				3.5		1.2	2.0	2.5
	1200	1.2M	7.5M	80	1.8	2.2	3.0	3-4.5
				65		3	2.0	4-4.5
				0		4.7	1.5	6-6.5
30	1000	1M	∞	70	2.7	6.2	7.0	4.0
				80		6.2	3.5	10
				3.5		9.1	1.5	11-13
	1200	1.1M	15M	80	1.8	3.9	4.0	7.5-8
				65		9.1	6.0	3.0
				0		9.1	4.0	12
45	15K	1M	3.3M	50	0.7	15	1.0	13-19
				70		18	3.0	16-21
				3.5		6.8	7.0	13
	1000	1M	∞	70	2.7	10	8.5	6.3
				80		10	6.0	16
				1.8		6.8	7.0	13
1200	1M	22M	80	0.7	15	8.5	5.5	
			65		15	5.0	20-21	
			0		30	9.0	28-35	
V _{DD} = +15 V _{SS} = -15								

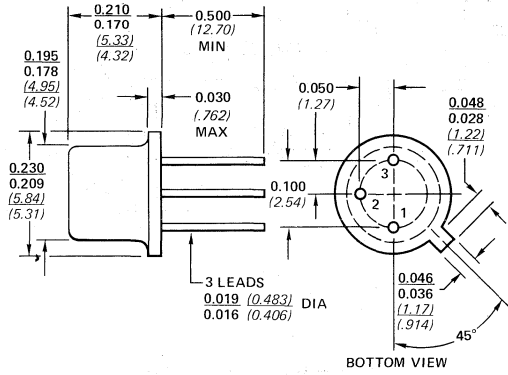
Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

Mechanical Data

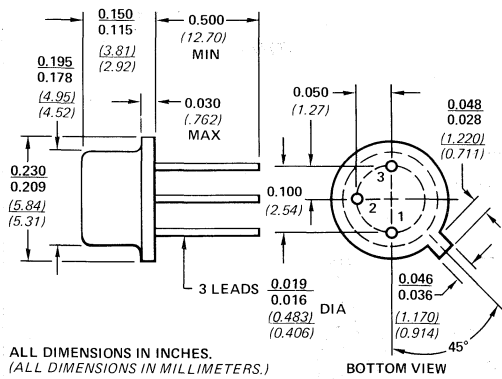
At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



**TO-18
(2 PIN)**

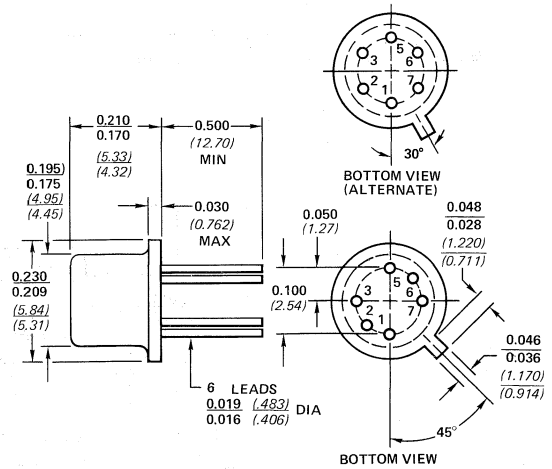


**TO-18
(3 PIN)**



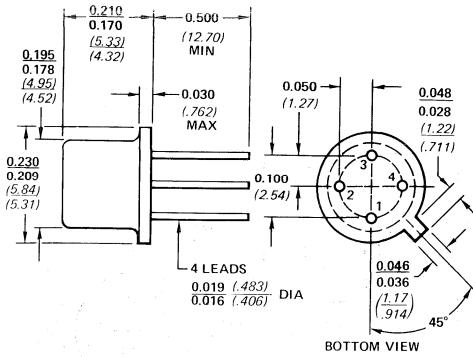
ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-52

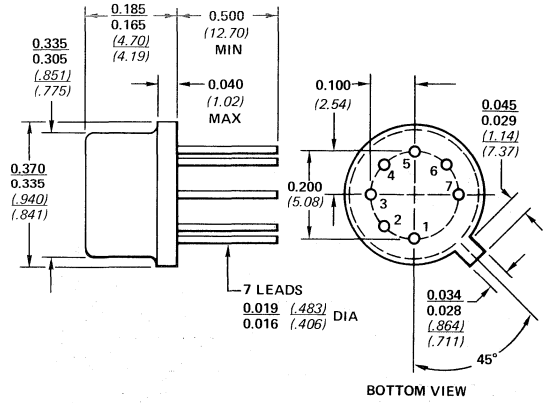


TO-71

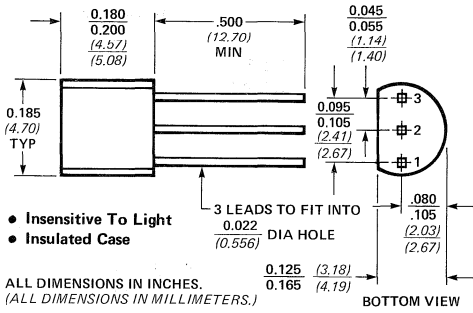
Mechanical Data (Cont'd) At Siliconix' option, lead finish will be either Gold Plate or Tin Plate. Electrical Characteristics are not affected.



TO-72



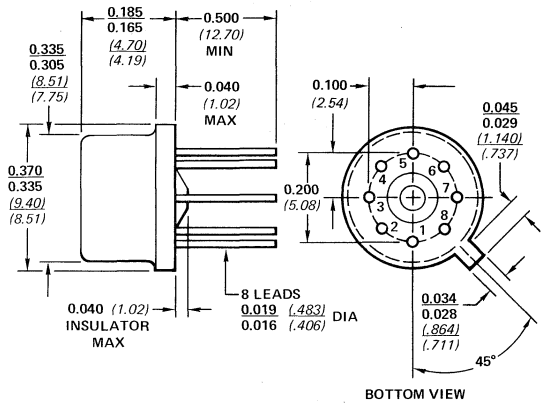
TO-78



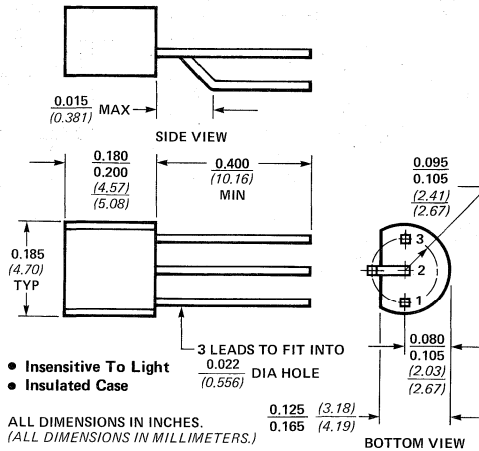
- Insensitive To Light
- Insulated Case

ALL DIMENSIONS IN INCHES.
 (ALL DIMENSIONS IN MILLIMETERS.)

TO-92



TO-99



- Insensitive To Light
- Insulated Case

ALL DIMENSIONS IN INCHES.
 (ALL DIMENSIONS IN MILLIMETERS.)

TO-92 LEAD FORM
 (-18)

Publications Index

Catalog (See Key)	Document Number	Title	Catalog (See Key)	Document Number	Title
Application Notes					
	AN70-1	FET Cascode Circuits Reduce Feedback Capacitance	M	* AN80-1	A Key to the Advance of Switching Power Supplies
F	AN70-2	FETs for Video Amplifiers	M	AN80-2	Meet the VMOS FET Model
	AN71-1	A High Resolution CMRR Test Method		AN80-3	Ultralinear Broadband Amplifier
F	AN72-1	FETs in Balanced Mixers		AN80-4	Enjoy VHF Power Amplifier Design
A	AN72-2	FETs as Analog Switches		AN80-6	AGC for the VMOS RF Power Amplifier
F	AN73-1	FETs as Voltage-Controlled Resistors	AIC	AN80-8	Function/Application of the LD122/LD121A $\pm 4\frac{1}{2}$ Digit A/D Converter Set in Measurement Systems
A	AN73-2	IC Multiplexer Increases Analog Switching Speeds	AIC	AN81-1	Microprocessor Interface Techniques As Applied to the Siliconix A/D Converter Family
	AN73-3	Switching High-Frequency Signals With FET Integrated Circuits	AIC	AN81-2	Introduction to Quantized Feedback
	AN73-4	Junction FETs in Active Double-Balanced Mixers	F	*AN81-3	Composite Op Amp for High Performance
A	* AN73-5	Driver Circuits for the JFET Analog Switch	Design Aids		
AIC	AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp	AIC	* DA77-2	Design Aid of the LD120/LD121 $4\frac{1}{2}$ Digit DVM
F, A	* AN73-7	An Introduction to FETs		DA78-4	Build a Smoke Detector With the SM110 IC
AIC	* AN74-1	Function/Application of the LD110/LD111 $3\frac{1}{2}$ Digit A/D Converter Set	M	* DA80-1	A Low Cost Regulator for Microprocessor Applications
A	AN74-2	Analog Switches in Sample and Hold Circuits		DA81-1	Logic Interfacing Made Easy with the DG308
	AN74-3	Designing Junction FET Input Op Amps		DA81-2	Logic Interfacing Made Easy with the DG308
F	* AN74-4	Audio-Frequency Noise Characteristics of Junction FETs	F	* DI71-1	The FET Constant Current Source
A	* AN75-1	CMOS Analog Switches—A Powerful Design Tool		DI71-4	Wideband Mixer-Preamplifier Using FETs
	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET		DI71-5	A FET Frequency Doubler
A	* AN76-6	DG300 Series Analog Switch Applications		DI71-6	Using FETs in Selective VHF Amplifiers
AIC	* AN76-7	Function/Application of the L161 Micropower Comparator		DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
AIC	* AN77-1	Function/Application of the LD120/LD121 $4\frac{1}{2}$ Digit A/D Converter Set in Measurement Systems	F	DI71-9	Wideband UHF Amplifier with High Performance FETs
M	* AN77-2	Don't Trade Off Analog Switch Specs. VMOS — A Solution to High Speed, High Current, Low Resistance Analog Switches	F	* DI73-2	High Performance FETs in Low-Noise VHF Oscillators
M	* AN79-1	A 500 KHz Switching Inverter for 12 V Systems		DI80-1	A 5 Watt, Parallel-Mode Crystal Oscillator
M	* AN79-3	Dynamic Input Characteristics of a VMOS Power Switch		TA70-1	High Frequency Junction FET Characterization and Application
M	* AN79-4	Driving VMOS FETs	F	* TA70-2	FET Biasing
	AN79-5	Using the VN64GA High Current, High Power VMOS Power FET	A	* TA73-1	Multiplexer Adds Efficiency to 32-Channel Telephone System
M	* AN79-6	Using Power MOSFET Transistors to Interface from IC Logic to High Power Loads	A	TA73-2	Designing with Monolithic FET Switches
	AN79-7	Applications of the VN10KM VMOS Power FET		TA76-1	VMOS Power FETs in Your Next Broadband Driver

Publications Index (Cont'd)

Catalog (See Key)	Document Number	Title
	TA76-2	A New Technology: Application of VMOS Power FETs for High Frequency Communications
M	*TA82-1	The Autobias Amplifier

Catalogs

- Analog Switch & IC Product Data Book
- Analog Switches and Their Applications (\$7.95 charge)
- FET Design Catalog
- MOSPOWER® FET Design Catalog
- OEM Pricing with Cross Reference
- RF Power FET Short Form Catalog
- Siliconix Short Form Selector Guide

Key

Catalogs

- | | |
|--|----------------------------------|
| AIC = Analog Switch & IC Product Data Book | F = FET Design Catalog |
| A = Analog Switches and Their Applications | M = MOSPOWER® FET Design Catalog |

*Available in bound catalog only.

Title

Reprints & Reports

- Siliconix, Inc. Annual Report.
- Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Powercon 3/78*
- Designing with CODECs: Know Your A's and μ 's. Thomas J. Mroz, *EDN 5/76*
- Log Data under μ Control. Gary Grandbois, *Electronic Design 5/76*
- Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics 6/78*
- CODEC has On-Chip Signaling for Phone Applications, Walter Heinzer and Steve Bolger, *Electronics 6/7/79*
- A Microprocessor Controlled VMOS Power Supply, David C. Hoffman
- Control Analog Signals with Voltage, Stephen Moore, *Electronic Design, 1978*
- Exploit VMOS FETs' Advantages to Drive Bipolar Power Transistors, F. Michael Barlage, *Powercon 5/78*
- Rely on IC Analog Switches for Fast Small-Signal Control, *EDN, August 5, 20, Sept. 5, 1980*
- Composite Op Amp Outperforms FET-input ICs, *EDN, May 27, 1981.*

Books

Designing with Field-Effect Transistors, Edited by Arthur D. Evans. Available at your technical bookstore or write to Suite 26-1; McGraw-Hill Book Co.; 1221 Avenue of the Americas; New York, NY 10020.

Power FETs and Their Applications, by Edwin S. Oxner. Available at your technical bookstore or write to: Mail Order Billing, Prentice-Hall, Inc., Tappan Road, Old Tappan, NJ 07675.

Glossary of Terms and Abbreviations



1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg}	= Common-Gate Forward Susceptance	C_{sb}	= Source-Body Capacitance
b_{fs}	= Common-Source Forward Susceptance	C_{sd}	= Source-Drain Capacitance
b_{igs}	= Common-Gate Input Susceptance	C_{sgo}	= Source-Gate Capacitance
b_{iss}	= Common-Source Input Susceptance	D	= Drain
b_{ogs}	= Common-Gate Output Susceptance	\bar{e}_N	= Equivalent Short Circuit Input Noise Voltage
b_{oss}	= Common-Source Output Susceptance	f_m	= Figure of Merit
b_{rg}	= Common-Gate Reverse Susceptance	G	= Gate
b_{rs}	= Common-Source Reverse Susceptance	g_{fg}	= Common-Gate Forward Transconductance
BV_{DGO}	= Drain-Gate Breakdown Voltage	g_{fs}	= Common-Source Forward Transconductance
BV_{DSS}	= Drain-Source Breakdown Voltage	g_{fso}	= Common-Source Forward Transconductance @ $V_{GS} = 0$
BV_{SDX}	= Drain-Source Breakdown Voltage	g_{fs1/g_{fs2}}	= Common-Source Forward Transconductance Ratio
BV_{G1SS}	= Gate 1 to Source Breakdown Voltage	g_{ig}	= Common-Gate Input Conductance
BV_{G2SS}	= Gate 2 to Source Breakdown Voltage	g_{is}	= Common-Source Input Conductance
BV_{GSS}	= Gate-Source Breakdown Voltage	g_{og}	= Common-Gate Output Conductance
BV_{SDS}	= Source-Drain Breakdown Voltage	g_{os}	= Common-Source Output Conductance
BV_{SGO}	= Source-Gate Breakdown Voltage	g_{oss}	= Common Source Output Conductance @ $V_{GS} = 0$
C_{db}	= Drain-Body Capacitance	g_{os1-g_{os2}}	= Differential Output Conductance
C_{dgo}	= Drain-Gate Capacitance	G_{pg}	= Common-Gate Power Gain
C_{gb}	= Gate-Body Capacitance	G_{ps}	= Common-Source Power Gain
C_{gd}	= Gate-Drain Capacitance	I_{D(off)}	= Drain Cutoff Current
C_{gs}	= Gate-Source Capacitance	I_{D(on)}	= Drain ON Current
C_{iss}	= Common-Source Input Capacitance	I_{DGO}	= Drain-Gate Leakage
C_{oss}	= Common-Source Output Capacitance		
C_{rss}	= Common-Source Reverse Transfer Capacitance		

Glossary of Terms and Abbreviations (Cont'd)

I_{DSS}	= Saturation Drain Current	$t_{d(on)}$	= Turn-On Delay Time
I_{DSS1}/I_{DSS2}	= Saturation Drain Current Ratio	t_f	= Fall Time
I_F	= Forward Current	T_j	= Junction Temperature
I_G	= Gate Operating Current	t_{off}	= Turn-Off Time
I_{G1G2}	= Gate to Gate Leakage Current	t_{on}	= Turn-On Time
$ I_{G1}-I_{G2} $	= Differential Gate Operating Currents	T_l	= Lead Temperature
I_{GBS}	= Gate to Body Leakage Current	t_r	= Rise Time
$I_G(f)$	= Gate Forward Current	T_{stg}	= Storage Temperature
I_{GSS}	= Gate Reverse Current	V_B	= Body Voltage
I_{G1SS}	= Gate 1 to Source Leakage Current	V_{BB}	= Body Supply Voltage
I_{G2SS}	= Gate 2 to Source Leakage Current	V_D	= Drain Voltage
I_{G1SSR}	= Gate 1 to Source Reverse Leakage Current	V_{DD}	= Drain Supply Voltage
I_{G2SSR}	= Gate 2 to Source Reverse Leakage Current	$V_{DS(on)}$	= Drain-Source ON Voltage
\bar{I}_n	= Equivalent Open-Circuit Noise Current	V_G	= Gate Voltage
I_p	= Pinch-Off Current	V_{GG}	= Gate Supply Voltage
NF	= Noise Figure	V_{GS}	= Gate-Source Voltage
P_D	= Continuous Power Dissipation	$ V_{GS1}-V_{GS2} $	= Differential Gate-Source Voltage
POV	= Peak Operating Voltage	ΔV_{GS}	= Differential Gate-Source Voltage
$r_{ds(on)}$	= Drain-Source ON Resistance	$\frac{\Delta V_{gs1}-V_{gs2} }{\Delta T}$	= Differential Gate-Source Voltage Change with Temperature
$r_{DS(on)}$	= Static Drain-Source ON Resistance	$V_{GS}(f)$	= Gate-Source Forward Voltage
$Re(Y_{fg})$	= Common-Gate Forward Transconductance	$V_{GS}(th)$	= Gate Threshold Voltage
$Re(Y_{fs})$	= Common-Source Forward Transconductance	$V_{GS}(off)$	= Gate Source Cutoff Voltage
$Re(Y_{ig})$	= Common-Gate Input Conductance	$V_{G1S}(off)$	= Gate 1 to Source Cutoff Voltage
$Re(Y_{is})$	= Common-Gate Output Conductance	$V_{G2S}(off)$	= Gate 2 to Source Cutoff Voltage
$Re(Y_{os})$	= Common-Source Output Conductance	V_S	= Source Voltage
$Re(Y_{rg})$	= Common-Gate Reverse Transconductance	V_{SS}	= Source Supply Voltage
$Re(Y_{rs})$	= Common-Source Reverse Transconductance	Z_d	= Dynamic Impedance
r_{GS}	= Common-Source Input Resistance	Z_k	= Knee AC Impedance
S	= Source	θ_l	= Current Temperature Coefficient
t_d	= Delay Time	θ_{J-A}	= Junction to Ambient Thermal Resistance
$t_{d(off)}$	= Turn-Off Delay Time	θ_{J-C}	= Junction to Case Thermal Resistance

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
MOSPOWER	7
Worldwide Sales Offices	8

Introduction

Siliconix is committed to your future system designs. As a multinational semiconductor manufacturer, we offer some of the industry's broadest product lines. No one gives you more analog switch ICs and power FETs to choose from. Our multiple technologies include DMOS, VMOS, CMOS, PMOS, PMOS/bipolar and bipolar. And we are constantly advancing semi-custom state-of-the-art technology.

MOSPOWER FETs

MOSPOWER identifies the "up front" technology that places Siliconix among the leaders in power device development for the 1980's, and has helped make Siliconix *the Discovery Company*.

MOSPOWER is a generic name coined by Siliconix to identify not only Siliconix's expanding family of medium and high power MOSFETs, but *all* power MOSFETs. The name also covers the many technologies used in the manufacture of these power MOSFETs which have been identified by various trade names. Vertical DMOS (double-diffused MOS); metal-gate V-groove MOS for high-frequency; lateral DMOS technology for FET arrays — all are covered by this generic name: MOSPOWER.

RF POWER FETs

MOSPOWER shadow-mask vertical technology is used to manufacture the only true power MOS transistors. The technology enables their use as RF broadband amplifiers in the 2MHz to 200MHz region, providing output powers from 2 to 120 watts. Devices are available for 12.5V or 28V operation and in a variety of packages to suit different needs. They offer the advantages of high stage gain, low baseband noise and immunity to burn-out due to mismatch. The latest addition is the 35V single-side-band 2-30MHz series.

Analog Switch ICs

Siliconix JFET, MOSFET and Integrated Circuit (IC) technologies have been utilized to produce an extensive family of Analog Switch ICs. They are used in many high-reliability military and aerospace applications such as Mercury, Gemini, Apollo and Skylab manned space programs. The family of analog switch ICs includes monolithic multi-channel switches with integral drivers. Also high performance JFET switches packaged with IC drivers offering very low ON-resistance, fast switching, excellent frequency response (DG180 series); low spike feed-through, low leakage and high OFF-isolation (DG281); low cost, single or dual supply operation (DG308, DG211); low consumption CMOS switches (DG300 series) and multiplexers with up to 16 channels (DG506A). The recent addition to the range of analog switch ICs is the Plus-40 enhanced DG5040 series with guaranteed safe operation up to 44V, and DG243CJ, the dual make-before-break equivalent of the DG5043CJ.

LSI/Linear Circuits

Siliconix is an industry leader in telecommunications circuits, A/D conversion and micropower linears. The Company's LSI or linear ICs are incorporated in products ranging from sophisticated instrumentation to consumer smoke detectors. Advanced processing capabilities used in the manufacture of such ICs range from high and low voltage CMOS to bipolar-PMOS. High reliability processing procedures combined with volume production capabilities complement state-of-the-art products.

Introduction (Cont'd)

Telecommunications

Siliconix is a high-technology manufacturer of complex, highly specialized integrated circuits for the telecommunications industry. The current product lines use the CMOS process to satisfy the low power requirements of the telecom industry. Our Loop Disconnect Dialer Circuits offer subscribers push-button dialing privileges even with exchange systems presently tied to the rotary dial pulse timing.

High-Reliability Devices

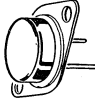
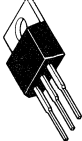
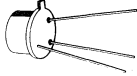



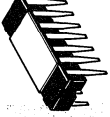

Siliconix's capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the Company's qualifications as a supplier for important European projects that include Ariane, Concorde, European Airbus, the Alpha Jet and Tornado Aircraft, also Apollo, Viking and Voyager space projects.

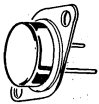
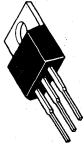
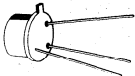


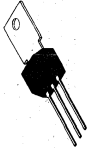


Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include screening to BS9000 for analog switches and CECC standards for FETs, also MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX and JANTXV processing, as well as an increasing number of QPL-listed analog switches. Special additional inspections and controls can be met and Siliconix can supply SEM-qualified products to meet individual customer requirements.

MOSPOWER Prime Products Selector Guide

MOSPOWER Prime Products Selector Guide

* 200°C RATING

Packages:								
	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
450-500	IRF450 13A, 0.4 Ω	IRF840 8A, 0.85 Ω						
	IRF440 8A, 0.85 Ω	VN5001D//IRF830 4A, 1.5 Ω						
	VNP002A* 6.5A, 1.5 Ω	IRF820 2.5A, 3 Ω						
	VN5001A//IRF430 4A, 1.5 Ω							
	IRF350 15A, 0.3 Ω	IRF740 10A, 0.55 Ω						
350-400	IRF340 10A, 0.55 Ω	VN4000D//IRF730 6A, 1.0 Ω						
	VNM001A* 8A, 1.0 Ω	IRF720 3A, 1.8 Ω						
	VN4000A//IRF330 6A, 1.0 Ω							
	IRF250 30A, 0.085 Ω	IRF640 18A, 0.18 Ω	VN2406B 0.8A, 6 Ω	VN2406M 0.3A, 6 Ω	VN2406L 0.21A, 6 Ω			
150-240	IRF240 18A, 0.18 Ω	IRF630 9A, 0.4 Ω		VN2410M 0.25A, 10 Ω	VN2410L 0.16A, 10 Ω			
	IRF230 9A, 0.4 Ω	IRF620 5A, 0.8 Ω						
	IRF220 5A, 0.8 Ω	VN2406D 1.4A, 6 Ω						

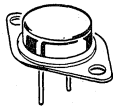
Packages:								
BV _{DSS} (Volts)	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
100-120	IRF150 40A, 0.055Ω	IRF540 27A, 0.085Ω	IRFF120 6A, 0.30Ω	VN1206M 0.3A, 6Ω	VN1206L 0.21A, 6Ω			
	IRF140 27A, 0.085Ω	VN1200D/IRF530 12A, 0.18Ω	IRFF122 5A, 0.40Ω	VN1210M 0.25A, 10Ω	VN1210L 0.16A, 10Ω			
	VN1200A/IRF130 12A, 0.18Ω	IRF520 8A, 0.30Ω	VN1206B 0.8A, 6Ω	VP1008M 0.37A, 5Ω	VP1008L 0.4A, 5Ω			
		VN1206D 1.4A, 6Ω	VP1008E 0.9A, 5Ω					
		VN0800A 12A, 0.18Ω	VN0800D 12A, 0.18Ω	2N6651 0.9A, 4Ω	VN0808M 0.35A, 4Ω	VP0308L 0.37A, 5Ω	VN88AF 1.5A, 4Ω	VQ1006P 0.40A, 4.5Ω
80-90	2N6658 1.9A, 4Ω	VN88AD 1.7A, 4Ω	VP0308E 0.9A, 5Ω	VP0308M 0.37A, 5Ω		VN80AF 1.3A, 5Ω	VQ2006P 1.3A, 5Ω	VQ2006J 1.3A, 5Ω
	IRF151 40A, 0.55Ω	IRF541 27A, 0.085Ω	IRFF121 6A, 0.30Ω	VN0606M 0.4, 3Ω	VN0610L 0.2A, 5Ω	VN66AF 1.7A, 3Ω	VQ1004P 0.46A, 5.5Ω	VQ1004J 0.46A, 5.5Ω
	IRF141 27A, 0.085Ω	VN0600D 16A, 0.12Ω	IRFF123 5A, 0.40Ω	VN10KM 0.3A, 5Ω	VN2222L 0.15A, 7.5Ω	VN67AF 1.6A, 3.5Ω	VQ1000P 0.225A, 3.5Ω	VQ1000J 0.225A, 3.5Ω
	VN0600A 16A, 0.12Ω	IRF531 14A, 0.18Ω	2N6650 1.1A, 3Ω	VN2222KM 0.25A, 7.5Ω			VQ2004P 1.3A, 5Ω	VQ2004J 1.3A, 5Ω
	IRF131 14A, 0.18Ω	IRF521 8A, 0.30Ω	VN67AB 1A, 3.5Ω					
30-40	2N6657 2A, 3Ω	VN66AD 1.9A, 3Ω						
	VN0400A 16A, 0.12Ω	VN0400D 16A, 0.12Ω	2N6659 1.4A, 1.8Ω	VN0300M 0.7A, 1.2Ω		VN48AF 1.6A, 3Ω	VQ1001P 0.85A, 1.0Ω	VQ1001J 0.85A, 1.0Ω
	2N6656 2A, 1.8Ω	VN0300D 2.5A, 1.5Ω	VP0300E 1.3A, 2.5Ω	VP0300M 0.48A, 2.5Ω		VN40AF 1.3A, 5Ω	VQ2001P 1.3A, 2Ω	VQ2001J 1.3A, 2Ω
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P 30V, 3Ω Total	VQ3001J 30V, 3Ω Total
							VQ7254P 20V, 3Ω Total	VQ7254J 20V, 3Ω Total

MOSPOWER Selector Guide



N-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	rDS(on) (Ohms)	ID Continuous (Amps)	Power Dissipation (Watts)	Part Number
	500	0.4	13.0	150	IRF450
	500	0.5	12.0	150	IRF452
	500	0.85	8.0	125	IRF440
	500	1.10	7.0	125	IRF442
	500	1.5	6.5	175	VNP002A*
	500	1.5	4.0	100	VN5001A
	500	1.5	5.0	75	IRF430
	500	2.0	4.0	100	VN5002A
	500	2.0	4.0	75	IRF432
	500	3.0	2.5	40	IRF420
	500	4.0	2.0	40	IRF422
	450	0.4	13.0	150	IRF451
	450	0.5	12.0	150	IRF453
	450	0.85	8.0	125	IRF441
	450	1.10	7.0	125	IRF443
	450	1.5	6.5	175	VNN002A*
	450	1.5	5.0	100	VN4501A
	450	1.5	5.0	75	IRF431
	450	2.0	4.0	100	VN4502A
	450	2.0	4.0	75	IRF433
	450	3.0	2.5	40	IRF421
	450	4.0	2.0	40	IRF423
	400	0.3	15.0	150	IRF350
	400	0.4	13.0	150	IRF352
	400	0.55	10.0	125	IRF340
	400	0.80	8.0	125	IRF342
	400	1.0	8.0	175	VNM001A*
	400	1.0	6.0	125	VN4000A
	400	1.0	6.0	75	IRF330
	400	1.5	5.0	100	VN4001A
	400	1.5	5.0	75	IRF332
	400	1.8	3.0	40	IRF320
	400	2.5	2.5	40	IRF322
	350	0.3	15.0	150	IRF351
	350	0.4	13.0	150	IRF353
	350	0.55	10.0	125	IRF341
	350	0.80	9.0	125	IRF343
	350	1.0	8.0	175	VNL001A*
	350	1.0	6.0	125	VN3500A
	350	1.0	6.0	75	IRF331
	350	1.5	5.0	125	VN3501A
	350	1.5	5.0	75	IRF333
	350	1.8	3.0	40	IRF321
	350	2.5	2.5	40	IRF323
	200	0.085	30.0	150	IRF250
	200	0.12	25.0	150	IRF252
	200	0.18	18.0	125	IRF240
	200	0.22	16.0	125	IRF242
	200	0.4	9.0	75	IRF230
	200	0.6	8.0	75	IRF232
	200	0.8	5.0	40	IRF220
	200	1.2	4.0	40	IRF222
	150	0.085	30.0	150	IRF251
	150	0.12	25.0	150	IRF253
	150	0.18	18.0	125	IRF241
	150	0.22	16.0	125	IRF243
	150	0.4	9.0	75	IRF231
	150	0.6	8.0	75	IRF233
	150	0.8	5.0	40	IRF221
	150	1.2	4.0	40	IRF223
	120	0.18	12.0	75	VN1200A
	120	0.25	12.0	100	VN1201A

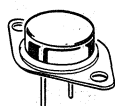
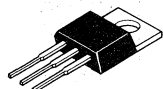


TO-3

*200°C Rating

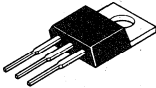
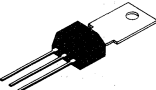

MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

Device	Breakdown Voltage (Volts)	r _{DS(on)} (Ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number	
 TO-3	100	0.055	40.0	150	IRF150	
	100	0.08	33.0	150	IRF152	
	100	0.085	27.0	125	IRF140	
	100	0.11	24.0	125	IRF142	
	100	0.18	12.0	100	VN1000A	
	100	0.18	14.0	75	IRF130	
	100	0.25	12.0	100	VN1001A	
	100	0.25	12.0	75	IRF132	
	100	0.3	6.0	40	IRF120	
	100	0.4	5.0	40	IRF122	
	90	4.0	1.9	25	2N6658	
	90	4.5	1.8	25	VN99AA	
	90	5.0	1.7	25	VN90AA	
	80	0.18	12.0	100	VN0800A	
	80	0.25	12.0	100	VN0801A	
	60	0.055	40.0	150	IRF151	
	60	0.08	33.0	150	IRF153	
	60	0.085	27.0	125	IRF141	
	60	0.11	24.0	125	IRF143	
	60	0.12	16.0	125	VN0600A	
	60	0.15	24.0	125	VN0601A	
	60	0.18	14.0	75	IRF131	
	60	0.25	12.0	75	IRF133	
	60	0.3	6.0	40	IRF121	
	60	0.4	10.0	80	VN64GA	
	60	0.4	5.0	40	IRF123	
	60	3.0	2.0	25	2N6657	
	60	3.5	2.0	25	VN67AA	
	40	0.12	16.0	100	VN0400A	
	40	0.15	16.0	100	VN0401A	
	35	1.8	2.0	25	2N6656	
	35	2.5	2.0	25	VN35AA	
	 TO-220AB	500	0.85	8.0	125	IRF840
		500	1.10	7.0	125	IRF842
		500	1.5	4.0	75	VN5001D
500		1.5	5.0	75	IRF830	
500		2.0	4.0	75	VN5002D	
500		2.0	4.0	75	IRF832	
500		3.0	2.5	40	IRF820	
500		4.0	2.0	40	IRF822	
450		0.85	8.0	125	IRF841	
450		1.10	7.0	125	IRF843	
450		1.5	4.0	75	VN4501D	
450		1.5	5.0	75	IRF831	
450		2.0	4.0	75	VN4502D	
450		2.0	4.0	75	IRF833	
450		3.0	2.5	40	IRF821	
450		4.0	2.0	40	IRF823	
400		0.55	10.0	125	IRF740	
400		0.80	8.0	125	IRF742	
400		1.0	6.0	75	VN4000D	
400		1.0	6.0	75	IRF730	
400		1.5	5.0	75	VN4001D	
400		1.5	5.0	75	IRF732	
400		1.8	3.0	40	IRF720	
400		2.5	2.5	40	IRF722	
350		0.55	10.0	125	IRF741	
350		0.80	8.0	125	IRF743	
350		1.0	6.0	75	VN3500D	
350		1.0	6.0	75	IRF731	
350		1.5	5.0	75	VN3501D	
350		1.5	5.0	75	IRF733	
350		1.8	3.0	40	IRF721	
350		2.5	2.5	40	IRF723	
240		6.0	1.4	20	VN2406D	




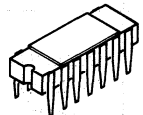
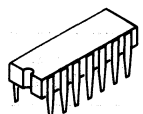
MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

Device	Breakdown Voltage (Volts)	rDS(on) (Ohms)	ID Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-220AB	200	0.18	18.0	125	IRF640
	200	0.22	16.0	125	IRF642
	200	0.4	9.0	75	IRF630
	200	0.6	8.0	75	IRF632
	200	0.8	5.0	40	IRF620
	200	1.2	4.0	40	IRF622
	170	6.0	1.4	20	VN1706D
	150	0.18	18.0	125	IRF641
	150	0.22	16.0	125	IRF643
	150	0.4	9.0	75	IRF631
	150	0.6	8.0	75	IRF633
	150	0.8	5.0	40	IRF621
	150	1.2	4.0	40	IRF623
	120	0.18	12.0	75	VN1200D
	120	0.25	12.0	75	VN1201D
	120	6.0	1.4	20	VN1206D
	100	0.085	27.0	125	IRF540
	100	0.11	24.0	125	IRF542
	100	0.18	12.0	75	VN1000D
	100	0.18	14.0	75	IRF530
	100	0.25	12.0	75	VN1001D
	100	0.25	12.0	75	IRF532
	100	0.30	8.0	40	IRF520
	100	0.40	7.0	40	IRF522
	80	0.18	12.0	75	VN0800D
	80	0.25	12.0	75	VN0801D
	80	4.0	1.7	20	VN88AD
	80	4.5	1.6	20	VN89AD
	60	0.085	27.0	125	IRF541
	60	0.11	24.0	125	IRF543
	60	0.12	16.0	75	VN0600D
	60	0.15	16.0	75	VN0601D
	60	0.18	14.0	75	IRF531
	60	0.25	12.0	75	IRF533
	60	0.30	8.0	40	IRF521
	60	0.40	7.0	40	IRF523
	60	3.0	1.9	20	VN66AD
	60	3.5	1.8	20	VN67AD
	40	0.12	16.0	75	VN0400D
	40	0.15	16.0	75	VN0401D
40	3.0	1.9	20	VN46AD	
40	5.0	1.5	20	VN40AD	
30	1.5	2.5	20	VN0300D	
 TO-202AA	80	4.0	1.5	15	VN88AF
	80	4.5	1.4	15	VN89AF
	80	5.0	1.3	15	VN80AF
	60	3.0	1.7	15	VN66AF
	60	3.5	1.6	15	VN67AF
	40	3.0	1.6	15	VN46AF
	40	5.0	1.3	15	VN40AF
	 TO-39	240	6.0	0.8	6.25
170		6.0	0.8	6.25	VN1706B
120		6.0	0.8	6.25	VN1206B
100		0.3	6.0	20	IRFF120
100		0.4	5.0	20	IRFF122
90		4.0	0.9	6.25	2N6661
90		4.5	0.9	6.25	VN99AB
90		5.0	0.8	6.25	VN90AB
60		0.3	6.0	20	IRFF121
60		0.4	5.0	20	IRFF123
60		3.0	1.1	6.25	2N6660
60		3.5	1.0	6.25	VN67AB
35		1.8	1.4	6.25	2N6659
35		2.5	1.2	6.25	VN35AB



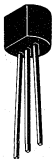
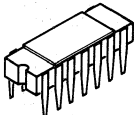
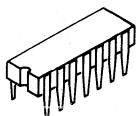
MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

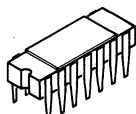
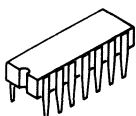
Device	Breakdown Voltage (Volts)	r _{DS(on)} (Ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-52	60	5.0	0.2	0.315	VN10KE
	60	5.0	0.2	0.315	VN10LE
 TO-237	240	6.0	0.3	1.0	VN2406M
	240	10.0	0.25	1.0	VN2410M
	170	6.0	0.3	1.0	VN1706M
	170	10.0	0.25	1.0	VN1710M
	120	6.0	0.3	1.0	VN1206M
	120	10.0	0.25	1.0	VN1210M
	80	4.0	0.35	1.0	VN0808M
	60	3.0	0.4	1.0	VN0606M
	60	5.0	0.3	1.0	VN10KM
	60	5.0	0.3	1.0	VN10LM
	60	7.5	0.25	1.0	VN2222KM
	60	7.5	0.25	1.0	VN2222LM
	30	1.2	0.7	1.0	VN0300M
	 TO-92	240	6.0	0.21	0.4
240		10.0	0.16	0.4	VN2410L
170		6.0	0.21	0.4	VN1706L
170		10.0	0.16	0.4	VN1710L
120		6.0	0.21	0.4	VN1206L
120		10.0	0.16	0.4	VN1210L
60		5.0	0.2	0.4	VN0610L
60		7.5	0.15	0.4	VN2222L
 14-Pin Dual-In-Line (Side Braze)	90	4.5	0.40	1.3	VQ1006P
	60	3.5	0.225	0.5	VQ1000P
	60	5.5	0.46	1.3	VQ1004P
	30	1.0	0.85	1.3	VQ1001P
 14-Pin Dual-In-Line (Plastic)	90	4.5	0.40	1.3	VQ1006J
	60	3.5	0.225	0.5	VQ1000J
	60	5.5	0.46	1.3	VQ1004J
	30	1.0	0.85	1.3	VQ1001J

MOSPOWER Selector Guide (Continued)

P-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	r _{DS(on)} (Ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 TO-39	-100	5.0	0.9	6.25	VP1008B
	-80	5.0	0.9	6.25	VP0808B
	-30	2.5	1.3	6.25	VP0300B
 TO-237	-100	5.0	0.37	1.0	VP1008M
	-80	5.0	0.37	1.0	VP0808M
	-30	2.5	0.48	1.0	VP0300M
 TO-92	-100	5.0	0.37	0.4	VP1008L
	-80	5.0	0.37	0.4	VP0808L
	-30	2.5	0.48	1.0	VP0300L
 14-Pin Dual-In-Line (Side Braze)	-90	5.0	0.600	1.3	VQ2006P
	-60	5.0	0.600	1.3	VQ2004P
	-30	2.0	0.600	1.3	VQ2001P
 14-Pin Dual-In-Line (Plastic)	-90	5.0	0.600	1.3	VQ2006J
	-60	5.0	0.600	1.3	VQ2004J
	-30	2.0	0.600	1.3	VQ2001J

N- and P-Channel Quad MOSPOWER

Device	Breakdown Voltage (Volts)	r _{DS(on)} (Ohms)	I _D Continuous (Amps)	Power Dissipation (Watts)	Part Number
 14-Pin Dual-In-Line (Side Braze)	30	3.0**	N- 0.600 P- 0.850	1.3	VQ3001P
	20	3.0**	N- 0.600 P- 0.850	1.3	VQ7254P
 14-Pin Dual-In-Line (Plastic)	30	3.0**	N- 0.600 P- 0.850	1.3	VQ3001J
	20	3.0**	N- 0.600 P- 0.850	1.3	VQ7254J

**Total (N + P)

MOSPOWER Cross Reference List

MOSPOWER Cross Reference List

7

HEWLETT-PACKARD

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
HPWR-6501	450	0.85	TO-3	IRF441	450	0.85
HPWR-6502	400	0.74	TO-3	IRF340	400	0.55
HPWR-6503	450	1.0	TO-3	VN4501A	450	1.5
HPWR-6504	400	1.0	TO-3	VN4001A	400	1.0

HITACHI

2SK132	100	1.71	TO-3	IRF122	100	0.4
2SK133	120	1.71	TO-3	IRF223	150	1.2
2SK134	140	1.71	TO-3	IRF223	150	1.2
2SK135	160	1.71	TO-3	IRF222	200	1.2
2SK175	180	1.71	TO-3	IRF222	200	1.2
2SK176	200	1.71	TO-3	IRF222	200	1.2
2SK220	160	—	TO-3	—	—	—
2SK221	200	—	TO-3	—	—	—
2SK259	350	3.0	TO-3	IRF323	350	2.5
2SK260	400	3.0	TO-3	IRF322	400	2.5
2SJ47	-100	1.71	TO-3	—	—	—
2SJ48	-120	1.71	TO-3	—	—	—
2SJ49	-140	1.71	TO-3	—	—	—
2SJ50	-160	1.71	TO-3	—	—	—

INTERNATIONAL RECTIFIER

IRF120	100	0.30	TO-3	IRF120	—	—
IRF121	60	0.30	TO-3	IRF121	—	—
IRF122	100	0.40	TO-3	IRF122	—	—
IRF123	60	0.40	TO-3	IRF123	—	—
IRF130	100	0.18	TO-3	IRF130	—	—
IRF131	60	0.18	TO-3	IRF131	—	—
IRF132	100	0.25	TO-3	IRF132	—	—
IRF133	60	0.25	TO-3	IRF133	—	—
IRF140	100	0.085	TO-3	IRF140	—	—
IRF141	60	0.085	TO-3	IRF141	—	—
IRF142	100	0.11	TO-3	IRF142	—	—
IRF143	60	0.11	TO-3	IRF143	—	—
IRF150	100	0.055	TO-3	IRF150	—	—
IRF151	60	0.055	TO-3	IRF151	—	—
IRF152	100	0.08	TO-3	IRF152	—	—
IRF153	60	0.08	TO-3	IRF153	—	—
IRF220	200	0.8	TO-3	IRF220	—	—
IRF221	150	0.8	TO-3	IRF221	—	—
IRF222	200	1.2	TO-3	IRF222	—	—
IRF223	150	1.2	TO-3	IRF223	—	—
IRF230	200	0.4	TO-3	IRF230	—	—
IRF231	150	0.4	TO-3	IRF231	—	—
IRF232	200	0.6	TO-3	IRF232	—	—
IRF233	150	0.6	TO-3	IRF233	—	—
IRF240	200	0.18	TO-3	IRF240	—	—
IRF241	150	0.18	TO-3	IRF241	—	—
IRF242	200	0.22	TO-3	IRF242	—	—
IRF243	150	0.22	TO-3	IRF243	—	—
IRF250	200	0.085	TO-3	IRF250	—	—
IRF251	150	0.085	TO-3	IRF251	—	—
IRF252	200	0.120	TO-3	IRF252	—	—
IRF253	150	0.120	TO-3	IRF253	—	—
IRF320	400	1.8	TO-3	IRF320	—	—
IRF321	350	1.8	TO-3	IRF321	—	—
IRF322	400	2.5	TO-3	IRF322	—	—
IRF323	350	2.5	TO-3	IRF323	—	—
IRF330	400	1.0	TO-3	IRF330	—	—
IRF331	350	1.0	TO-3	IRF331	—	—
IRF332	400	1.5	TO-3	IRF332	—	—
IRF333	350	1.5	TO-3	IRF333	—	—
IRF340	400	0.55	TO-3	IRF340	—	—
IRF341	350	0.55	TO-3	IRF341	—	—
IRF342	400	0.80	TO-3	IRF342	—	—
IRF343	350	0.80	TO-3	IRF343	—	—
IRF350	400	0.3	TO-3	IRF350	—	—
IRF351	350	0.3	TO-3	IRF351	—	—
IRF352	400	0.4	TO-3	IRF352	—	—
IRF353	350	0.4	TO-3	IRF353	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
IRF420	500	3.0	TO-3	IRF420	—	—
IRF421	450	3.0	TO-3	IRF421	—	—
IRF422	500	4.0	TO-3	IRF422	—	—
IRF423	450	4.0	TO-3	IRF423	—	—
IRF430	500	1.5	TO-3	IRF430	—	—
IRF431	450	1.5	TO-3	IRF431	—	—
IRF432	500	2.0	TO-3	IRF432	—	—
IRF433	450	2.0	TO-3	IRF433	—	—
IRF440	500	0.85	TO-3	IRF440	—	—
IRF441	450	0.85	TO-3	IRF441	—	—
IRF442	500	1.10	TO-3	IRF442	—	—
IRF443	450	1.10	TO-3	IRF443	—	—
IRF450	500	0.4	TO-3	IRF450	—	—
IRF451	450	0.4	TO-3	IRF451	—	—
IRF452	500	0.5	TO-3	IRF452	—	—
IRF453	450	0.5	TO-3	IRF453	—	—
IRF510	100	0.6	TO-220	—	—	—
IRF511	60	0.6	TO-220	—	—	—
IRF512	100	0.8	TO-220	—	—	—
IRF513	60	0.8	TO-220	—	—	—
IRF520	100	0.3	TO-220	IRF520	—	—
IRF521	60	0.3	TO-220	IRF521	—	—
IRF522	100	0.4	TO-220	IRF522	—	—
IRF523	60	0.4	TO-220	IRF523	—	—
IRF530	100	0.18	TO-220	IRF530	—	—
IRF531	100	0.25	TO-220	IRF531	—	—
IRF532	60	0.18	TO-220	IRF532	—	—
IRF533	60	0.25	TO-220	IRF533	—	—
IRF540	100	0.085	TO-220	IRF540	—	—
IRF541	60	0.085	TO-220	IRF541	—	—
IRF542	100	0.11	TO-220	IRF542	—	—
IRF543	60	0.11	TO-220	IRF543	—	—
IRF610	100	1.6	TO-220	—	—	—
IRF611	60	1.6	TO-220	—	—	—
IRF612	100	2.4	TO-220	—	—	—
IRF613	60	2.4	TO-220	—	—	—
IRF620	200	0.8	TO-220	IRF620	—	—
IRF621	150	0.8	TO-220	IRF621	—	—
IRF622	200	1.2	TO-220	IRF622	—	—
IRF623	150	1.2	TO-220	IRF623	—	—
IRF630	200	0.4	TO-220	IRF630	—	—
IRF631	150	0.4	TO-220	IRF631	—	—
IRF632	200	0.6	TO-220	IRF632	—	—
IRF633	150	0.6	TO-220	IRF633	—	—
IRF640	200	0.18	TO-220	IRF640	—	—
IRF641	150	0.18	TO-220	IRF641	—	—
IRF642	200	0.22	TO-220	IRF642	—	—
IRF643	150	0.22	TO-220	IRF643	—	—
IRF710	100	3.6	TO-220	—	—	—
IRF711	60	3.6	TO-220	—	—	—
IRF712	100	5.0	TO-220	—	—	—
IRF713	60	5.0	TO-220	—	—	—
IRF720	400	1.8	TO-220	IRF720	—	—
IRF721	350	1.8	TO-220	IRF721	—	—
IRF722	400	2.5	TO-220	IRF722	—	—
IRF723	350	2.5	TO-220	IRF723	—	—
IRF730	400	1.0	TO-220	IRF730	—	—
IRF731	350	1.0	TO-220	IRF731	—	—
IRF732	400	1.5	TO-220	IRF732	—	—
IRF733	350	1.5	TO-220	IRF733	—	—
IRF820	500	3.0	TO-220	IRF820	—	—
IRF821	450	3.0	TO-220	IRF821	—	—
IRF822	500	4.0	TO-220	IRF822	—	—
IRF823	450	4.0	TO-220	IRF823	—	—
IRF830	500	1.5	TO-220	IRF830	—	—
IRF831	450	1.5	TO-220	IRF831	—	—
IRF832	500	2.0	TO-220	IRF832	—	—
IRF833	450	2.0	TO-220	IRF833	—	—
IRF840	500	0.85	TO-220	IRF840	—	—
IRF841	450	0.85	TO-220	IRF841	—	—
IRF842	500	1.1	TO-220	IRF842	—	—
IRF843	450	1.1	TO-220	IRF843	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
IRF9130	100	0.3	TO-3	IRF9130	—	—
IRF9131	60	0.3	TO-3	IRF9131	—	—
IRF9132	100	0.4	TO-3	IRF9132	—	—
IRF9133	60	0.4	TO-3	IRF9133	—	—
IRF9230	200	0.8	TO-3	—	—	—
IRF9231	150	0.8	TO-3	—	—	—
IRF9232	200	1.2	TO-3	—	—	—
IRF9233	150	1.2	TO-3	—	—	—
IRF9520	100	0.6	TO-220	IRF9520	—	—
IRF9521	60	0.6	TO-220	IRF9521	—	—
IRF9522	100	0.8	TO-220	IRF9522	—	—
IRF9523	60	0.8	TO-220	IRF9523	—	—
IRF9530	100	0.3	TO-220	IRF9530	—	—
IRF9531	60	0.3	TO-220	IRF9531	—	—
IRF9532	100	0.4	TO-220	IRF9532	—	—
IRF9533	60	0.4	TO-220	IRF9533	—	—
IRF9610	200	3.0	TO-220	—	—	—
IRF9611	150	3.0	TO-220	—	—	—
IRF9612	200	4.5	TO-220	—	—	—
IRF9613	150	4.5	TO-220	—	—	—
IRF9620	200	1.5	TO-220	—	—	—
IRF9621	150	1.5	TO-220	—	—	—
IRF9622	200	2.4	TO-220	—	—	—
IRF9623	150	2.4	TO-220	—	—	—
IRF9630	200	0.8	TO-220	—	—	—
IRF9631	150	0.8	TO-220	—	—	—
IRF9632	200	1.2	TO-220	—	—	—
IRF9633	150	1.2	TO-220	—	—	—
IRFF110	100	0.6	TO-39	—	—	—
IRFF111	60	0.6	TO-39	—	—	—
IRFF112	100	0.8	TO-39	—	—	—
IRFF113	60	0.8	TO-39	—	—	—
IRFF120	100	0.30	TO-39	IRFF120	—	—
IRFF121	60	0.30	TO-39	IRFF121	—	—
IRFF122	100	0.40	TO-39	IRFF122	—	—
IRFF123	60	0.40	TO-39	IRFF123	—	—
IRFF130	100	0.18	TO-39	—	—	—
IRFF131	60	0.18	TO-39	—	—	—
IRFF132	100	0.25	TO-39	—	—	—
IRFF133	60	0.25	TO-39	—	—	—
2N6755	60	0.25	TO-3	IRF131	—	—
2N6756	100	0.18	TO-3	IRF130	—	—
2N6757	150	0.6	TO-3	—	—	—
2N6758	200	0.4	TO-3	—	—	—
2N6759	350	1.5	TO-3	IRF333	—	—
2N6760	400	1.0	TO-3	IRF330	—	—
2N6761	450	2.0	TO-3	IRF433	—	—
2N6762	500	1.5	TO-3	IRF430	—	—
2N6763	60	0.08	TO-3	—	—	—
2N6764	100	0.055	TO-3	—	—	—
2N6765	150	0.120	TO-3	—	—	—
2N6766	200	0.085	TO-3	—	—	—
2N6767	350	0.4	TO-3	—	—	—
2N6768	400	0.3	TO-3	—	—	—
2N6769	450	0.5	TO-3	—	—	—
2N6770	500	0.4	TO-3	—	—	—
2N6781	60	0.6	TO-39	—	—	—
2N6782	100	0.6	TO-39	—	—	—
2N6783	150	1.5	TO-39	—	—	—
2N6784	200	1.5	TO-39	—	—	—
2N6785	350	3.6	TO-39	—	—	—
2N6786	400	3.6	TO-39	—	—	—
2N6787	60	0.3	TO-39	—	—	—
2N6788	100	0.3	TO-39	—	—	—
2N6789	150	0.8	TO-39	—	—	—
2N6790	200	0.8	TO-39	—	—	—
2N6791	350	1.8	TO-39	—	—	—
2N6792	400	1.8	TO-39	—	—	—
2N6793	450	3.0	TO-39	—	—	—
2N6794	500	3.0	TO-39	—	—	—
2N6795	60	0.18	TO-39	—	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BVDSS (Volts)	rDS(on) (Ohms)	Package	Siliconix Equivalent	BVDSS (Volts)	rDS(on) (Ohms)
2N6796	100	0.18	TO-39	—	—	—
2N6797	150	0.4	TO-39	—	—	—
2N6798	200	0.4	TO-39	—	—	—
2N6799	350	1.0	TO-39	—	—	—
2N6800	400	1.0	TO-39	—	—	—
2N6801	450	1.5	TO-39	—	—	—
2N6802	500	1.5	TO-39	—	—	—

INTERSIL

IVN5000AND	40	2.5	TO-237	—	—	—
IVN5000ANE	60	2.5	TO-237	—	—	—
IVN5000ANF	80	2.5	TO-237	—	—	—
IVN5000ANH	100	2.5	TO-237	—	—	—
IVN5000SND	40	2.5	TO-52	—	—	—
IVN5000SNE	60	2.5	TO-52	—	—	—
IVN5000SNF	80	2.5	TO-52	—	—	—
IVN5000SNH	100	2.5	TO-52	—	—	—
IVN5000TND	40	2.5	TO-39	—	—	—
IVN5000TNE	60	2.5	TO-39	—	—	—
IVN5000TNF	80	2.5	TO-39	—	—	—
IVN5000TNH	100	2.5	TO-39	—	—	—
IVN5001AND	40	2.5	TO-237	—	—	—
IVN5001ANE	60	2.5	TO-237	—	—	—
IVN5001ANF	80	2.5	TO-237	—	—	—
IVN5001ANH	100	2.5	TO-237	—	—	—
IVN5001SND	40	2.5	TO-52	—	—	—
IVN5001SNE	60	2.5	TO-52	—	—	—
IVN5001SNF	80	2.5	TO-52	—	—	—
IVN5001SNH	100	2.5	TO-52	—	—	—
IVN5001TND	40	2.5	TO-39	—	—	—
IVN5001TNE	60	2.5	TO-39	—	—	—
IVN5001TNF	80	2.5	TO-39	—	—	—
IVN5001TNH	100	2.5	TO-39	—	—	—
IVN5200HND	40	0.5	TO-66	—	—	—
IVN5200HNE	60	0.5	TO-66	—	—	—
IVN5200HNF	80	0.5	TO-66	—	—	—
IVN5200HNH	100	0.5	TO-66	—	—	—
IVN5200KND	40	0.5	TO-3	IRF123	60	0.4
IVN5200KNE	60	0.5	TO-3	IRF123	60	0.4
IVN5200KNF	80	0.5	TO-3	IRF122	100	0.4
IVN5200KNH	100	0.5	TO-3	IRF122	100	0.4
IVN5200TND	40	0.5	TO-39	IRFF123	60	0.4
IVN5200TNE	60	0.5	TO-39	IRFF123	60	0.4
IVN5200TNF	80	0.5	TO-39	IRFF122	100	0.4
IVN5200TNH	100	0.5	TO-39	IRFF122	100	0.4
IVN5201CND	40	0.5	TO-220	IRF523	60	0.4
IVN5201CNE	60	0.5	TO-220	IRF523	60	0.4
IVN5201CNF	80	0.5	TO-220	IRF522	100	0.4
IVN5201CNH	100	0.5	TO-220	IRF522	100	0.4
IVN5201HND	40	0.5	TO-66	—	—	—
IVN5201HNE	60	0.5	TO-66	—	—	—
IVN5201HNF	80	0.5	TO-66	—	—	—
IVN5201HNH	100	0.5	TO-66	—	—	—
IVN5201KND	40	0.5	TO-3	IRF123	60	0.4
IVN5201KNE	60	0.5	TO-3	IRF123	60	0.4
IVN5201KNF	80	0.5	TO-3	IRF122	100	0.4
IVN5201KNH	100	0.5	TO-3	IRF122	100	0.4
IVN5201TND	40	0.5	TO-39	IRF123	60	0.4
IVN5201TNE	60	0.5	TO-39	IRF123	60	0.4
IVN5201TNF	80	0.5	TO-39	IRF122	100	0.4
IVN5201TNH	100	0.5	TO-39	IRF122	100	0.4
IVN6000CNS	400	3.5	TO-220	IRF722	400	2.5
IVN6000CNT	450	3.5	TO-220	IRF821	450	3.0
IVN6000CNU	500	4.0	TO-220	IRF822	500	4.0
IVN6000KNR	350	3.0	TO-3	IRF323	350	2.5
IVN6000KNS	400	3.0	TO-3	IRF322	400	2.5
IVN6000KNT	450	3.0	TO-3	IRF421	450	3.0
IVN6000KNU	500	4.0	TO-3	IRF422	500	4.0
IVN6100TNS	400	15.0	TO-39	—	—	—
IVN6100TNT	450	15.0	TO-39	—	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERSIL (Cont'd)

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
IVN6100TNU	500	15.0	TO-39	—	—	—
IVN6200CND	40	0.35	TO-220	VN0401D	40	0.15
IVN6200CNE	60	0.25	TO-220	IRF533	60	0.25
IVN6200CNF	80	0.25	TO-220	VN0801D	80	0.25
IVN6200CNH	100	0.25	TO-220	VN1001D	100	0.25
IVN6200CNI	200	0.5	TO-220	IRF630	200	0.4
IVN6200CNP	250	0.5	TO-220	—	—	—
IVN6200CNR	395	2.5	TO-220	VN4001D	400	1.5
IVN6200CNS	400	1.5	TO-220	VN4001D	400	1.5
IVN6200CNT	450	1.5	TO-220	VN4501D	450	1.5
IVN6200CNU	500	2.0	TO-220	VN5001D	500	1.5
IVN6200KND	40	0.25	TO-3	VN0401A	40	0.15
IVN6200KNE	60	0.25	TO-3	IRF133	60	0.25
IVN6200KNF	80	0.25	TO-3	VN0801A	80	0.25
IVN6200KNH	100	0.25	TO-3	VN1001A	100	0.25
IVN6200KNI	200	0.5	TO-3	IRF230	200	0.4
IVN6200KNP	250	0.5	TO-3	—	—	—
IVN6200KNS	400	1.5	TO-3	VN4001A	400	1.5
IVN6200KNT	450	1.5	TO-3	VN4501A	450	1.5
IVN6200KNU	500	2.0	TO-3	VN5000A	500	1.5
IVN6300ANE	60	7.5	TO-237	VN2222LM	60	7.5
IVN6300ANF	80	7.5	TO-237	—	—	—
IVN6300ANH	100	7.5	TO-237	—	—	—
IVN6300ANM	200	25.0	TO-237	VN2410M	240	10.0
IVN6300ANP	250	25.0	TO-237	VN2410M	240	10.0
IVN6300ANS	400	75.0	TO-237	—	—	—
IVN6300ANT	450	75.0	TO-237	—	—	—
IVN6300ANU	500	75.0	TO-237	—	—	—
IVN6300SNE	60	7.5	TO-52	VN10LE	60	5.0
IVN6300SNF	80	7.5	TO-52	—	—	—
IVN6300SNH	100	7.5	TO-52	—	—	—
IVN6300SNM	200	25.0	TO-52	—	—	—
IVN6300SNP	250	25.0	TO-52	—	—	—
IVN6300SNS	400	75.0	TO-52	—	—	—
IVN6300SNT	450	75.0	TO-52	—	—	—
IVN6300SNU	500	75.0	TO-52	—	—	—

MOTOROLA

MTM1N95	950	10.0	TO-3	—	—	—
MTM1N100	1000	10.0	TO-3	—	—	—
MTM2N45	450	4.0	TO-3	IRF423	450	4.0
MTM2N50	500	4.0	TO-3	IRF422	500	4.0
MTM2N85	850	8.0	TO-3	—	—	—
MTM2N90	900	8.0	TO-3	—	—	—
MTM3N35	350	3.3	TO-3	IRF323	350	2.5
MTM3N40	400	3.3	TO-3	IRF322	400	2.5
MTM3N55	550	2.5	TO-3	—	—	—
MTM3N60	600	2.5	TO-3	—	—	—
MTM4N45	450	2.0	TO-3	VN4502A	450	2.0
MTM4N50	500	2.0	TO-3	VN5002A	500	2.0
MTM5N35	350	1.5	TO-3	VN3501A	350	1.5
MTM5N40	400	1.5	TO-3	VN4001A	400	1.5
MTM6N55	550	1.5	TO-3	—	—	—
MTM6N60	600	1.5	TO-3	—	—	—
MTM7N45	450	1.2	TO-3	IRF443	450	1.1
MTM7N50	500	1.2	TO-3	IRF442	500	1.1
MTM8N12	120	0.5	TO-3	—	—	—
MTM8N15	150	0.5	TO-3	—	—	—
MTM8N18	180	0.4	TO-3	—	—	—
MTM8N20	200	0.4	TO-3	—	—	—
MTM8N35	350	0.8	TO-3	IRF343	350	0.8
MTM8N40	400	0.8	TO-3	IRF342	400	0.8
MTM10N08	80	0.33	TO-3	IRF120	100	0.3
MTM10N10	100	0.33	TO-3	IRF120	100	0.3
MTM10N12	120	0.3	TO-3	—	—	—
MTM10N15	150	0.3	TO-3	—	—	—
MTM12N05	50	0.2	TO-3	VN0601A	60	0.15
MTM12N06	60	0.2	TO-3	VN0601A	60	0.15
MTM12N08	80	0.25	TO-3	VN0801A	80	0.25
MTM12N10	100	0.25	TO-3	VN1001A	100	0.25

MOSPOWER Cross Reference List

MOSPOWER Cross Reference List (Cont'd)

MOTOROLA (Cont'd)

Industry Part No.	BVDSS (Volts)	rDS(on) (Ohms)	Package	Siliconix Equivalent	BVDSS (Volts)	rDS(on) (Ohms)
MTM15N05	50	0.16	TO-3	VN0601A	60	0.15
MTM15N06	60	0.16	TO-3	VN0601A	60	0.15
MTM15N35	350	0.4	TO-3	IRF353	350	0.4
MTM15N40	400	0.4	TO-3	IRF352	400	0.4
MTM15N45	450	0.5	TO-3	IRF453	450	0.5
MTM15N50	500	0.5	TO-3	IRF452	500	0.5
MTM2P45	450	6.0	TO-3	—	—	—
MTM2P50	500	6.0	TO-3	—	—	—
MTM814	80	0.4	TO-3	—	—	—
MTM815	100	0.4	TO-3	—	—	—
MTP1N95	950	10.0	TO-220	—	—	—
MTP1N100	1000	10.0	TO-220	—	—	—
MTP2N45	450	4.0	TO-220	IRF823	450	4.0
MTP2N50	500	4.0	TO-220	IRF822	500	4.0
MTP2N85	850	8.0	TO-220	—	—	—
MTP2N90	900	8.0	TO-220	—	—	—
MTP3N35	350	3.3	TO-220	IRF723	350	2.5
MTP3N40	400	3.3	TO-220	IRF722	400	2.5
MTP3N55	550	2.5	TO-220	—	—	—
MTP3N60	600	2.5	TO-220	—	—	—
MTP4N45	450	2.0	TO-220	VN4502D	450	2.0
MTP4N50	500	2.0	TO-220	VN5002D	500	2.0
MTP5N35	350	1.5	TO-220	VN3501D	350	1.5
MTP5N40	400	1.5	TO-220	VN4001D	400	1.5
MTP6N55	550	1.5	TO-220	—	—	—
MTP6N60	600	1.5	TO-220	—	—	—
MTP7N45	450	1.2	TO-220	IRF843	450	1.1
MTP7N50	500	1.2	TO-220	IRF842	500	1.1
MTP8N12	120	0.5	TO-220	—	—	—
MTP8N15	150	0.5	TO-220	—	—	—
MTP8N18	180	0.4	TO-220	—	—	—
MTP8N20	200	0.4	TO-220	—	—	—
MTP8N35	350	0.8	TO-220	IRF743	350	0.8
MTP8N40	400	0.8	TO-220	IRF742	400	0.8
MTP10N08	80	0.33	TO-220	IRF520	100	0.3
MTP10N10	100	0.33	TO-220	IRF520	100	0.3
MTP10N12	120	0.3	TO-220	—	—	—
MTP10N15	150	0.3	TO-220	—	—	—
MTP12N05	50	0.2	TO-220	VN0601D	60	0.15
MTP12N06	60	0.2	TO-220	VN0601D	60	0.15
MTP12N08	80	0.25	TO-220	VN0801D	80	0.25
MTP12N10	100	0.25	TO-220	VN1001D	100	0.25
MTP15N05	50	0.16	TO-220	VN0601D	60	0.15
MTP15N06	60	0.16	TO-220	VN0601D	60	0.15
MTP15N35	350	0.4	TO-220	IRF753	350	0.4
MTP15N40	400	0.4	TO-220	IRF752	400	0.4
MTP15N45	450	0.5	TO-220	IRF853	450	0.5
MTP15N50	500	0.5	TO-220	IRF852	500	0.5
MTP2P45	450	6.0	TO-220	—	—	—
MTP2P50	500	6.0	TO-220	—	—	—
MTP814	80	0.4	TO-220	—	—	—
MTP815	100	0.4	TO-220	—	—	—

RCA

RCA-9213A	100	2.5	TO-220	—	—	—
RCA-9213B	150	2.5	TO-220	—	—	—
RCA-9196A	100	2.5	TO-39	—	—	—
RCA-9196B	150	2.5	TO-39	—	—	—
RCA-9212A	100	0.3	TO-220	IRF520	100	0.3
RCA-9212B	150	0.3	TO-220	—	—	—
RCA-9192A	100	0.3	TO-3	IRF120	100	0.3
RCA-9192B	150	0.3	TO-3	—	—	—
RCA-9230A	100	0.15	TO-220	IRF542	100	0.11
RCA-9230B	150	0.15	TO-220	—	—	—
RCA-9195A	100	0.15	TO-3	IRF142	100	0.11
RCA-9195B	150	0.15	TO-3	—	—	—

SIEMENS

BUZ 10	50	0.10	TO-220	IRF541	60	0.085
BUZ 11	50	0.04	TO-220	—	—	—

MOSPOWER Cross Reference List (Cont'd)

SIEMENS (Cont'd)

Industry Part No.	BVDSS (Volts)	rDS(on) (Ohms)	Package	Siliconix Equivalent	BVDSS (Volts)	rDS(on) (Ohms)
BUZ 14	50	0.04	TO-3	—	—	—
BUZ 15	50	0.03	TO-3	—	—	—
BUZ 20	100	0.20	TO-220	VN1000D	100	0.18
BUZ 21	100	0.10	TO-220	IRF522	100	0.4
BUZ 23	100	0.20	TO-3	VN1000A	100	0.18
BUZ 24	100	0.06	TO-3	—	—	—
BUZ 25	100	0.10	TO-3	IRF540	100	0.085
BUZ 30	200	0.75	TO-220	IRF632	200	0.6
BUZ 31	200	0.20	TO-220	IRF640	200	0.18
BUZ 33	200	0.75	TO-3	IRF232	200	0.6
BUZ 34	200	0.20	TO-3	IRF240	200	0.18
BUZ 40	500	4.5	TO-220	IRF822	500	4.0
BUZ 41	500	1.1	TO-220	IRF842	500	1.1
BUZ 43	500	4.5	TO-3	IRF422	500	4.0
BUZ 44	500	1.1	TO-3	IRF442	500	1.1
BUZ 45	500	0.6	TO-3	IRF452	500	0.5
BUZ 50	1000	3.5	TO-220	—	—	—
BUZ 53	1000	3.5	TO-3	—	—	—
BUZ 54	1000	2.0	TO-3	—	—	—
BUZ 80	800	2.6	TO-220	—	—	—
BUZ 83	800	2.6	TO-3	—	—	—
BUZ 84	800	1.3	TO-3	—	—	—

SONY

2SJ54	- 210	1.0	TO-220	—	—	—
2SK173	210	1.0	TO-220	IRF232	200V	0.6

SUPERTEX

VN0104N1	40	4.0	TO-3	VN67AA	60	3.5
VN0104N2	40	4.0	TO-39	VN67AB	60	3.5
VN0104N3	40	4.0	TO-92	—	—	—
VN0104N4	40	4.0	TO-202	VN46AF	40	3.0
VN0104N5	40	4.0	TO-220	VN46AD	40	3.0
VN0104N6	40	4.0	DIP	VQ1004J	60	3.5
VN0106N1	60	4.0	TO-3	VN67AA	60	3.5
VN0106N2	60	4.0	TO-39	VN67AB	60	3.5
VN0106N3	60	4.0	TO-92	—	—	—
VN0106N4	60	4.0	TO-202	VN67AF	60	3.5
VN0106N5	60	4.0	TO-220	VN67AD	60	3.5
VN0106N6	60	4.0	DIP	VQ1004J	60	3.5
VN0108N1	80	4.0	TO-3	2N6658	90	4.0
VN0108N2	80	4.0	TO-39	2N6661	90	4.0
VN0108N3	80	4.0	TO-92	—	—	—
VN0108N4	80	4.0	TO-202	VN88AF	80	4.0
VN0108N5	80	4.0	TO-220	VN88AD	80	4.0
VN0108N6	80	4.0	DIP	VQ1006J	90	4.5
VN0109N1	90	4.0	TO-3	2N6658	90	4.0
VN0109N2	90	4.0	TO-39	2N6661	90	4.0
VN0109N3	90	4.0	TO-92	—	—	—
VN0109N4	90	4.0	TO-202	—	—	—
VN0109N5	90	4.0	TO-220	—	—	—
VN0109N6	90	4.0	DIP	VQ1006J	90	4.5
VN0204N1	40	2.0	TO-3	—	—	—
VN0204N2	40	2.0	TO-39	—	—	—
VN0204N5	40	2.0	TO-220	—	—	—
VN0204N6	40	2.0	DIP	—	—	—
VN0206N1	60	2.0	TO-3	—	—	—
VN0206N2	60	2.0	TO-39	—	—	—
VN0206N5	60	2.0	TO-220	—	—	—
VN0206N6	60	2.0	DIP	—	—	—
VN0208N1	80	2.0	TO-3	—	—	—
VN0208N2	80	2.0	TO-39	—	—	—
VN0208N5	80	2.0	TO-220	—	—	—
VN0208N6	80	2.0	DIP	—	—	—
VN0209N1	90	2.0	TO-3	—	—	—
VN0209N2	90	2.0	TO-39	—	—	—
VN0209N5	90	2.0	TO-220	—	—	—
VN0209N6	90	2.0	DIP	—	—	—
VN0330N1	300	3.0	TO-3	IRF323	350	2.5
VN0330N2	300	3.0	TO-39	—	—	—

MOSPOWER Cross Reference List (Cont'd)

SUPERTEX (Cont'd)

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
VN0330N5	300	3.0	TO-220	IRF723	350	2.5
VN0335A1	350	1.0	TO-3	VN3500A	350	1.0
VN0335N1	350	3.0	TO-3	IRF323	350	2.5
VN0335N2	350	3.0	TO-39	—	—	—
VN0335N5	350	3.0	TO-220	IRF723	350	2.5
VN0340A1	400	1.0	TO-3	IRF4000A	400	1.0
VN0340N1	400	3.0	TO-3	IRF322	400	2.5
VN0340N2	400	3.0	TO-39	—	—	—
VN0340N5	400	3.0	TO-220	IRF722	400	2.5
VN0345A1	450	1.0	TO-3	IRF441	450	0.85
VN0345N1	450	3.0	TO-3	IRF421	450	3.0
VN0345N2	450	3.0	TO-39	—	—	—
VN0345N5	450	3.0	TO-220	IRF821	450	3.0
VN0350A1	500	1.0	TO-3	IRF440	500	1.0
VN0430N1	300	0.8	TO-3	IRF343	350	0.8
VN0435N1	350	0.8	TO-3	IRF343	350	0.8
VN0440N1	400	0.8	TO-3	IRF342	400	0.8
VN0445N1	450	0.8	TO-3	IRF441	450	0.85
VN1204N1	40	0.4	TO-3	IRF123	60	0.4
VN1204N2	40	0.4	TO-39	IRFF123	60	0.4
VN1204N5	40	0.4	TO-220	IRF523	60	0.4
VN1206N1	60	0.4	TO-3	IRF123	60	0.4
VN1206N2	60	0.4	TO-39	IRFF123	60	0.4
VN1206N5	60	0.4	TO-220	IRF523	60	0.4
VN1208N1	80	0.4	TO-3	IRF122	100	0.4
VN1208N2	80	0.4	TO-30	IRFF122	100	0.4
VN1208N5	80	0.4	TO-220	IRF522	100	0.4
VN1209N1	90	0.4	TO-3	IRF122	100	0.4
VN1209N2	90	0.4	TO-39	IRFF122	100	0.4
VN1209N5	90	0.4	TO-220	IRF522	90	0.4
VN1304N2	40	10.0	TO-39	VN90AB	60	5.0
VN1304N3	40	10.0	TO-92	VN2222L	60	7.5
VN1304N6	40	10.0	DIP	VQ1000J	90	5.5
VN1306N2	60	10.0	TO-39	VN90AB	60	5.0
VN1306N3	60	10.0	TO-92	VN2222L	60	7.5
VN1306N6	60	10.0	DIP	VQ1000J	90	5.5
VN1308N2	80	10.0	TO-39	VN90AB	90	5.0
VN1308N3	80	10.0	TO-92	—	—	—
VN1308N6	80	10.0	DIP	VQ1006J	90	4.5
VN1309N2	90	10.0	TO-39	VN90AB	90	5.0
VN1309N3	90	10.0	TO-92	—	—	—
VN1309N6	90	10.0	DIP	VQ1006J	90	4.5
VP0104N1	-40	8.0	TO-3	—	—	—
VP0104N2	-40	8.0	TO-39	VP0808B	-60	5.0
VP0104N3	-40	8.0	TO-92	VP0808L	-60	5.0
VP0104N5	-40	8.0	TO-220	—	—	—
VP0104N6	-40	8.0	DIP	—	—	—
VP0106N1	-60	8.0	TO-3	—	—	—
VP0106N2	-60	8.0	TO-39	VP0808B	-60	5.0
VP0106N3	-60	8.0	TO-92	VP0808L	-60	5.0
VP0106N5	-60	8.0	TO-220	—	—	—
VP0106N6	-60	8.0	DIP	—	—	—
VP0108N1	-80	8.0	TO-3	—	—	—
VP0108N2	-80	8.0	TO-39	VP0808B	-80	5.0
VP0108N3	-80	8.0	TO-92	VP0808L	-80	5.0
VP0108N5	-80	8.0	TO-220	—	—	—
VP0108N6	-80	8.0	DIP	—	—	—
VP0109N1	-90	8.0	TO-3	—	—	—
VP0109N2	-90	8.0	TO-39	VP1008B	-100	5.0
VP0109N3	-90	8.0	TO-92	VP1008L	-100	5.0
VP0109N5	-90	8.0	TO-220	—	—	—
VP0109N6	-90	8.0	DIP	—	—	—
VP0204N1	-40	4.0	TO-3	—	—	—
VP0204N2	-40	4.0	TO-39	—	—	—
VP0204N5	-40	4.0	TO-220	—	—	—
VP0204N6	-40	4.0	DIP	—	—	—
VP0206N1	-60	4.0	TO-3	—	—	—
VP0206N2	-60	4.0	TO-39	—	—	—
VP0206N5	-60	4.0	TO-220	—	—	—
VP0206N6	-60	4.0	DIP	—	—	—
VP0208N1	-80	4.0	TO-3	—	—	—

MOSPOWER Cross Reference List (Cont'd)

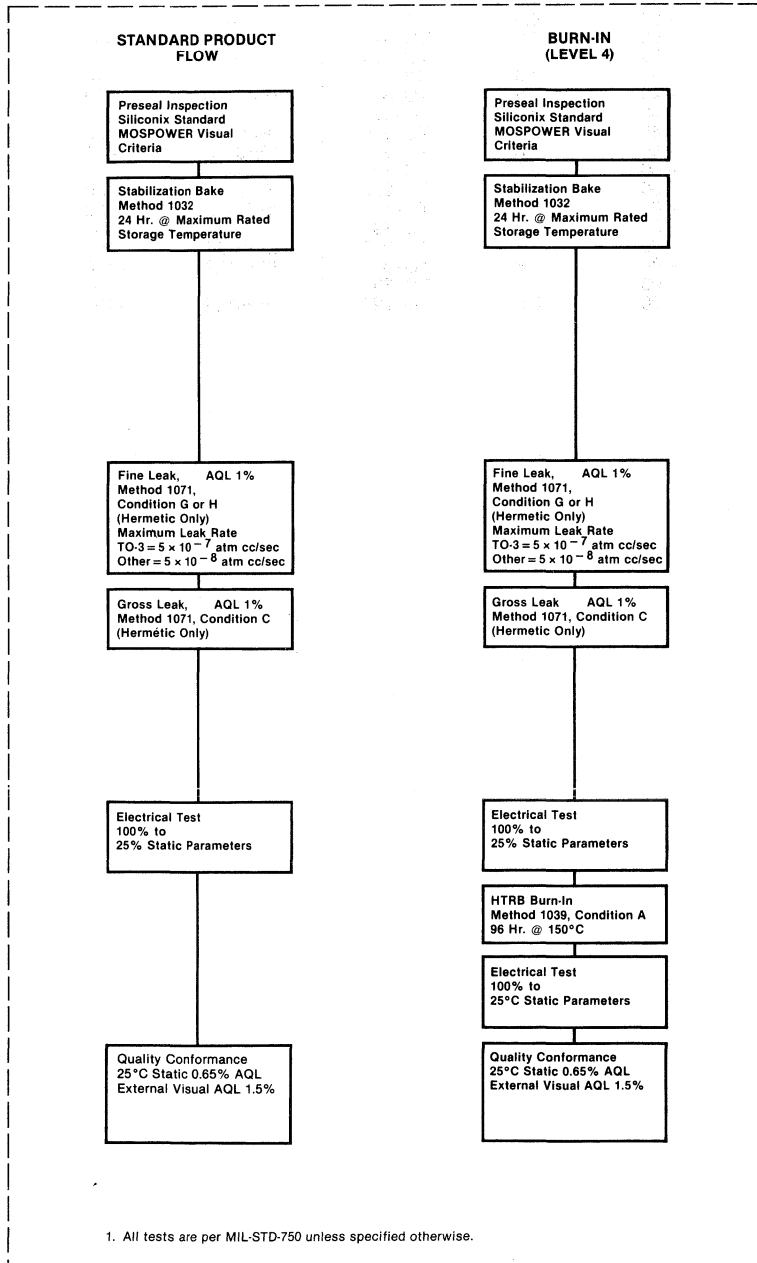
MOSPOWER Cross Reference List

SUPERTEX (Cont'd)

Industry Part No.	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)	Package	Siliconix Equivalent	BV _{DSS} (Volts)	r _{DS(on)} (Ohms)
VP0208N2	-80	4.0	TO-39	—	—	—
VP0208N5	-80	4.0	TO-220	—	—	—
VP0208N6	-80	4.0	DIP	—	—	—
VP0209N1	-90	4.0	TO-3	—	—	—
VP0209N2	-90	4.0	TO-39	—	—	—
VP0209N5	-90	4.0	TO-220	—	—	—
VP0209N6	-90	4.0	DIP	—	—	—
VP1204N1	-40	0.8	TO-3	IRF9133	-60	0.4
VP1204N2	-40	0.8	TO-39	—	—	—
VP1204N5	-40	0.8	TO-220	IRF9523	-60	0.8
VP1206N1	-60	0.8	TO-3	IRF9133	-60	0.4
VP1206N2	-60	0.8	TO-39	—	—	—
VP1206N5	-60	0.8	TO-220	IRF9523	-100	0.8
VP1208N1	-80	0.8	TO-3	IRF9132	-100	0.4
VP1208N2	-80	0.8	TO-39	—	—	—
VP1208N5	-80	0.8	TO-220	IRF9522	-100	0.8
VP1209N1	-90	0.8	TO-3	IRF9132	-100	0.4
VP1209N2	-90	0.8	TO-39	—	—	—
VP1209N5	-90	0.8	TO-220	IRF9522	-100	0.8

MOSPOWER

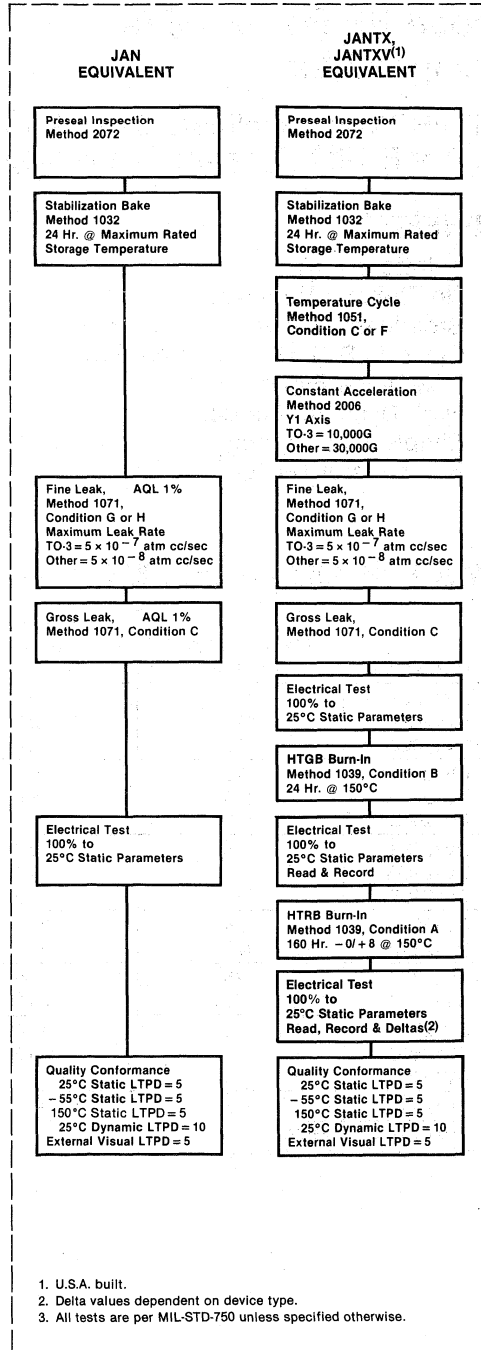
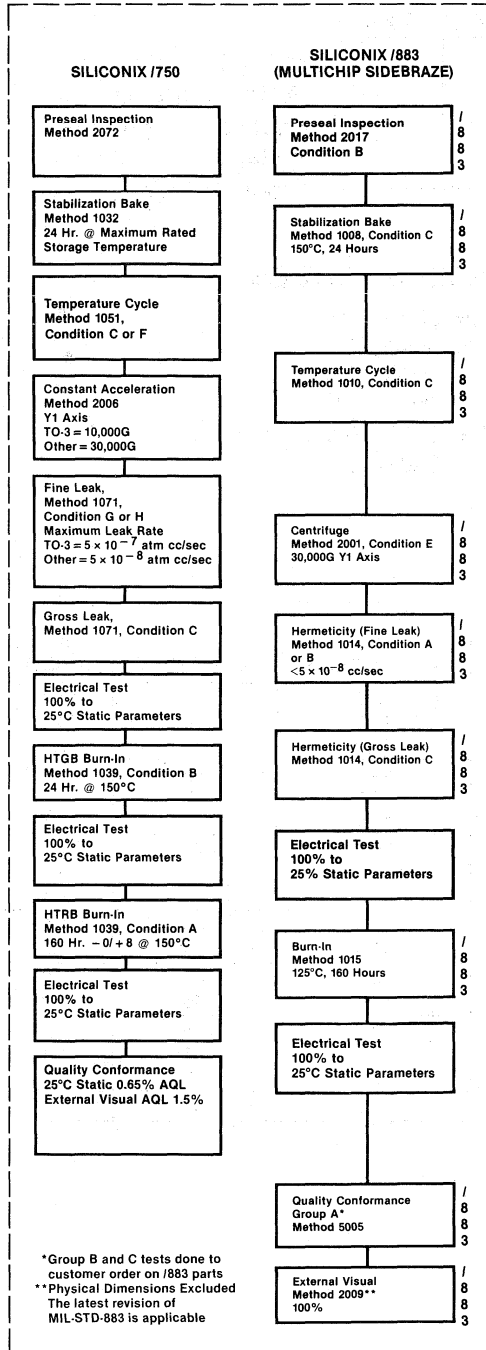
Commercial/Industrial Process Flow⁽¹⁾



MOSPOWER Military/Hi-Rel Process Flows⁽³⁾

Standard Military/Hi-Rel Flows

19500 MIL-STD Optional Flows

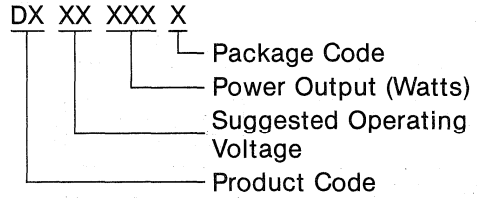


RF Power FETs Selector Guide

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers Class A, B, C, D or E. High Dynamic Range Amp

ORDERING INFORMATION



BENEFITS

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B C, D, or E Operation
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

PACKAGE CODES

- S = 380SOEF
- T = 500JOF
- U = 500SOEF
- V = Push-Pull
- W = C-220 Standard
- Z = 280SOE

12.5 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5V _{DC}	Min. Gain (dB) 12.5V, 175 MHz	Min. BV _{DSS}	θ _{Jc} (°C/W)
DV1202S	175	2.0	10.0	45	17.6
DV1202W	175	2.0	10.0	45	14.1
DV1202Z	175	2.0	10.0	45	17.6
DV1205S	175	5.0	10.0	45	8.8
DV1205W	175	5.0	10.0	45	7.0
DV1205Z	175	5.0	10.0	45	8.8
DV1210S	175	10.0	10.0	45	4.4
DV1210W	175	10.0	10.0	45	3.5
DV1210Z	175	10.0	10.0	45	4.4
DV1220S	175	20.0	10.0	45	2.2
DV1220W	175	20.0	10.0	45	1.8
DV1230T	175	30.0	9.5	45	1.5
DV1230W	175	30.0	9.3	45	1.2
DV1240T	175	40.0	9.0	45	1.1
DV1240U	175	40.0	8.6	45	1.1
DV1240W	175	40.0	9.0	45	0.9
DV1260T	175	60.0	8.0	45	0.73

*All parts tested at 20:1 VSWR.
 Note: See application notes AN80-4, AN80-6.

RF Power FETs Selector Guide (Cont'd)

28 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 28 VDC	Min. Gain (dB) 28V, 175 MHz	Min. BV _{DSS}	θ_{Jc} (°C/W)
DV2805S	175	5	10	80	17.6
DV2805W	175	5	10	80	14.1
DV2805Z	175	5	10	80	17.6
DV2810S	175	10	10	80	8.8
DV2810W	175	10	10	80	7.0
DV2810Z	175	10	10	80	8.8
DV2820S	175	20	10	80	4.4
DV2820W	175	20	10	80	3.5
DV2820Z	175	20	10	80	4.4
DV2840S	175	40	10	80	2.2
DV2840W	175	40	10	80	1.8
DV2880T	175	80	10	80	1.1
DV2880U	175	80	10	80	1.1
DV2880W	175	80	10	80	0.9
DV28120T	175	120	10	80	0.73
DV28120U	175	120	9	80	0.73
VMP4	175	20	10	60	4.4

*All parts tested at 20:1 VSWR.

28 Volt Push-Pull — DC-300 MHz Series

Part Number	Test Frequency (MHz)	Test Voltage (V _{DS})	P _{in} (Max.) (Watts)	P _{out} @ 28V (Watts)	G _{ps} (Min.) Power Gain (dB)	θ_{Jc} Thermal Impedance (°C/W)
DV2880V	175	28	8	80	10	1.1
DV28120V	175	28	12	120	10	0.73

100 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5VDC	Min. Gain (dB) 12.5V, 175 MHz	Min. BV _{DSS}	θ_{Jc} (°C/W)
DVD030S	175	25	13	220	4.40
DVD150T	175	120	10	220	0.73

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Analog Switches/ICs	7
Worldwide Sales Offices	8

Analog Switches Selector Guide

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches	
Battery Operated or Battery Back-Up Supply	1) Low Power	Low Supply Current		CMOS DG304-DG308, DG304A, DG307A, DG309 DG300-DG303, DG381-DG390, DG300A-DG303A, DG381A-DG390A	
	2) Minimum Number of Power Supplies	Only One or Two Supplies Needed		CMOS DG300-DG308A, DG300A-DG307A, DG309 (Can Also Be Used As Single Supply) CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 (For MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)	
	3) Low Standby Power	Low Standby Current		CMOS DG304-DG308A, DG211, DG304A-DG307A, DG309, DG212	
Audio	1) Low Signal Distortion	Low $r_{DS(on)}$; Constant $r_{DS(on)}$	JFET is Constant, $r_{DS(on)}$; Signal Range Limited Toward Negative Supply; CMOS Slight $r_{DS(on)}$ Variation, Full Signal Range	JFET DG180-DG191 CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045 DG243 (Make-Before-Break)	
	2) Low Noise (Channel)	Low $r_{DS(on)}$		CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243 JFET DG180-DG191	
	3) Wide Signal Range	$\pm 15V$ Signal Range			CMOS DG300-DG308, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243 CMOS DG200, DG200A, DG201, DG201A, DG202, DG211, DG212 (MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
		Signal Range is From the Positive Supply to Above the Negative Supply	Higher $r_{DS(on)}$ (Must Stay Above Negative Supply By 5V to 7.5V)		JFET (75Ω) DG182, DG185, DG188, DG191 (10 Ω , 30 Ω) Remainder of DG181-DG190 Family
	4) Large Dynamic Range	Wide Signal Range and Low Thermocouple Noise			CMOS DG304-DG308A, DG304A-DG307A, DG309 DG300-DG303, DG381-DG390, DG211, DG300A-DG303A, DG381A-DG390A, DG212
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	High OFF Isolation	Higher $r_{DS(on)}$	JFET (30Ω, 75Ω) DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243	
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	Low $r_{DS(on)}$	Lower OFF Isolation	JFET (10Ω) DG180, DG183, DG186, DG189 (30 Ω) DG181, DG184, DG187, DG190 CMOS DG300-DG308A, DG211 DG300A-DG307A, DG309, DG212	

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Sample and Hold	1) Low Droop Rate	Low Leakage	Higher ON Resistance	CMOS DG300A-DG307A, DG300, DG309 DG381A-DG390A CMOS DG300-DG308A, DG381-DG390, DG5040-DG5045 JFET DG180-DG191 CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212
	2) Low Sample to Hold Offset	Low Charge Coupling	Higher ON Resistance	CMOS DG200A, DG201A, DG202, DG212 CMOS DG200, DG201, DG211 JFET DG181, DG182 (30 Ω , 75 Ω) DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300-DG308A, DG300A-DG307A, DG309
	3) Fast Acquisition Speed	Low ON Resistance	Higher Leakage Higher Charge Coupling	JFET (10Ω) DG180, DG183, DG186, DG189 (30 Ω , 75 Ω) Remainder of DG181-DG191 Family CMOS DG300-DG307, DG381-DG390, DG300A-DG307A CMOS DG200, DG201, DG211, DG212 CMOS DG381A-DG390A, DG200A, DG201A, DG202
Switching to High Impedance Inputs	1) Low Error Voltage	Low Leakage		CMOS DG300A-DG307A, DG381A-DG390A CMOS DG300-DG307, DG381-DG390, DG5040-DG5045, DG200-DG201, DG211, DG200A, DG201A, DG212
	2) Low Switching Transient Error Voltage	Low Charge Coupling		CMOS DG200A, DG201A, DG202, DG212 CMOS DG200, DG201, DG211 DG300-DG307, DG381-DG390, DG300A-DG307A, DG381A-DG390A
Low Cost	1) Best Performance for Lowest Cost	Monolithic Good Switch Performance		CMOS DG211, DG212, DG303, DG309, DG308A, DG300-DG307, DG5040-DG5045 DG200, DG201, DG381-DG390, DG200A, DG201A, DG202, DG300A-DG307A, DG243, DG381A-DG390A
Military System	1) Hi-Rel Specified			BS9000 JM38510/XXXX
Differential Signal Switching	1) Good Matching of Switch Parameters	Monolithic Switch		CMOS DG300, DG302, DG303, DG304, DG243, DG306, DG307, DG308A, DG381, DG384, DG390, DG309 CMOS DG200, DG201, DG211, DG5040-DG5045, DG300A, DG302A, DG303A, DG304A, DG306A, DG307A, DG309, DG381A, DG384A, DG390A, DG200A, DG207A, DG202, DG212
	2) Low Thermo-couple Offset Voltage	Drain and Source of FET Switch in Close Proximity on <i>Small Chip</i> Low Power Dissipation on Switch Driver	JFET Switches Not Monolithic	JFET DG183, DG184, DG185 CMOS DG304, DG306, DG307, DG308A DG304A, DG309 DG300-DG303, DG300A-DG303A, DG306A, DG307A, DG381-DG390, DG381A-DG390A, DG309

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Small Signal (<1V)	1) Low Noise (Channel)	Low $r_{DS(on)}$	Higher Leakages	JFET (10Ω) DG180, DG183, DG186, DG189 (30 Ω , 75 Ω) Remainder of DG181-DG191 Family
	2) Low Charge Coupling			CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212, DG308A CMOS DG300-DG308, DG381-DG390, DG211
	3) High Impedance Inputs of Load	Low Leakage	Higher $r_{DS(on)}$	CMOS DG300-DG308A, DG381-DG390, DG211, DG5040-DG5045, DG243, DG309 DG200-DG201 JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212
	4) Low Thermocouple Offset Voltage	Low Power Switch		
Drain and Source of FET Switch in Close Proximity on <i>Small Chip</i>				JFET DG180-DG190 Family
Multiplexing	1) Break-Before-Make Switching	t_{ON} is Greater Than t_{OFF}		CMOS DG506, DG506A, DG507, DG507A, DG508, DG508A, DG509, DG509A, DG528, DG529 (Latchable)
	2) Binary Controlled Logic Inputs	Binary Decoding Stage on Chip		PMOS DG501, DG503
	3) Differential Multiplexing	Dual Switching Action		CMOS DG507, DG509, DG507A, DG509A, DG529
	4) D/A Conversion	Binary Weighted ON Resistance and Channel Resistance to Minimize Error		NMOS DG515, DG516

Bold Print = Recommended for the application

Analog Switches

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (Note 4)	I _{DS(on) Max} (Q) (Note 4)	I _{D(off)} (mA)	Switching Time (μsec)	Logic Levels (V)		Opt. Supply Voltage (V)		Ref. Sup. V _R	Comments	Switch Configuration		
						V _{INH}	V _{INL}	(+) Sup. V _R	(-) Sup. V _L					
SINGLE CHANNEL SPST														
DG5040	Plus 40 CMOS	+15 to -15	50	1	1.0	0.5	0.8	2	15	-15	5	TTL Compatible	1 SPST Switch per Package	
TWO CHANNEL SPST														
DG180	N-JFET	+10 to -12.5	10	10	0.3	0.25	0.8	2.0	10	-20	5	Break-Before-Make	<p>2 SPST Switches per Package</p>	
DG181	N-JFET	+10 to -12.5	30	1	0.15	0.13	0.8	2.0	10	-20	5	Break-Before-Make		
DG182	N-JFET	+10 to -15	30	1	0.15	0.13	0.8	2.0	10	-20	5	Break-Before-Make		
DG200	CMOS	+10 to -15	75	1	0.25	0.13	0.8	2.0	15	-15	5	15 V Supplies JAN/1102		
DG200A	Plus 40 CMOS	+15 to -15	70	2	1.0	0.5	0.8	2.4	15	-15	5	15 V Supplies JAN/1203		
DG281	N-JFET	+15 to -15	300	0.2	0.15	0.13	0.8	2.0	15	-15	5	TTL In		
DG300	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Charge Injection		
DG300A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, TTL In JAN/11601		
DG304	CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	5	Low Power, CMOS In		
DG304A	Plus 40 CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	5	Low Power, CMOS In		
DG381	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, CMOS In		
DG381A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, CMOS In		
DG5041	Plus 40 CMOS	+15 to -15	50	1	1.0	0.5	0.8	2.0	15	-15	5	Low Power, DG181 Pin Out		
FOUR CHANNEL SPST														
DG201	CMOS	+15 to -15	175	1	1.0	0.5	0.8	2.4	15	-15	5	JAN/12304	<p>4 SPST Switches per Package</p>	
DG201A	Plus 40 CMOS	+15 to -15	175	1	1.0	0.5	0.8	2.4	15	-15	5	TTL In		
DG202	Plus 40 CMOS	+15 to -15	175	1	1.0	0.5	0.8	2.4	15	-15	5	TTL In		
DG211	Plus 40 CMOS	+15 to -15	175	5	0.6	0.4	0.8	2.4	15	-15	5	Low Cost, TTL In		
DG212	Plus 40 CMOS	+15 to -15	175	5	0.6	0.46	0.8	2.4	15	-15	5	Low Cost, TTL In		
DG308A	Plus 40 CMOS	+15 to -15	100	1	0.2	0.15	3.5	11.0	15	-15	5	Low Cost CMOS In		
DG309	Plus 40 CMOS	+15 to -15	100	5	0.2	0.15	3.5	11.0	15	-15	5	Low Cost CMOS In		
ONE CHANNEL SPDT														
DG186	N-JFET	+10 to -12.5	10	10	0.3	0.25	0.8	2.0	10	-20	5	Break-Before-Make		<p>1 SPST Switch per Package</p>
DG187	N-JFET	+10 to -12.5	30	1	0.15	0.13	0.8	2.0	10	-20	5	Break-Before-Make		
DG188	N-JFET	+10 to -15	75	1	0.25	0.13	0.8	2.0	10	-20	5	Break-Before-Make		
DG287	N-JFET	+15 to -15	300	0.2	0.15	0.13	0.8	2.0	15	-15	5	Break-Before-Make		
DG301	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, TTL In JAN/11602		
DG301A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, CMOS In		
DG305	CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	5	Low Power, CMOS In		
DG305A	Plus 40 CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	5	Low Power, CMOS In		
DG387A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	5	Low Power, CMOS In		
DG5042	Plus 40 CMOS	+15 to -15	50	1	1.0	0.5	0.8	2.0	15	-15	5	Low Power, DG187 Pin Out		

NOTES:

- The devices shown in **boldface** are recommended parts for new designs.
- The appropriate switching characteristic for multiplexers is **T_{TRANSITION}**, not **T_{ON}**, **T_{OFF}**.
- V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 V are used.
- Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, **DS** is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
- Device normally operates with resistor to +10 V.

Analog Switches (Cont'd)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	I _{DS(on)} Max (I) (Note 4)	I _{D(off)} (mA)	Switching Time (μsec)		Logic Levels (V)		Opt. Supply Voltage (V)		Ref. Sup. V _R	Comments	Switch Configuration	
					t _{ON}	t _{OFF}	V _{INH}	V _{INH}	(+)	(-)				
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to -12.5	10	10	0.3	0.25	0.8	2.0	10	-20	5	Break-Before-Make 15 V Supplies	<p>2 SPDT Switches per Package</p>	
DG190	N-JFET	+10 to -12.5	10	10	0.3	0.25	0.8	2.0	15	-15	5	Break-Before-Make JAN/11107		
DG191	N-JFET	+10 to -12.5	30	1	0.15	0.13	0.8	2.0	10	-20	5	15 V Supplies		
DG191	N-JFET	+10 to -15	75	1	0.25	0.13	0.8	2.0	10	-20	5	Break-Before-Make JAN/11108		
DG191	N-JFET	+10 to -10	75	1	0.25	0.13	0.8	2.0	15	-15	5	15 V Supplies		
DG243	Plus 40 CMOS	+15 to -15	50	1	0.5	1.0	0.8	2.0	15	-15	5	Break-Before-Make (DG191 Pin Out)		
DG290	N-JFET	+15 to -7.5	300	0.2	0.15	0.13	0.8	2.0	15	-15	5	Low Power, TTL In		
DG303	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, CMOS In		
DG303A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, CMOS In		
DG307	CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	—	Low Power, DG190 Pin Out		
DG307A	Plus 40 CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	—	Low Power, DG190 Pin Out		
DG390	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, DG190 Pin Out		
DG390A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, DG190 Pin Out		
DG5043	Plus 40 CMOS	+15 to -15	50	1	1.0	0.5	0.8	2.0	15	-15	5	—		
ONE CHANNEL DPST														
DG5044	Plus 40 CMOS	+15 to -15	50	1	1.0	0.5	0.8	2	15	-15	5	TTL Compatible	<p>1 DPST Switch per Package</p>	
TWO CHANNEL DPST														
DG183	N-JFET	+10 to -12.5	10	10	0.3	0.25	0.8	2.0	10	-20	5	Break-Before-Make 15 V Supplies		
DG184	N-JFET	+10 to -12.5	30	1	0.15	0.13	0.8	2.0	10	-20	5	Break-Before-Make 15 V Supplies		
DG185	N-JFET	+10 to -15	75	1	0.25	0.13	0.8	2.0	10	-20	5	Break-Before-Make 15 V Supplies		
DG185	N-JFET	+10 to -10	75	1	0.25	0.13	0.8	2.0	15	-15	5	Break-Before-Make 15 V Supplies		
DG384	N-JFET	+15 to -15	300	0.2	0.15	0.13	0.8	2.0	15	-15	5	Low Power, TTL In		
DG302	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, CMOS In		
DG302A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, CMOS In		
DG386A	CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	—	Low Power, CMOS In		
DG386A	Plus 40 CMOS	+15 to -15	50	1	0.25	0.15	3.5	11.0	15	-15	—	Low Power, CMOS In		
DG394A	CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, DG184 Pin Out		
DG394A	Plus 40 CMOS	+15 to -15	50	1	0.3	0.25	0.8	4.0	15	-15	—	Low Power, DG184 Pin Out		

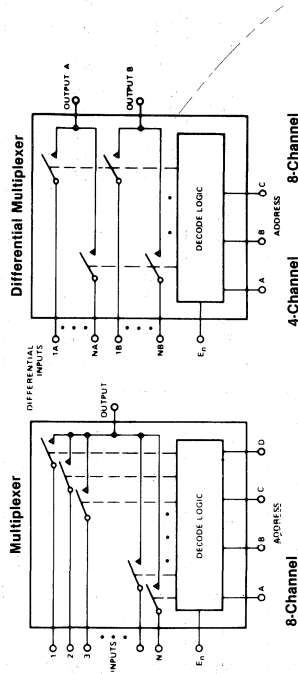
NOTES:

- The devices shown in **boldface** are recommended parts for new designs.
- The appropriate switching characteristic for multiplexers is **TRANSITION**, not **ON-OFF**.
- V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 V are used.
- Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, V_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
- Device normally operates with resistor to +10 V.

Multiplexers with Input Latches

Basic Part No.	Process Type	Analog Voltage Range (V) (Note 4)	t _{D(on)} Max (t) (Note 4)	I _{D(off)} (nA)	Transition Time (μsec) (Note 2)	Logic Levels (V)		Supply Voltage (V)		Comments
						V _{INH}	V _{INH}	(+) Sup. V ₊	(-) Sup. V ₋	
EIGHT CHANNEL MUX + ENABLE										
DG501	PMOS	+5 to -5	150-240	8	1.5	0.6	3.5	5	-20	Logic Pullup Resistors
DG503	PMOS	+10 to -10	150-800	8	1.5	0.6	8.5	10	-20	
DG508A	Plus 40 CMOS	+10 to -15	400	10	1.0	0.8	2.4	15	-15	Break-Before-Make
DG528	Plus 40 CMOS	+15 to -15	400	10	1.0	0.8	2.4	+15	-15	Latches On Inputs
SIXTEEN CHANNEL MUX + ENABLE										
DG506A	Plus 40 CMOS	+15 to -15	400	10	1.0	0.8	2.4	15	-15	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE										
DG509A	Plus 40 CMOS	+15 to -15	400	10	1.0	0.8	2.4	15	-15	Break-Before-Make
DG529	Plus 40 CMOS	+15 to -15	400	10	1.0	0.8	2.4	15	-15	Latches On Inputs
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE										
DG507A	Plus 40 CMOS	+15 to -15	400	5	1.0	0.8	2.4	+15	-15	Break-Before-Make

Switch Configurations



- NOTES:**
1. The devices shown in boldface are recommended parts for new designs.
 2. The appropriate switching characteristic for multiplexers is TRANSITION, not TOV, TOF.
 3. V_{REG} = 1.5 V is used when supply voltages < ±15 V are used. Not provided when supply voltages of ±15 are used.
 4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, t_D is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
 5. Device normally operates with resistor to +10 V.

Analog Switches Product Information

Drivers and Gates

Basic Part No. (Notes 1 & 2)	Switch Type	rDS(on) Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				tON	tOFF		V _{INL}	V _{INH}	(+) Sup. V ₁	(-) Sup. V ₂	Logic Sup. V ₁	
One Channel SPST												
DG5040	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	
Two Channel SPST												
DGM111	PMOS	75-200	20	0.3	1.0	0	0.5	4.6	10	-20	5	
DG133	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG181
DG134	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG182
DG141	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	—	See DG180
DG151	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	—	See DG180
DG152	N-JFET	50	15	0.8	1.6	1	0.8	2.5	15	-15	—	See DG181
SG180	N-JFET	10	20	0.3	0.25	0	0.8	2.0	10	-20	5	Break-Before-Make
		10	15	0.3	0.25	0	0.8	2.0	15	-15	5	15V Supplies
*DG181	N-JFET	30	20	0.15	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		30	15	0.15	0.13	0	0.8	2.0	15	-15	5	15V Supplies
*DG182	N-JFET	75	20	0.25	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		75	20	0.25	0.13	0	0.8	2.0	15	-15	5	15V Supplies
DG200	CMOS	70	30	1.0	0.5	0	0.8	2.4	15	-15	—	
*DG200A	CMOS Plus-40	70	30	1.0	0.5	0	0.8	2.4	15	-15	—	
DG281	N-JFET	300	20	0.15	0.13	0	0.8	2.0	15	-15	5	Break-Before-Make
*DG300	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	-15	—	
*DG381	CMOS	50	30	0.300	0.250	0	0.8	4.0	15	-15	—	
*DG304	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	-15	—	CMOS compatible
*DG5041	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	Break-Before-Make
Four Channel SPST												
*DG172	PMOS	150-450	20	0.3	0.75	0	0.8	2.0	10	-20	5	
DG201	CMOS	175	30	1.0	0.5	0	0.8	2.4	15	-15	—	
*DG201A	CMOS Plus-40	175	30	0.6	0.45	0	0.8	2.4	15	-15	—	
*DG202	CMOS Plus-40	175	30	0.6	0.45	1	0.8	2.4	15	-15	—	
*DG211	CMOS Plus-40	175	30	1.0	0.5	0	0.8	2.4	15	-15	5	
*DG212	CMOS Plus-40	175	30	1.0	0.5	1	0.8	2.4	15	-15	5	
*DG308A	CMOS Plus-40	100	30	0.2	0.15	1	3.5	11.0	15	-15	—	Single Supply Operation
*DG309	CMOS Plus-40	100	30	0.2	0.15	0	3.5	11.0	15	-15	—	Single Supply Operation
Five Channel SPST												
DG125	PMOS	100-450	20	0.3	2.0	0	0.5	4.6	10	-20	5	
One Channel SPDT												
DG143	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG188
DG144	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG187
DG146	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	—	See DG186
DG161	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	—	See DG186
DG162	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	—	See DG187
DG186	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JEFT	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
*DG187	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
*DG188	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
DG287	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make

*Devices recommended for new designs are indicated in bold face type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	r _{DS(on)} Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t _{ON}	t _{OFF}		V _{INL}	V _{INH}	(+) Sup. V ₁	(-) Sup. V ₂	Logic Sup. V _I	
One Channel SPDT (Cont'd)												
*DG301	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	CMOS compatible Same as HAD30021XX Break-Before-Make
*DG387	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
*DG305	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	-15	—	
SI3002	PMOS	100-400	20	1.0	1.5	(Note 5)	0.8	2.0	10	-20	—	
*DG5042	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	
Two Channel SPDT												
DG189	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5		
*DG190	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5		
*DG191	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5		
*DG243	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	Make-Before-Break
DG290	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make
*DG303	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	CMOS compatible Break-Before-Make
*DG390	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
*DG307	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	-15	—	
*DG5043	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	
CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	-15	—		
One Channel DPST												
*DG5044	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make
Two Channel DPST												
DG126	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG185
DG129	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG184
DG140	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	—	See DG183
DG153	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	—	See DG183
DG154	N-JFET	50	15	0.6	1.6	1	0.8	2.5	15	-15	—	See DG185
DG183	N-JFET	10	20	0.3	0.25	1	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	10	15	0.3	0.25	1	0.8	2.0	15	-15	5		
*DG184	N-JFET	30	20	0.15	0.13	1	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	30	15	0.15	0.13	1	0.8	2.0	15	-15	5		
*DG185	N-JFET	75	20	0.25	0.13	1	0.8	2.0	10	-20	5	Break-Before-Make 15V Supplies
N-JFET	75	20	0.25	0.13	1	0.8	2.0	15	-15	5		
DG284	N-JFET	300	20	0.15	0.13	1	0.8	2.0	15	-15	5	Break-Before-Make
*DG302	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	-15	—	CMOS compatible Break-Before-Make
*DG384	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	-15	—	
*DG306	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	-15	—	
*DG5045	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	
CMOS	50	30	0.250	0.150	1	3.5	11.0	15	-15	—		
One Channel DPDT												
DG139	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG191
DG142	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG190
DG145	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	—	See DG189
DG163	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	—	See DG189
DG164	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	—	See DG191
Eight Channel MUX + Enable												
DG501	PMOS	150-250	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	—	Logic Pullup Resistors
DG503	PMOS	150-800	20	1.5	(Note 8)	(Note 7)	0.6	8.5	10	-20	—	
DG508	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	

*Devices recommended for new designs are indicated in **bold face** type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	r _{DS(on)} Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t _{ON}	t _{OFF}		V _{INL}	V _{INH}	(+) Sup. V ₁	(-) Sup. V ₂	Logic Sup. V ₁	
Eight Channel MUX + Enable (Cont'd)												
*DG508A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
*DG528	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
SI3705	PMOS	150-400	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	—	See DG501/No Pullup Resistors
Sixteen Channel MUX + Enable												
DG506	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG506A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
Four Channel Differential MUX												
DG509	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG509A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
*DG529	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
Eight Channel Differential MUX + Enable												
DG507	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG507A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
Four Channel SPDT D/A Converter Summing Node Switches												
DG515	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	R ₁ = 6.25Ω, R ₂ = 12.5Ω, R ₃ = 25Ω, R ₄ = 50Ω
Ten Channel SPDT D/A Converter Summing Node Switches												
DG516	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	R ₁ = 100Ω, R ₂ = 200Ω, R ₃ = 400Ω, R ₄ = 800Ω, R ₅ = 1600Ω, R ₆₋₁₀ = 3200Ω

Multiple FET Switches

Siliconix P-Channel MOSFET & DMOS Switches are available for such applications as sequential switching (commutation), signal processing, modulation, and A-to-D conversion. The MOSFET is normally OFF. These devices are also available with Siliconix drivers in a single package.

Basic Part Number (Note 2)	S O D			Switch Type	Pull Up On Gate	r _{DS} Max. (V)		BV _{DSS}	I _{S(off)} (nA)	V _{GS} (th)		C _{gs} Typ. (pF)	C _{ds} Typ. (pF)	C _{sb} Typ. (pF)
	R C S	R A S	G A S			@ V _S = +10V	@ V _S = -10V			Min.	Max.			
G115	6	1	6	SP6T	Yes	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G118	6	1	8	SP6T	No	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G119	6	2	3	DP3T	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G122	4	2	2	DPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G123	4	2	4	2 × SPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
*SD5000	4	4	4	4 × SPST	No	50	50	20	10.0	0.1	2.0	3.5	0.5	4
*SD5001	4	4	4	4 × SPST	No	50	50	10	10.0	0.1	2.0	3.5	0.5	4
*SD5002	4	4	4	4 × SPST	No	50	50	15	10.0	0.1	2.0	3.5	0.5	4
*SD5200	4	4	4	4 × SPST	No	80	80	30	1000	0.5	2.0	3.5	0.5	4

*Devices recommended for new designs are indicated in **bold face** type.

Drivers for MOS FET Switches

These drivers were designed to function as a level shifter and buffer between low level logic and the control gate of FET analog switches. Output voltage ratings are as high as 50V.

Basic Part Number (Note 2)	I N P U T S	O U T P U T S	Function and Uses	ON Level $V_{(OUT)ON-V_2}$ at Rated Current(s)	OFF Level $V_{(OUT)OFF}$ at Rated Current or $I_{(OUT)OFF}$ at Rated Voltage	Input Logic for V_{OUT} (low)	V_{INL} (V)	V_{INH} (V) (I_{INH} (mA))	Optimum Supply Voltage (V)				Switching Time (μ s)	
									V_1	V_2	V_L	V_R	t_{ON}	t_{OFF}
D125	6	6	Six Separate MOSFET-Drivers	0.4V@5mA	0.1 μ A@10V	0	0.5	4.6	(Note 9)	-20	5	—	0.5	1.2
D129	7	4	Four Channel (BV = 50) MOSFET-Driver with Decode	0.7V@10mA	0.1 μ A@10V	1	0.7	2.2	(Note 9)	-20	—	—	0.25	0.8
*D169	2	4	Dual High-Speed Drivers with Complementary Outputs designed to drive high-capacity loads.	1.2V@1mA	1.1V@1mA	Output & Complement Available	0.8	2.0	15	-15	5	0	t_{d+}	t_{d-}
				3.0V@40mA	2.5V@40mA		0.8	2.0	15	-15	5	0	0.17	0.20

NOTES:

- (1) *Devices recommended for new designs are indicated in **bold face** type.
- (2) See pages 7-26 through 7-28 for package and temperature designations for most products.
- (3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
- (4) Input reference voltage of 2.5V is required (see data sheets).
- (5) See data sheet for switch state of differential switches.
- (6) Current Driven Device— $I_{INH} = 1$ mA.
- (7) For truth table see data sheet.
- (8) The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON} , t_{OFF} .
- (9) Device normally operates with resistor—to +10V.
- (10) ($C_L = 35$ pF).

LSI/Linear Product Information

A/D Converters

3½-Digit High Performance	LD110/LD111A 16-pin plastic DIPs	±3½-Digit A/D Converter Accuracy 0.02% ±1 count Auto zero Auto polarity 10µV resolution Typical T.C. of 5 ppm/°C A usable 20mV scale	Three voltage ranges: 1.999V, 199.9mV & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
4½-Digit	LD120/LD121A 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
4½-Digit	LD122/LD121A 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count 1µV resolution for 20 mV FS Auto zero Auto polarity TTL compatibility Internal clock Linear to 28,500 counts	MUX BCD outputs Two over-range outputs, under- range, blink inhibit and convert-on-command capability Interfaces to external circuitry and microprocessors

Micropower Linears

Triple Op Amp	L144 14-pin plastic, ceramic, flat- pack & Dice	±1.5 to ±18V supply Programmable supply current Internally compensated 0.4V/µs slew rate	80dB gain with 20kΩ load Drives large capacitive loads ±30V differential input Monolithic construction
Quad Comparator	L161 16-pin plastic, ceramic, flat- pack & Dice	±1.5 to ±18V supply Single supply operation Programmable supply current 3V/µs slew rate	Gain greater than 20V/mV Sensing near ground ±30V differential input CMOS Logic compatible

Telecommunications Products

Loop Disconnect Dialer (pulse dialer)	DF320 18-lead ceramic, plastic & CERDIP		Operation from 2.5V to 5V supply Low standby power dissipation; 3µW Low dynamic power consump- tion; 600µW On-chip oscillator for 3.579545 MHz crystal Redial capability Hold capability delays impulsing Post-impulsing pause of 33 ms Mask during impulsing and inter- digit pause Selectable make-break ratio 10, 16, 20, 932 Hz impulsing rates Inter-digit pause of 800 ms
--	--	--	--

LSI/Linear Product Information (Cont'd)

Loop Disconnect Dialer (pulse dialer) (Cont'd)	DF320A		Same as DF320, except post-impulsing pause of 500ms
	DF322		Same as DF320, except mask during impulsing only
	DF328 16-lead plastic		Same as DF320, except 10, 932Hz impulsing rates No hold capability during impulsing

Interface

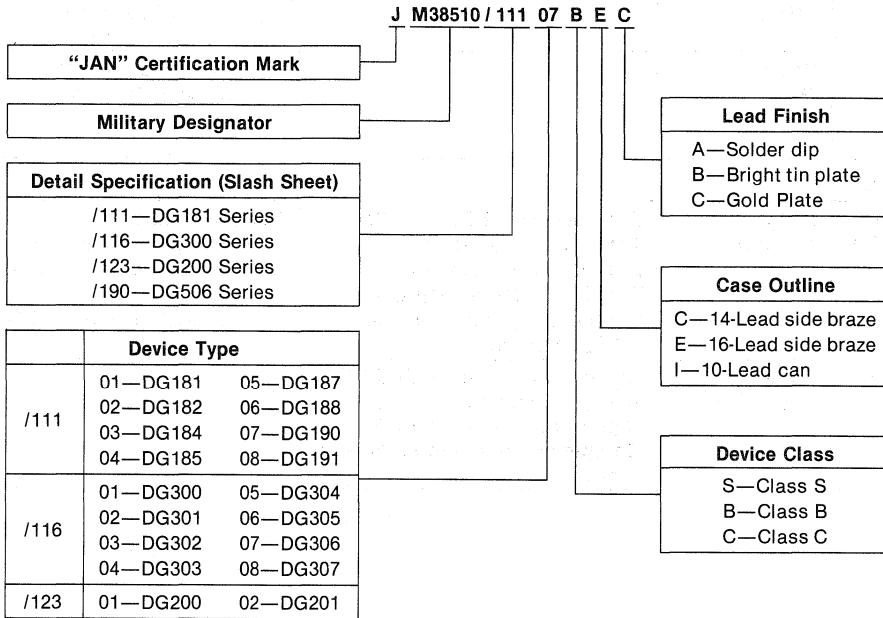
Four-digit MUX'd BCD to LCD Display Driver	DF412 40-pin plastic	Decodes MUX BCD to LCD 4-Digit drive capability Low power consumption TTL, DTL, CMOS compatible Can be ganged to drive more than 4 digits	7-segment LCD drive signals Drives large LCDs easily Can be clocked using an external oscillator Internal oscillator available
Dual High-Voltage Driver	D169 14-pin DIP	Designed to drive MOSPOWER Accepts TTL input High output drive; up to 36V Complementary outputs on each channel	

Analog Switches

JAN 38510

Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers.

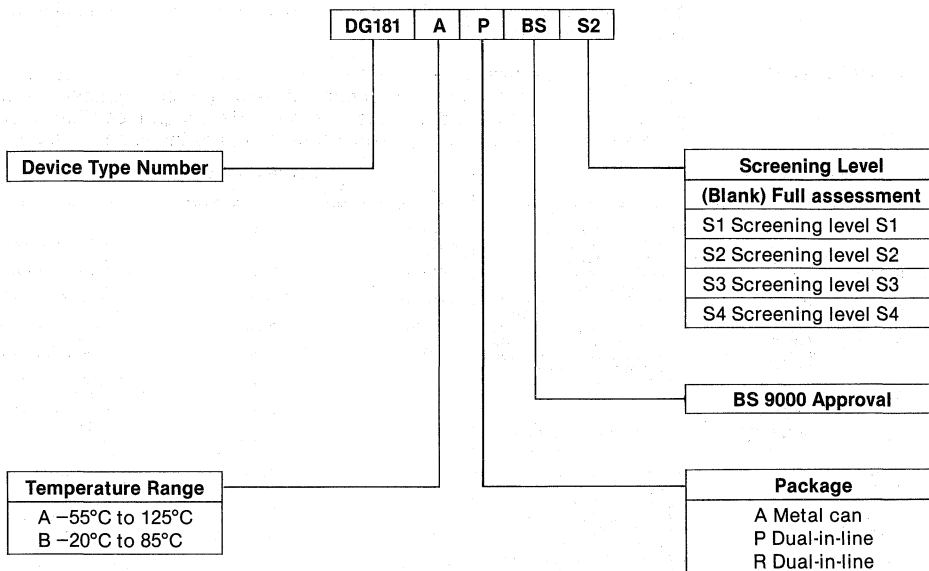
JAN Part Numbering System



Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BFC	SJM183BFC	DG183AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200AP/883
JM38510/12303BIC	SJM200BIC	DG200AA/883
JM38510/12304BEC	SJM201BEC	DG201AP/883

Analog Switches BS9000

BS9000 Part Numbering System



Approved Parts		Awaiting Approval*
Generic Part No.	Generic Part No.	Generic Part No.
DG126/ /BS	DG180/ /BS	DG281/ /BS
DG129/ /BS	DG181/ /BS	DG284/ /BS
DG133/ /BS	DG182/ /BS	DG287/ /BS
DG134/ /BS	DG183/ /BS	DG290/ /BS
DG139/ /BS	DG184/ /BS	DG300/ /BS
DG140/ /BS	DG185/ /BS	DG301/ /BS
DG141/ /BS	DG186/ /BS	DG302/ /BS
DG142/ /BS	DG187/ /BS	DG303/ /BS
DG143/ /BS	DG188/ /BS	DG304/ /BS
DG144/ /BS	DG189/ /BS	DG305/ /BS
DG145/ /BS	DG190/ /BS	DG306/ /BS
DG146/ /BS	DG191/ /BS	DG307/ /BS
DG151/ /BS	DG200/ /BS	DG308/ /BS
DG152/ /BS	DG201/ /BS	DG381/ /BS
DG153/ /BS	DG501/ /BS	DG384/ /BS
DG154/ /BS	DG503/ /BS	DG387/ /BS
DG161/ /BS	DG506/ /BS	DG390 /BS
DG162/ /BS	DG507/ /BS	
DG163/ /BS	DG508/ /BS	
DG164/ /BS	DG509/ /BS	
	SI3705/ /BS	

*Contact one of the Siliconix sales offices for latest information.

Analog Switch and ICs Cross Reference Guide

Direct Replacement: Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Similar Function: Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts usually have different pin configurations. Before selecting a device as a substitute, compare the specifications.

Mfr's Device Number	SILICONIX DEVICE			Mfr's Device Number	SILICONIX DEVICE		
	Direct Replacement	Similar Function	Manufacturer's Description		Direct Replacement	Similar Function	Manufacturer's Description
AD7501		DG508A	8 x Analog Mux, CMOS	CAG10D	DG180(1/2)		
AD7502		DG509A	4 x Diff Analog Mux, CMOS	CAG13	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7503		DG508A	8 x Analog Mux, CMOS	CAG13A	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7506	DG506A		16 x Analog Mux, CMOS	CAG13C	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7507	DG507A		8 x Diff Analog Mux, CMOS	CAG13D	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7510		DG201A	4 x SPST Analog Switch, CMOS	CAG14	DG181	SPST JFET Analog Switch, High Speed	
AD7511		DG201A	4 x SPST Analog Switch, CMOS	CAG14A	DG181	SPST JFET Analog Switch, High Speed	
AD7512		DG303	2 x SPST Analog Switch, CMOS	CAG21	DG184	2 x DPST JFET Analog Switch, Low f _{DS}	
AD7513	DG200A	DG300	2 x SPST Analog Switch, CMOS	CAG22	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7516		DG201A	4 x SPST Analog Switch, CMOS	CAG23	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AD7519		DG515	4 x SPDT Steering Switch	CAG24	DG134	2 x SPST JFET Analog Switch, Low f _{DS} , Low Power	
ADG200	DG200A		2 x SPST Analog Switch, CMOS	CAG27	DG141, DG180	2 x SPST JFET Analog Switch, Very Low f _{DS}	
ADG201	DG201A		4 x SPST Virtual Gnd Analog Sw	CAG27-10	DG141, DG180	2 x SPST JFET Analog Switch, Very Low f _{DS}	
AH0014		DG303, DG307	DPDT MOG Analog Switch	CAG30	DG181(1/2)	SPST JFET Analog Switch, Low f _{DS}	
AH0015		DG172, DG201A	4 x SPST MOS Analog Switch	CAG42	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AH0019		DG184, DG302, DG306	2 x DPST MOS Analog Switch	CAG45	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AH0126	DG126		2 x DPST JFET Analog Switch	CAG45A	DG181	2 x SPST JFET Analog Switch, Low f _{DS}	
AH0129	DG129		2 x DPST JFET Analog Switch	CAG48	DG184	2 x DPST JFET Analog Switch	
AH0145	DG145		2 x SPST JFET Analog Switch	CAG48A	DG184	2 x DPST JFET Analog Switch	
AH0134	DG134		2 x SPST JFET Analog Switch	CD4016	DG308A		
AH0139	DG139		DPDT Diff JFET Analog Switch	CD4051	DG508A		
AH0140	DG140		2 x DPST JFET Analog Switch	CD4052	DG509A		
AH0141	DG141		2 x SPST JFET Analog Switch	CD4067	DG506A		
AH0142	DG142		2 x DPST JFET Analog Switch	CD4097	DG507A		
AH0143	DG143		2 x SPST JFET Analog Switch	CDA2	DG181	2 x SPST JFET Analog Switch	
AH0144	DG144		SPDT Diff JFET Analog Switch	CDA18	DG187	SPDT JFET Analog Switch, Fast	
AH0145	DG145		DPDT 2 x Diff JFET Analog Sw	CDA18A	DG187	SPDT JFET Analog Switch, Fast	
AH0146	DG146		SPDT Diff JFET Analog Switch	CDA23	DG186	SPDT JFET Analog Switch, Fast	
AH0151	DG151		2 x SPST JFET Analog Switch	CDR5	DG139(1/2)	Low-Level to High-Level Interface Circuit	
AH0152	DG152		2 x SPST JFET Analog Switch	CDR125AL	D125AL	6 x FET Driver	
AH0153	DG153		2 x DPST JFET Analog Switch	CDR125AP	D125AP	6 x FET Driver	
AH0154	DG154		2 x DPST JFET Analog Switch	CDR125BL	D125BL	6 x FET Driver	
AH0161	DG161		SPDT Diff JFET Analog Switch	CDR125BK	D125BP	6 x FET Driver	
AH0162	DG162		SPDT Diff JFET Analog Switch	CD4052	DG509A	4 x Diff CMOS Analog Mux	
AH0163	DG163		DPDT Diff JFET Analog Switch	CD4066	DG308A	4 x SPST CMOS Analog Switch	
AH0164	DG164		DPDT Diff JFET Analog Switch	D123	D123	6 x FET Driver	
AH2114		DG181, 184	DPST JFET Analog Switch	D125	D125	6 x FET Driver	
AH5009		DG172	4 x SPST Virtual Gnd Analog Sw	DG111	DGM111	4 x SPST MOS Analog Switch	
AH5010		DG172	4 x SPST Virtual Gnd Analog Sw	DG116		4 x SPST MOS Analog Switch	
AH5011		DG201A	4 x SPST Virtual Gnd Analog Sw	DG118		4 x SPST MOS Analog Switch	
AH5012		DG201A	4 x SPST Virtual Gnd Analog Sw	DG123	DG123	5 x SPST MOS Analog Switch	
AH5013		DG172(3/4)	3 x SPST Virtual Gnd Analog Sw	DG125	DG125	5 x SPST MOS Analog Switch	
AH5014		DG172(3/4)	3 x SPST Virtual Gnd Analog Sw	DG126	DG126	2 x DPST JFET Analog Switch	
AH5015		DG201A(3/4)	3 x SPST Virtual Gnd Analog Sw	DG129	DG129	2 x DPST JFET Analog Switch	
AH5016		DG201A(3/4)	3 x SPST Virtual Gnd Analog Sw	DG133	DG133	2 x SPST JFET Analog Switch	
AM181	DG181		SPST BIFET	DG134	DG134	2 x SPST JFET Analog Switch	
AM182	DG182		SPST BIFET	DG139	DG139	DPDT Diff JFET Analog Switch	
AM184	DG184		2 x DPST BIFET	DG140	DG140	2 x DPST JFET Analog Switch	
AM185	DG185		2 x DPST BIFET	DG141	DG141	2 x SPST JFET Analog Switch	
AM187	DG187		SPDT BIFET	DG142	DG142	DPDT Diff JFET Analog Switch	
AM188	DG188		SPDT BIFET	DG143	DG143	SPDT Diff JFET Analog Switch	
AM190	DG190		2 x SPDT BIFET	DG144	DG144	DPDT Diff JFET Analog Switch	
AM191	DG191		2 x SPDT BIFET	DG145	DG145	SPDT Diff JFET Analog Switch	
AM2009	G115, G118		6 x MOS Analog Switch	DG146	DG146	SPDT Diff JFET Analog Switch	
AM3705			8 x MOS Analog Mux	DG151	DG151	2 x SPST JFET Analog Switch	
AM3709			4 x SPST Virtual Gnd Analog Sw				
AM9710		DG172	4 x SPST Virtual Gnd Analog Sw				
AM9711		DG172	4 x SPST Virtual Gnd Analog Sw				
AM9712		DG201A	4 x SPST Virtual Gnd Analog Sw				
AY-S-9151		DF320	CMOS Loop Disconnect Dialer				
CAG6		DG141(1/2), DG180(1/2)	SPST JFET Analog Switch, Very Low f _{DS}				
CAG6-10		DG141(1/2), DG180(1/2)	SPST JFET Analog Switch, Very Low f _{DS}				
CAG7		DG145, 161, 186, 187	SPDT JFET Analog Switch, Very Low f _{DS}				
CAG7-10		DG145, 161, 186, 187	SPDT JFET Analog Switch, Very Low f _{DS}				
CAG10		DG181(1/2)	SPST JFET Analog Switch, Low f _{DS} , Fast				
CAG10A		DG180(1/2), DG181(1/2)	SPST JFET Analog Switch, Very Low f _{DS} , Fast				
CAG10B		DG181(1/2), DG182(1/2)	SPST JFET Analog Switch, Fast f _{DS}				
CAG10C		DG180(1/2), DG181(1/2)	SPST JFET Analog Switch, Very Low f _{DS} , Fast				

Analog Switch and ICs Cross Reference Guide (Cont'd)

Migr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description	Migr's Device Number	SILICONIX DEVICE Direct Replacement	Similar Function	Manufacturer's Description
DG152	DG152		2 x SPST JFET Analog Switch	HI-5051	DG190	DG290, DG303, DG307, DG390	2 x SPDT CMOS Analog Switch
DG153	DG153		2 x DPST JFET Analog Switch	HS-1000	DG506		16 x JFET Analog Mux
DG154	DG154		2 x DPST JFET Analog Switch	DG200A			2 x SPST CMOS Analog Switch
DG161	DG161		SPDT Diff JFET Analog Switch	DG201A			4 x SPST CMOS Analog Switch
DG162	DG162		DPDT Diff JFET Analog Switch	DG202			4 x SPST CMOS Analog Switch
DG163	DG163		DPDT Diff JFET Analog Switch	IH5001	DG133(1/2)		SPST JFET Analog Switch
DG164	DG164		DPDT Diff JFET Analog Switch	IH5002	DG134(1/2)		SPST JFET Analog Switch
DG181	DG181		2 x SPST CMOS Analog Switch	IH5003	DG133		2 x SPST JFET Analog Switch
DG181	DG381		2 x SPST CMOS Analog Switch	IH5004	DG134		2 x SPST JFET Analog Switch
DG182	DG182		2 x SPST CMOS Analog Switch	IH5005	DG141		2 x SPST JFET Analog Switch
DG184	DG184		2 x DPST CMOS Analog Switch	IH5006	DG133		2 x SPST JFET Analog Switch
DG184	DG384		2 x DPST CMOS Analog Switch	IH5007	DG134		2 x SPST JFET Analog Switch
DG185	DG185		2 x DPST CMOS Analog Switch	IH5009	DG172		4 x SPST Virtual Gnd Analog Sw
DG187	DG187		2 x DPST CMOS Analog Switch	IH5010	DG172		4 x SPST Virtual Gnd Analog Sw
DG187	DG387		SPDT CMOS Analog Switch	IH5011	DG201A		4 x SPST Virtual Gnd Analog Sw
DG188	DG188		SPDT CMOS Analog Switch	IH5012	DG201A		4 x SPST Virtual Gnd Analog Sw
DG190	DG190		2 x SPDT CMOS Analog Switch	IH5013	DG172(3/4)		3 x SPST Virtual Gnd Analog Sw
DG190	DG390		2 x SPDT CMOS Analog Switch	IH5014	DG172(3/4)		3 x SPST Virtual Gnd Analog Sw
DG191	DG191		2 x SPDT CMOS Analog Switch	IH5015	DG201A(3/4)		3 x SPST Virtual Gnd Analog Sw
DG200	DG200A		2 x SPST CMOS Analog Switch	IH5016	DG201A(3/4)		3 x SPST Virtual Gnd Analog Sw
DG426	DG126		See DG126/DG184 preceding for package identification	IH5017	DGM111, DG200A, DG300, DG304		3 x SPST Virtual Gnd Analog Sw
DG464	DG164			IH5018	DGM111, DG200A, DG300, DG304		2 x SPST Virtual Gnd Analog Sw
G115	G115		6 x MOS FET Switch	IH5019	DGM111, DG200A, DG300, DG304		2 x SPST Virtual Gnd Analog Sw
G116	G116		5 x MOS FET Switch	II5020	DGM111, DG200A, DG300, DG304		2 x SPST Virtual Gnd Analog Sw
G117	G117		5 x MOS FET Switch	IH5021	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Virtual Gnd Analog Sw
G118	G118		6 x MOS FET Switch	IH5022	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Virtual Gnd Analog Sw
G119	G119		3 x Diff MOS FET Switch	IH5023	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Virtual Gnd Analog Sw
G123	G123		4 x MOS FET Switch	IH5024	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Virtual Gnd Analog Sw
G125	G125		4 x JFET Switch	IH5025	DG172		4 x SPST Positive Signal Analog Switch
G127	G127		4 x JFET Switch	IH5026	DG172		4 x SPST Positive Signal Analog Switch
G128	G128		4 x JFET Switch	IH5027	DG201A		4 x SPST Positive Signal Analog Switch
G129	G129		4 x JFET Switch	IH5028	DG201A		4 x SPST Positive Signal Analog Switch
G130	G130		4 x JFET Switch	IH5029	DG172(3/4)		3 x SPST Positive Signal Analog Switch
G131	G131		4 x JFET Switch	IH5030	DG172(3/4)		3 x SPST Positive Signal Analog Switch
G132	G132		4 x JFET Switch	IH5031	DG201A(3/4)		3 x SPST Positive Signal Analog Switch
HI-200	DG200A		2 x SPST CMOS Analog Switch	IH5032	DG201A(3/4)		3 x SPST Positive Signal Analog Switch
HI-201	DG201A		4 x SPST CMOS Analog Switch	IH5033	DGM111, DG200A, DG300, DG304		2 x SPST Positive Signal Analog Switch
HI-300	DG300		2 x SPST CMOS Analog Switch	IH5034	DGM111, DG200A, DG300, DG304		2 x SPST Positive Signal Analog Switch
HI-301	DG301		1 x SPDT CMOS Analog Switch	IH5035	DGM111, DG200A, DG300, DG304		2 x SPST Positive Signal Analog Switch
HI-302	DG302		2 x DPST CMOS Analog Switch	IH5036	DGM111, DG200A, DG300, DG304		2 x SPST Positive Signal Analog Switch
HI-303	DG303		2 x SPDT CMOS Analog Switch	IH5037	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Positive Signal Analog Switch
HI-304	DG304		2 x SPST CMOS Analog Switch	IH5038	DG200A(1/2), DG300(1/2), DG304(1/2)		SPST Positive Signal Analog Switch
HI-305	DG305		1 x SPDT CMOS Analog Switch	IH5040	DG5040		SPST CMOS Analog Switch
HI-306	DG306		2 x DPST CMOS Analog Switch	IH5041	DG5041		2 x SPST CMOS Analog Switch
HI-307	DG307		2 x SPDT CMOS Analog Switch	IH5042	DG5042		SPDT CMOS Analog Switch
HI-381	DG381		2 x SPST CMOS Analog Switch	IH5043	DG5043		2 x SPDT CMOS Analog Switch
HI-384	DG384		2 x DPST CMOS Analog Switch	IH5044	DG5044		DPST CMOS Analog Switch
HI-387	DG387		2 x SPDT CMOS Analog Switch	IH5045	DG5045		2 x DPST CMOS Analog Switch
HI-390	DG390		2 x SPDT CMOS Analog Switch	IH5046	DG185, DG302, DG306, DG384		2 x DPST CMOS Analog Switch
HI-400		DG200A	2 x SPST Analog Switch, CMOS	IH5047	DG191, DG303, DG307, DG390		DPDT CMOS Analog Switch
HI-401		DG201A	4 x SPST Analog Switch, CMOS	IH5048	DG185, DG302, DG306, DG384		4PST CMOS Analog Switch
HI-506	DG506A		16 x CMOS Analog Mux	IH5048	DG181, DG300, DG304		2 x SPST CMOS Analog Switch
HI-506A	DG506A		16 x CMOS Analog Mux				
HI-507	DG507A		8 x CMOS Diff Analog Mux				
HI-507A	DG507A		8 x CMOS Diff Analog Mux				
HI-508A	DG508A		8 x CMOS Analog Mux				
HI-509A	DG509A		4 x CMOS Diff Analog Mux				
HI-1800		DG184, DG302, DG306	2 x DPST CMOS Analog Switch				
HI-1800A		DG185, DG302, DG306	2 x DPST CMOS Analog Switch				
HI-1818		DG508A	8 x CMOS Analog Mux				
HI-1818A		DG508A	8 x CMOS Analog Mux				
HI-1828		DG509A	4 x CMOS Diff Analog Mux				
HI-1828A		DG509A	4 x CMOS Diff Analog Mux				
HI-5040	DG5040	DG182(1/2), DG200A(1/2), DG300(1/2), DG304(1/2)	SPST CMOS Analog Switch				
HI-5041	DG5041	DG182, DG200A, DG300, DG304	2 x SPST CMOS Analog Switch				
HI-5042	DG5042	DG188, DG301, DG304	SPDT CMOS Analog Switch				
HI-5043	DG5043	DG191, DG290, DG303, DG307, DG390	2 x SPDT CMOS Analog Switch				
HI-5044	DG5044	DG182, DG185(1/2), DG200A, DG300, DG302(1/2), DG304, DG306(1/2)	DPST CMOS Analog Switch				
HI-5045	DG5045	DG302, DG306	2 x DPST CMOS Analog Switch				
HI-5046		DG191, DG303, DG307	DPDT CMOS Analog Switch				
HI-5046A		DG190, DG303, DG307	DPDT CMOS Analog Switch				
HI-5047		DG185, DG302, DG306	4PST CMOS Analog Switch				
HI-5047A		DG184, DG302, DG306	4PST CMOS Analog Switch				
HI-5048		DG181, DG300, DG304	2 x SPST CMOS Analog Switch				
HI-5049	DG184	DG302, DG306, DG384	2 x DPST CMOS Analog Switch				
HI-5050		DG187, DG287, DG301, DG305	SPDT CMOS Analog Switch				

Analog Switch and ICs Cross Reference Guide (Cont'd)

Mfr's Device Number	SILICONIX DEVICE			Mfr's Device Number	SILICONIX DEVICE		
	Direct Replacement	Similar Function	Manufacturer's Description		Direct Replacement	Similar Function	Manufacturer's Description
IH5048		DG181, DG300	2 x SPST CMOS Analog Switch	MC14066	DG172, 201A	4 x SPST CMOS Analog Switch	
IH5049		DG304, DG5041		MC14529	DG508A, 509A	8 x CMOS Analog Mux	
IH5050		DG5045, DG306	2 x DPST CMOS Analog Switch	MH320	DF320	CMOS Loop Disconnect Dialer	
IH5050	DG187	DG187, DG301	SPDT CMOS Analog Switch	MK5098	DF-320	CMOS Loop Disconnect Dialer	
IH5051	DG190	DG301, DG305	2 x SPST CMOS Analog Switch	MM4504	G115, G118	6 x MOS Analog Switch	
IH5060	DG506	DG303, DG307	16 x CMOS Analog Mux	MM5504	G115, G118	6 x MOS Analog Switch	
IH5070	DG507		8 x Diff CMOS Analog Mux	MM5393	DF320	CMOS Loop Disconnect Dialer	
IH6108	DG508A		8 x CMOS Analog MUX	MCP-16S	DG508A	16 x CMOS Analog Mux	
IH6116	DG506A		16 x CMOS Analog MUX	MPC-8D	DG507A	8 x Diff CMOS Analog Mux	
IH6208	DG509A		4 x Diff Analog MUX	MPC-8S	DG508A	8 x CMOS Analog Mux	
IH6216	DG507A		8 x Diff Analog MUX	MPC-4D	DG509A	4 x Diff CMOS Analog Mux	
LF11331		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MPM-8S	DG508A	8 x MOS Analog Mux	
LF12331		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MT4320	DF320	CMOS Loop Disconnect Dialer	
LF13331		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MT4322	DF322	CMOS Loop Disconnect Dialer	
LF11332		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MUX08	DG508A	8 x CMOS Analog Mux	
LF12332		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MUX16	DG506A	16 x CMOS Analog Mux	
LF13332		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MUX24	DG509A	8 x CMOS Analog Mux	
LF11333		DG201A, 211, 308A	4 x SPST JFET Analog Switch	MUX28	DG507A	8 x Diff CMOS Analog Mux	
LF12333		DG201A, 211, 308A	4 x SPST JFET Analog Switch	NC2320	DF320	CMOS Loop Disconnect Dialer	
LF13333		DG201A, 211, 308A	4 x SPST JFET Analog Switch	NC2322	DF322	CMOS Loop Disconnect Dialer	
LF11201	DG201A		4 x SPST JFET Analog Switch	37052	SI3705	DG501	
LF12201	DG201A		4 x SPST JFET Analog Switch	37053	SI3705	DG501	
LF13201	DG201A		4 x SPST JFET Analog Switch	37062	SI3705	DG501	
LF11202	DG202		4 x SPST JFET Analog Switch	37083	SI3705	DG501	
LF12202	DG202		4 x SPST JFET Analog Switch	S2560	DF320	CMOS Loop Disconnect Dialer	
LF13202	DG202		4 x SPST JFET Analog Switch	TL182	DG182	DG281, 381	
LFXX506	DG506A	DG501	8 x CMOS Analog Mux	TL185	DG185	DG284, 384	
LFXX507	DG507A	DG511	8 x Diff CMOS Analog Mux	TL188	DG188	DG287, 387	
LFXX508	DG508A	DG170, 201A	8 x CMOS Analog Mux	TL191	DG191	DG290, 390	
LFXX509	DG509A	DG508A	4 x Diff CMOS Analog Mux	UC4250	L144(1/3)	Low Power Op Amp	
MC1150L		DG509A	4 x Diff CMOS Analog Mux	UC4252	L144(2/3)	2 x Low Power Op Amp	
MC1151L				UC4253	L144	Triple Low Power Op Amp	
MC14016							
MC14051							
MC14052							

Temperature Range and Package Cross Reference

Competitor	Temperature Range		Package	
	Competitor	Siliconix	Competitor	Siliconix
Analog Devices	A, B, C	A	DN	P, K
	J, K, L	B	F	L
	S, T, U	C	H	A
Harris	2	A	1	P, K
	4 & 9	B	2	A
	5	C	3	J
	8	A/883	9	L
Intersil	C	C	D, P	P
	I	B	F, L	L
	M	A	P	J
			T, A	A
National	C, 2	B	H	A
	3	C	N	J
	M, 1	A	F, W	L
			J, D	P, K
Precision Monolithics	—	—	K	A
	—	—	M	L
	—	—	Y, Q, X	P, K, J
Texas Instruments	C	B	T, FA, J, W,	L
	L	C	JA, JB, JP	P, K
	M	A	L, LA	A
		N, P	J	

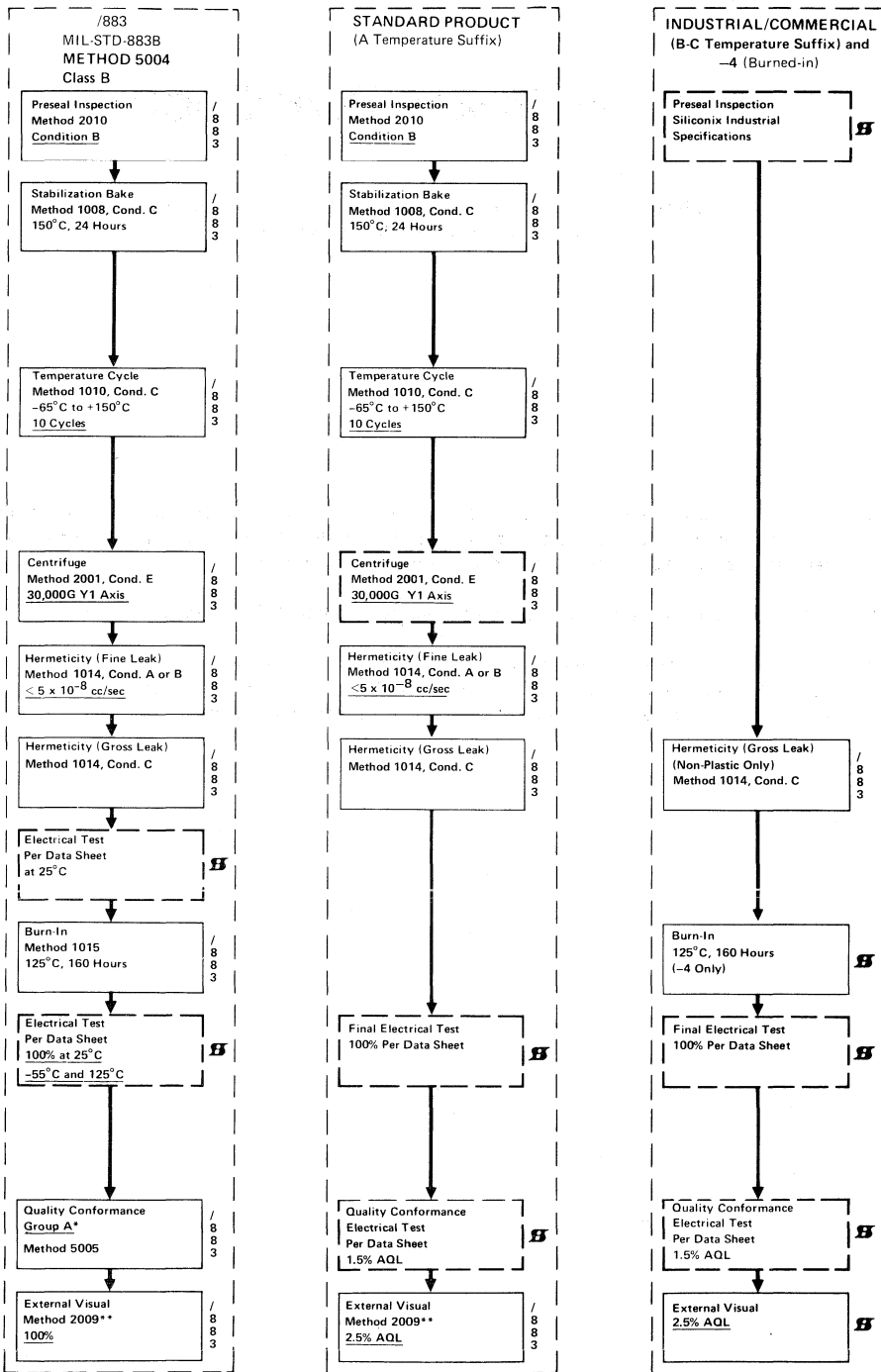
Process Option Flow Chart

The Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

- Column 1:** Denotes the screening process for MIL-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. If Group B or C Quality Conformance is also required, call out as a separate line item. Parts in this classification are carried in inventory.
- Column 2:** Is the screening procedure for military grade standard products ("A" temperature suffix).
- Column 3:** Is the normal screening procedure for industrial and commercial grade products (B and C temperature suffixes). An industrial and commercial grade product (B and C temperature range) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (-4) following the package suffix letter.

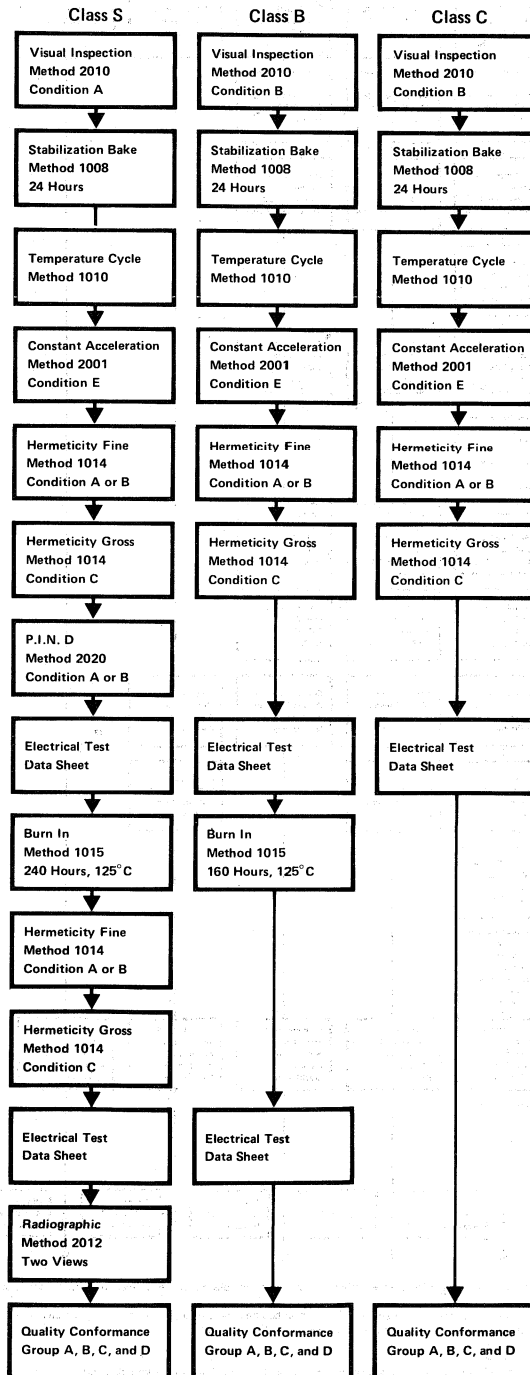
Process Option Flow Chart

Process Option Flow Chart

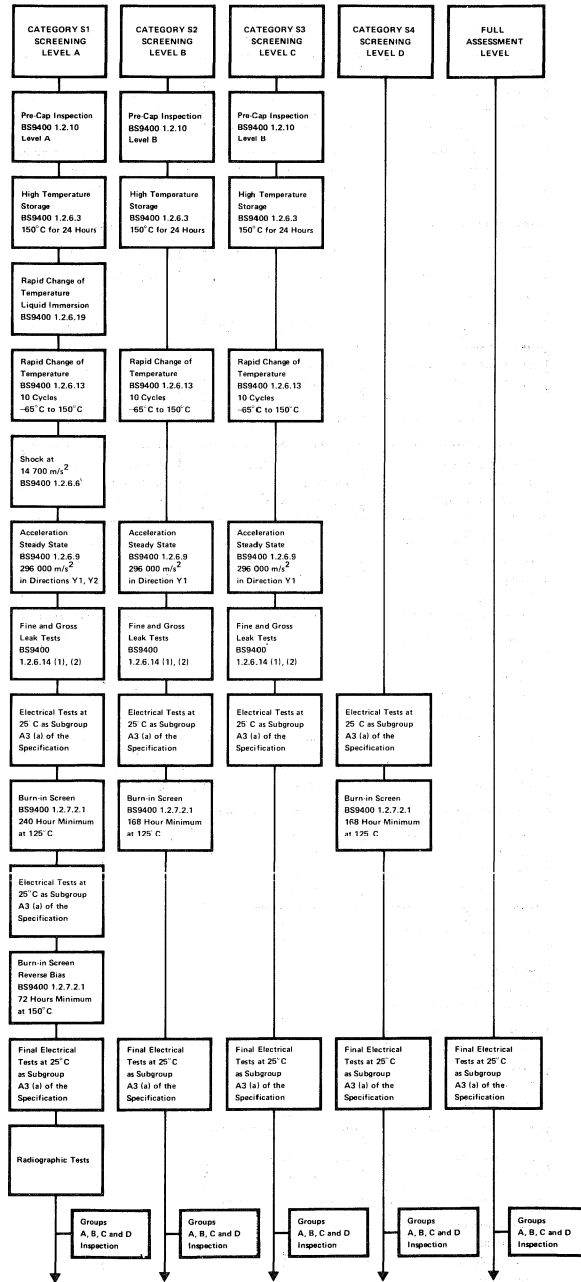


* Group B and C tests done to customer order on /883 parts
 ** Physical Dimensions Excluded
 The latest revision of MIL-STD-883 is applicable

JM38510/883 Process Option Flow Chart



BS9000 Series Process Option Flow Chart



INSPECTION REQUIREMENTS: All tests to be conducted at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise specified. Samples submitted to tests marked 'D' shall not be accepted for release under BS9000 (see 2.6.5 of BS9000 Part I).

Flow chart for 100% screening test procedures (see also Inspection Requirements). Production batches containing greater than 10% defective units subsequent to Burn-in will not be issued for release. The following acceptance/rejection criteria apply to the electrical tests after Burn-in for screening levels A, B and D.

- (a) Lots exhibiting greater than 20% defectives shall be rejected.
- (b) Lots exhibiting less than 10% defectives shall be accepted.
- (c) Lots exhibiting between 10% and 20% defectives (inclusive) shall have the defectives removed and the remainder of the lot subjected to an identical Burn-in. If such a Lot then exhibits greater than 5% defectives it shall be rejected.

Radiographic tests. Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

Introduction	1
Data Sheets	2
Selector Guides	3
Geometry	4
Application Notes	5
Appendices	6
Other Products	7
Worldwide Sales Offices	8

Worldwide Sales Offices

Manufacturing Facilities

TAIWAN

Siliconix (Taiwan) Ltd.
Nantze Export Processing Zone
Kaohsiung
Tel: 3612019
Tlx: 78571235

HONG KONG

Siliconix (H.K.) Ltd.
5/6/7th Floors
Liven House
61-63 King Yip Street
Kwun Tong, Kowloon
Tel: 3-427151
Tlx: 4449SILXHX

UNITED KINGDOM

Siliconix Ltd.
Morrison, Swansea
SA6 6NE
Tel: (0792) 74681
Tlx: 48197

UNITED STATES

2201 Laurelwood Road
Santa Clara, CA 95054
Tel: (408) 988-8000
Tlx: 910-338-0227

U.S. Sales Offices

Eastern

Siliconix Incorporated
31 Bailey Avenue
Ridgefield, CT 06877
(203) 431-3535
Tlx: 710-467-0660

Siliconix Incorporated
395 Totten Pond Rd.
Waltham, MA 02154
(617) 890-7180
Tlx: 710-324-1783

Central

Siliconix Incorporated
1327 Butterfield Rd., Suite 620
Downers Grove, IL 60515
(312) 960-0106
Tlx: 910-695-3232

Siliconix Incorporated
Two King James South, Suite 143
24650 Center Ridge Road
Westlake, OH 44145
(216) 835-4470
Tlx: 810-427-9258

Siliconix Incorporated
P.O. Box 487
3310 Keller Springs Rd.
Suite 110A
Carrollton, TX 75006
(214) 358-4046/4047

Northwestern

Siliconix Incorporated
2201 Laurelwood Rd.
Santa Clara, CA 95054
(408) 988-8000
Tlx: 910-338-0227

Southwestern

Siliconix Incorporated
1525 E. 17th St., Suite L
Santa Ana, CA 92701
(714) 547-4474
Tlx: 910-595-2643

Southeastern

Siliconix Incorporated
4431 Winderlake Dr.
Orlando, FL 32811
(305) 293-4255

International Sales Offices

EUROPEAN

FRANCE

Siliconix S.A.R.L.
70-72 Avenue Du General De Gaulle
Echat 660
94022 Creteil Cedex
Tel: (1) 377 07 87
Tlx: Siliconx 230389F

WEST GERMANY

Siliconix GmbH
Johannesstrasse 27
7024 Filderstadt-1
Postfach 1340
Tel: (0711) 702066
Tlx: 7-255 553

UNITED KINGDOM

Siliconix Ltd.
Brook House
Northbrook Street
Newbury, Berks
RG13 1AH
Tel: (0635) 47609
Tlx: 849357

Siliconix Ltd.
Morrison, Swansea
United Kingdom SA6 6NE
Tel: (0792) 74681
Tlx: 48197

FAR EAST

HONG KONG

Siliconix (H.K.) Ltd.
5th Floor
Liven House
61-63 King Yip Street
Kwun Tong, Kowloon
Tel: 3-427151
Tlx: 44449SILXHX

JAPAN

Nippon Siliconix Incorporated
101 Daigo Tanaka Bldg.
4-4 Idabashi 3-Chome
Chiyoda Ku, Tokyo 102
Tel: (03) 264-7905
Tlx: 2322739 NSIXJ

TAIWAN

Siliconix (Taiwan) Ltd.
Nantze Export Processing Zone
Kaohsiung
Tel: 3612019
Tlx: 785 712 35

Worldwide Sales Offices (Cont'd)

U.S. Sales Representatives

ALABAMA, Huntsville (35803)

Rep Incorporated
11547 S. Memorial Pkwy.
(205) 881-9270
Twx: 810-726-2102

ARIZONA, Tempe (85281)

Quatra Associates, Inc.
1801 S. Jen Tilly Lane
Suite C-14
(602) 894-2808
Twx: 910-950-1153

CALIFORNIA, Cupertino (95014)

Costar Incorporated
10080 North Wolfe Rd., Suite SW3-175
(408) 446-9339
Twx: 910-338-0206

CALIFORNIA, Fountain Valley (92708)

Bager Electronics Inc.
17220 Newhope St., #211
(714)957-3367
Twx: 910-596-2638

COLORADO, Englewood (80112)

Delta Sales Assoc.
Bldg. 8 — Penthouse F
14 Inverness Dr. E.
(303) 741-0646
Twx: 910-935-0717

CONNECTICUT, Cheshire (06410-0160)

Scientific Components
1185 South Main St.
(203) 272-2963
Twx: 710-455-2078

FLORIDA, Clearwater BCH (33515)

Perrott Associates
473 East Shore Drive
(813) 443-5214
Twx: 810-866-0328

FLORIDA, Orlando (32807)

Perrott Associates
1607 Forsyth Road
(305)275-1132
Twx: 810-850-0103

FLORIDA, Sunrise (33313)

Perrott Associates
1371 Sunset Strip
(305) 792-2211

GEORGIA, Norcross (30092)

Montgomery Marketing
3640 Peachtree Corner W., #303
(404)447-6124
Twx: 810-766-0448

ILLINOIS, Des Plaines (60018)

Electron Marketing Corp.
3166 Des Plaines Ave.
Suite 35
(312)298-2330
Twx: 910-233-0183

INDIANA, Indianapolis (46240)

Wilson Technical Sales, Inc.
P. O. Box 40999
(317) 298-3345
Twx: 810-341-3264

IOWA, Cedar Rapids (52402)

Technical Reps Incorporated
1930 St. Andrews Dr. N.E.
(319)393-1300
Twx: 910-525-1351

KANSAS, Wichita (67206)

Technical Reps Incorporated
1115 Parklane
Suite 208
(316) 681-0242

MARYLAND, Baltimore (21208)

Pro Rep
107 Sudbrook Lane
(301)653-3600
Twx: 710-862-0862

MICHIGAN, Brighton (48116)

A.P. Associates
P.O. Box 777
9880 E. Grand River Ave.
(313)229-6550
Twx: 910-242-1510

MINNESOTA, Burnsville (55337)

Electromec Sales Inc.
101 W. Burnsville Pkwy.
(612) 894-8200
Twx: 910-576-0233

MISSOURI, Earth City (63045)

Technical Reps Inc.
502 Earth City Plaza, #201
(314)291-0001
Twx: 910-762-0685

MISSOURI, Kansas City (64111)

Technical Reps Incorporated
406 W. 34th, #616 VFW Bldg.
(816) 756-3575
Twx: 910-771-0025

NEBRASKA, Lincoln (68502)

Technical Reps Inc.
3100 N. 14th St., Suite 21
(402) 475-2115

NEW HAMPSHIRE, Nashua (03063)

Comp Tech Incorporated
491 Amherst St.
(603) 883-9380
Twx: 710-228-1491

NEW JERSEY, Marlton (08053)

B.G.R. Associates
3001 Greentree Exec. Campus
(609)428-2440
Twx: 710-940-1358

NEW JERSEY, Teaneck (07666)

R.T. Reid Associates
705 Cedar Lane
(201)692-0200
Twx: 710-990-5086

NEW YORK, Endwell (13760)

Tri-Tech Electronics, Inc.
2215 E. Main St.
(607)754-1094
Twx: 510-252-0891

NEW YORK, Fairport (14450)

Tri-Tech Electronics, Inc.
590 Perinton Hills Office Park
(716)223-5720
Twx: 510-253-6356

NEW YORK, Fayetteville (13066)

Tri-Tech Electronics, Inc.
6836 E. Genesee St.
(315)446-2881
Twx: 710-393-6552

NY City, Ll. See Teaneck, NJ

NEW YORK, Poughkeepsie (12603)

Tri-Tech Electronics, Inc.
19 Davis Ave.
(914)473-3880

NORTH CAROLINA, Cary (27511)

Montgomery Marketing
P.O. B. 520 (1391 N. Harrison Ave.)
(919)467-6319
Twx: 510-920-0634

OHIO, Cleveland (44143)

Arthur H. Baier Company
67 Alpha Park
(216)461-6161
Twx: 810-427-9278

OHIO, Dayton (45414)

Arthur H. Baier Company
4940 Profit Way
(513)276-4128
Twx: 810-459-1624

OREGON, Beaverton (97005)

Blair Hirsch Co., Inc.
9645 S.W. Beaverton Hwy.
(503)641-1875

TENNESSEE, Jefferson City (37760)

Rep Incorporated
P.O. B. 287 (113 So. Branner Ave.)
(615)475-4105
Twx: 810-570-4203

TEXAS, Austin (78753)

Electronics Marketing Assoc.
607A Deen Avenue
(512)837-0893

TEXAS, Grapevine (76051)

Electronics Marketing Assoc.
P.O. Box 487
(403 E. Wall)
(817)481-7502 or 7503
Twx: 910-890-8659

TEXAS, Houston (77099)

Electronics Marketing Assoc.
P.O. Box 42388
(1450 Bissonnet, #309)
(713) 498-8120

UTAH, Salt Lake City (84115)

Delta Sales Associates
1800 Southwest Temple, Ste. 405
(801) 487-7571

WASHINGTON, Lynnwood (98036)

Blair Hirsch Co., Inc.
P.O. Box 2250
19410 36th Avenue West
Suite 106
(206) 774-8151

WISCONSIN, Milwaukee (53227)

JM Sales
9431 W. Belmont Road, Suite 119
(414)546-0040

WISCONSIN, Wauwatosa (53226)

Larsen Associates
10855 West Potter Rd.

U.S. CHIP DISTRIBUTORS**FLORIDA, Orlando (32807)**

Chip Supply Inc.
1607 Forsyth Road
(305)275-3810
Twx: 810-850-0103

PENNSYLVANIA, Malvern (19335)

Hybrid Die Technology
111 Great Valley Pkwy.
(215)296-5905
Twx: 510-668-6123

Worldwide Sales Offices (Cont'd)

U.S. Distributors

ALABAMA, Huntsville (35805)

Bell Industries
1130 Commercial Drive
(205)837-7210
Twx: 810-726-2162

ALABAMA, Huntsville (35805)

Pioneer/Huntsville
1207 Putman Dr. NW
(205)837-9300
Twx: 810-726-2197

ARIZONA, Tempe (85281)

Hamilton/Avnet, #04
505 South Madison Dr.
(602)894-9600
Twx: 910-950-0077

CALIFORNIA, Anaheim (92807)

Zeus West, Inc.
1130 Hawk Circle
(714) 632-6880

CALIFORNIA, Chatsworth (91311)

Anthem Electronics, Inc.
21730 Nordhoff St.
(213) 700-1000

CALIFORNIA, Costa Mesa (92626)

Avnet Elec.
350 McCormick Ave
(714)754-6111
Twx: 910-595-1928

CALIFORNIA, Costa Mesa (92626)

Hamilton Electro Sales, #29
3170 Pullman St.
(714)641-4100
Twx: 910-595-2638

CALIFORNIA, Culver City (90230)

Hamilton Electro Sales, #01
10912 W. Washington Bl.
(213)558-2121 or (714)522-8200
Twx: 910-340-6364

CALIFORNIA, San Diego (92121)

Anthem Electronics, Inc.
4125 Sorrento Valley Blvd.
(714)453-9005
Twx: 910-335-1515

CALIFORNIA, San Diego (92123)

Hamilton/Avnet
4545 Viewridge Ave.
(714)571-5710
Twx: 910-335-1216

CALIFORNIA, Santa Clara (95052)

Wyle Distribution Group
3000 Bowers Ave.
(408)727-2500
Twx: 910-379-6480

CALIFORNIA, Sunnyvale (94086)

Bell Industries
1161 No. Fair Oaks Ave.
(408)734-8570
Twx: 910-339-9378

CALIFORNIA, Sunnyvale (94086)

Wyle Distribution Group
1175 Bordeaux Avenue
(408) 743-3300
Twx: 910-339-9332

CALIFORNIA, Tustin (92680)

Anthem Electronics, Inc.
2851 Dow Avenue
(714)730-8000
Twx: 910-595-1585

COLORADO, Englewood (80111)

Hamilton/Avnet, #06
8765 E. Orchard Rd., Suite 708
(303)740-1000
Twx: 910-931-0510

COLORADO, Thornton (80241)

Wyle Distribution Group
451 E. 124th Ave.
(303)457-9953
Twx: 910-936-0770

COLORADO, Wheatridge (80033)

Bell Industries
8155 W. 48th Ave.
(303)424-1985
Twx: 910-938-0393

CONNECTICUT, Danbury (06810)

Hamilton/Avnet, #21
Commerce Drive, Commerce Park
(203)797-2800
Twx: 710-460-0594

CONNECTICUT, Wallingford (06492)

Marshall Industries
Village Lane
Barnes Industrial Park
(203)265-3622
Twx: 710-465-0747

FLORIDA, Ft. Lauderdale (33309)

Hamilton/Avnet, #17
6801 N.W. 20th Way
(305)971-2900
Twx: 510-955-3097

FLORIDA, Orlando (32809)

Pioneer Elec.
6220 S. Orange Blossom Trail, Ste. 412
(305)859-3600
Twx: 810-850-0177

FLORIDA, St. Petersburg (33702)

Hamilton/Avnet, #25
3197 Tech Drive No.
(813)576-3930
Twx: 810-863-0374

GEORGIA, Norcross (30092)

Hamilton/Avnet
5825 Peachtree Corners, E-D
(404)447-7500
Twx: 810-766-3969

GEORGIA, Norcross (30093)

Marshall Industries
4364B Shakelford Rd.
(404)923-5750
Twx: 810-766-3969

ILLINOIS, Bensenville (60106)

Hamilton/Avnet, #10
1130 Thorndale Ave.
(312)678-6310
Twx: 910-227-0060

ILLINOIS, Elk Grove Village (60007)

Pioneer/Chicago
1551 Carmen Drive
(312)437-9680
Twx: 910-222-1834

INDIANA, Carmel (46032)

Hamilton/Avnet, #28
485 Gradle Drive
(317)844-9333
Twx: 810-260-3966

INDIANA, Indianapolis (46250)

Pioneer/Indiana
6408 Castlepine Drive
(317)849-7300
Twx: 810-260-1794

KANSAS, Overland Park (66215)

Hamilton/Avnet
9219 Quivira Rd.
(913)888-8900
Twx: 910-743-0005

MARYLAND, Columbia (21046)

Hamilton/Avnet, #12
6822 Oak Hall Lane
(301)995-3500(MD)
(301)621-5410(DC)
Twx: 710-862-1861

MARYLAND, Gaithersburg (20760)

Pioneer/Washington
9100 Gaitner Rd.
(301)948-0710
Twx: 710-828-0545

MARYLAND, Gaithersburg (20760)

Marshall Industries
16760 Oakmont Ave.
(301)840-9450
Twx: 710-828-0223

MASSACHUSETTS, Burlington (01803)

Milgray Electronics
79 Terrace Hall Ave.
(617)272-6800
Twx: 510-225-3673

MASSACHUSETTS, Burlington (01803)

Marshall Industries
1 Wilshire Road
(617)272-8200
Twx: 710-332-6359

MASSACHUSETTS, Woburn (01801)

Hamilton/Avnet, #18
50 Tower Office Park
(617)953-9700
Twx: 710-393-0382

MICHIGAN, Livonia (48150)

Hamilton/Avnet, #66
32487 Schoolcraft
(313)522-4700
Twx: 810-242-8775

MICHIGAN, Livonia (48150)

Pioneer/Michigan
13485 Stamford
(313)825-1800
Twx: 810-242-3271

MINNESOTA, Minneapolis (55435)

Industrial Components
5229 Edina Industrial Blvd.
(612)831-2666
Twx: 910-576-3153

MINNESOTA, Minnetonka (55343)

Hamilton/Avnet
10300 Bren Rd. East
(612)932-0600
Twx: 910-576-2729

MINNESOTA, Minnetonka (55343)

Pioneer/Twin Cities
10203 Bren Rd. East
(612)935-5444

MINNESOTA, Plymouth (55441)

Marshall Industries
13810 24th Avenue, No.
Suite 460
Twx: 910-576-2729

MISSOURI, Earth City (63045)

Hamilton/Avnet
13743 Shoreline Ct.
(314)344-1200
Twx: 910-762-0606

NEW HAMPSHIRE, Nashua

Comp Tech, Inc.
491 Amherst St.
(603) 883-9380
Tix: 710-228-1491

NEW JERSEY, Cherry Hill (08003)

Hamilton/Avnet, #14
One Keystone Ave.
(609)424-0100
Twx: 710-940-0262

NEW JERSEY, Clifton (07015)

Marshall Industries
1111 Paulison Ave.
(201)340-1900
Twx: 710-989-7052

NEW JERSEY, Fairfield (07006)

Hamilton/Avnet, #19
10 Industrial Rd.
(201)575-3390
Twx: 710-734-4388

NEW JERSEY, Mt. Laurel (08057)

Marshall Industries
102 Gaitner Dr., Unit 2
(609)234-9100 NJ (215)627-1920 PA
Twx: 710-941-1361

NEW MEXICO, Albuquerque (87123)

Alliance Electronics
11030 Cochiti S.E.
(505)293-3360
Twx: 910-989-1151

NEW MEXICO, Albuquerque (87123)

Bell Industries
11728 Linn NE
(505)292-2700
Twx: 910-989-0625

NEW MEXICO, Albuquerque (87119)

Hamilton/Avnet, #22
2524 Baylor Dr., SE
(505)765-1500
Twx: 910-989-0614

NEW YORK, Buffalo (14202)

Summit Distributors, Inc.
916 Main Street
(716)887-2800
Twx: 710-522-1692

NEW YORK, East Syracuse (13057)

Hamilton/Avnet, #8
1600 Corporate Circle
(315)437-2642
Twx: 710-541-1560

NEW YORK, Endwell (13760)

Marshall Industries
10 Hooper Road
(607)754-1570
Twx: 510-252-0194

NEW YORK, Freeport (11520)

Milgray Electronics, Inc.
191 Hansa Ave.
(516)546-5600
Twx: 516-546-5600

NEW YORK, Hauppauge (11787)

Harvey Military/Components Plus
40 Oser Ave.
(516)231-9200
Twx: 510-227-9869

NEW YORK, Hauppauge (11787)

Marshall Industries
275 Oser Avenue
(516) 273-2424
Twx: 510-224-6109

NEW YORK, Melville (11747)

Hamilton/Avnet, #20
5 Hub Drive
(516)454-6000
Twx: 510-224-6166

NEW YORK, Port Chester (10573)

Zeus Components, Inc.
100 Midlin Ave.
(914)937-7400
Twx: 710-567-1248

NEW YORK, Rochester (14623)

Hamilton/Avnet, #61
333 Metro Park
(716)475-9130
Twx: 510-253-5470

NEW YORK, Rochester (14623)

Marshall Industries
1260 Scottsville Rd.
(716)235-7620
Twx: 510-253-5470

NORTH CAROLINA, Greensboro (27406)

Pioneer/NC
103 Industrial Ave.
(919)273-4441
Twx: 510-925-1114

NORTH CAROLINA, Raleigh (27609)

Hamilton/Avnet
2803 Industrial Dr.
(919)829-8030
Twx: 510-928-1836

OHIO, Cleveland (44105)

Pioneer/Cleveland
4800 E. 131st Street
(216)587-3600
Twx: 810-422-2210

Worldwide Sales Offices (Cont'd)

U.S. Distributors (Cont'd)

OHIO, Dayton (45459)

Hamilton/Avnet, #64
954 Senate Dr.
(513)433-0610
Twx: 810-450-2531

OHIO, Dayton (45424)

Pioneer/Dayton
4433 Interpoint Blvd.
(513)236-9900
Twx: 810-459-1622

OHIO, Warrensville Heights (44128)

Hamilton/Avnet, #62
4588 Emery Industrial Parkway
(216)831-3500
Twx: 810-427-9452

OKLAHOMA, Tulsa (74129)

Quality Components
9934 E. 21st St. South
(918)664-8812

OREGON, Lake Oswego (97034)

Hamilton/Avnet, #27
6024 SW Jean Road, Bldg. C, Ste. 10
(503)635-8836
Twx: 910-455-8179

PENNSYLVANIA, Horsham (19044)

Pioneer Elec.
261 Gibraltar Rd.
(215)674-4000
Twx: 510-665-6778

PENNSYLVANIA, Pittsburgh (15238)

Pioneer/Pittsburgh
259 Kappa Dr.
(412)782-2300
Twx: 710-795-3122

TEXAS, Addison (75001)

Quality Components
4257 Kellway Circle
(214)387-4949
Twx: 910-860-5459

TEXAS, Austin (78758)

Hamilton/Avnet, #26
2401 Rutland Dr.
(512)837-8911
Twx: 910-874-1319

TEXAS, Austin (78758)

Harrison Equipment Co., Inc.
8910-A1 Research Blvd.
(512) 458-3555

TEXAS, Austin (78758)

Quality Components
2427 Rutland Drive
(512)835-0220
Twx: 910-874-1377

TEXAS, Dallas (75234)

Harrison Equipment Co., Inc.
14282 Gillis Rd.
(214) 239-2750

TEXAS, Houston (77063)

Hamilton/Avnet, #11
8750 Westpark
(713)780-1771
Twx: 910-481-5523

TEXAS, Houston (77036)

Quality Components
6126 Westline
(713)772-7100

TEXAS, Irving (75062)

Hamilton/Avnet, #16
2111 W. Walnut Hill Lane
(214)659-4151
Twx: 910-860-5929

TEXAS, Stafford (77477)

Harrison Equipment Co., Inc.
11100 W. Airport Blvd.
(713) 879-2771

UTAH, Salt Lake City (84119)

Hamilton/Avnet, #09
1585 West 2100 South
(801)972-2800
Twx: 910-925-4018

WASHINGTON, Bellevue (98000)

Hamilton/Avnet, #07
14212 NE 21st St.
(206)453-5844
Twx: 910-443-2464

WASHINGTON, Bellevue (98005)

Wyle Distribution Group
1750 - 132nd Ave. NE
(206)453-8300
Twx: 910-443-2526

WISCONSIN, Milwaukee (53214)

Marsh Electronics, Inc.
1563 So. 101st St.
(414)475-6000
Twx: 910-262-3321

WISCONSIN, New Berlin (53115)

Hamilton/Avnet, #57
2975 Moorland Rd.
(414)784-4510
Twx: 910-262-1182

European Distributors/Representatives

AUSTRIA

Ing. Ernest Steiner
Hummelgasse 14
A-1130 Vienna
Tel: 0222/827474
Tlx: 135026

BELGIUM

Belram S.A.
83 Avenue Des Mimosas
1150 Brussels

For the distributor's
address, contact our
Siliconix sales office
in West Germany

DENMARK

Ditz Schweitzer A.S.
Valien sboekvej 41
DK-2600 Glostrup
Tel: (02)45-30-44
Tlx: 33257

FINLAND

Oy Findip AB
Teollisuustie 7, P.O. B. 34
SF 02700 Kauniainen
Tel: 358-0-5952255
Tlx: 12-3129

FRANCE

Almex
48 Rue de L'Aubepine
92160 Antony Cedex.
Tel: 666-21-12
Tlx: 250067

Alrodis

40 Rue Villon
69008 Lyon
Tel: (78)00.87.12
Tlx: 380636

Composants S. A.
Avenue Gustave Eiffel
B. P. 81
33605 Pessac Cedex
Tel: (56)36.4040
Tlx: 550696F

Composants S. A.
55 Avenue Louis Breguet
31400 Toulouse
Tel: (61)20.82.38

Composants S. A.
183 Route de Paris
86000 Poitiers
Tel: (49)88.60.50
Twx: 791525F

A. Baltzinger
18-26 Route Du gen De Gaulle
B.P. 63
67042 Strasbourg Cedex
Tel: (88)331852
Tlx: 870952F

Composants S. A.
57 Rue Manoir de Servigne
Z1, Route de Lorient
B. P. 3209
35000 Rennes Cedex
Tel: (99)54.01.53
Tlx: 740311

Sanellec Electronique
7 Rue de la Couture
Z1, de la Pilaterie
59700 Marca-en-Baroeuil
Tel: (20)96-92-13
Tlx: 160 143F

SCAIB
80 Rue d'Arcueil
94523 Rungis Cedex
Tel: 687-23-13
Tlx: 204 674F

GERMANY

Ditronic GmbH
IM Asemwald 48
7000 Stuttgart 70
Tel: (0711)724844. 722079
Tlx: 07-255638

Ing. Buro K.H. Dreyer
Fiensburger Strasse 3
2380 Schleswig
Tel: (0462)24055
Tlx: 02-21334

Ing. Buro K.H. Dreyer
Albert Schweitzer - Ring 36
2000 Hamburg 70
Tel: (040)669027
Tlx: 2164484

EBV Elektronik GmbH
Oberweg 5
D-8025 Unterhaching
Tel: 089-61105-1
Tlx: 05-24535

EBV Elektronik GmbH
Alexanderstrasse 42
7000 Stuttgart 1
Tel: (0711)247481
Tlx: 07-22271

EBV Elektronik GmbH
Ostrasse 129
4000 Dusseldorf
Tel: (0211)84846/7
Tlx: 08-587267

EBV Elektronik GmbH
Kiebitzrain 18
3006 Burgwedel 1/Hannover
Tel: (05139)5038
Tlx: 09 23694

EBV Elektronik GmbH
Schenckstr 99
6000 Frankfurt M.90
Tel: 0611/785037
Tlx: 04-13590

Ing. Buro Rainer Konig
Königsbergerstrasse 16A
1000 Berlin 45
Tel: 030 772 8009
Tlx: 184 707

Iv-electronic
Klaus Vespermann Kg
Bachstrasse 30a
6380 Bad Homburg v.d.H.
Tel: (06172)23061-5
Tlx: 0415864

Ultronik GmbH
Munchner Strasse 6
8031 Oberaiting-Seefeld
Tel: (08152)7773
Tlx: 05-26459

GREECE

General Electronics, Ltd.
209 Thevon St.
Nikaia, Piraeus
Tel: (1) 491 35 95 or
(1) 491 10 56
Tlx: 212949 GELT GR

General Electronics Ltd.
6 Skoutis St.
Athens 136
Tel: (1) 490 69 98
Tlx: 219250 RETE GR

HOLLAND

Datron B.V.
P.O. Box 75
1243ZM S-Graveland
Netherlands

Koning en Harman Elektrotechnik BV
Postbus 43220, 30 Koperwerf
2504 A E The Hague
Koperwerf 30
Tel: 070-210101
Tlx: 31528

Tektronix Holland N.V.
P.O. Box 526
Heerenveen,
Netherlands

IRELAND, REP. of

E. I. Co. Ltd.
Shannon Airport
Co. Clare

ITALY

Adelsy S.P.A.
Via Novara 570
21053 Milano

Dott. Ing. Giuseppe DeMico S.P.A.
Via Manzoni 31
20121 Milano
Tel: (02)9520551
Tlx: 330869

NORWAY

A. S. Kjell Bakke
Ovre Raelingsvei 20
P.O. Box 27
N-2001 Lillesstrom
Tel: (02) 83 02 20

PORTUGAL

Telectra S.A.R.L.
Rua Rodrigo da Fonseca 103
1000 Lisbon
Tel: 68.60.72
Tlx: 42827

Worldwide Sales Offices (Cont'd)

European Distributors/Representatives (Cont'd)

SOUTH AFRICA

Electrolink (PTY) Ltd.
P.O. Box 1020
Cape Town 8000
Tel: 215 350
Tlx: 572 732

SPAIN

Comercial Espanola Componentes S.A.
Calle Arzobispo
Morcillo 24 Oficinas
Madrid 34
Tel: 1 250 6687
Tlx: 47010 ECCE E

Redis Logar SA
Casanova 56
Barcelona 11
Tel: 2549048

Redis Logar SA
Lopez de Hoyos,
78 DPDO, Madrid 2
Tel: 4113561
Tlx: 23967

SWEDEN

Komponentbolaget NAXAB
Box 4115
171 04 Solna
Tel: 08 995140
Tlx: 17912 KOMP

SWITZERLAND

Abelec A.G.
CH-8116 Würenlos
Landstrasse 78
Tel: 01-730-0455
Tlx: 59834

UNITED KINGDOM

Abercorn Electronics Ltd.
Abercorn House, 3 Pittville St.
Edinburgh, Scotland
Tel: 031 669 6479

Bartec Ltd.
Foundry Road, Horsham
West Sussex RH13 5PX
Tel: 0403-51881
Tlx: 87722

Dage Eurosem Ltd.
Rabans Lane
Aylesbury
Bucks HP19 3RG
Tel: 0296-32881
Tlx: 83518

Hartech Ltd., Smugglers Lane
Bosham, Nr. Chichester, Sussex
Tel: (0243)573164
Tlx: 86230

Macro-Marketing Ltd.
Burnham Lane,
Slough, Berks
Tel: (06286)4422
Tlx: 847945

Semiconductor Specialists (UK) Ltd.
Carroll House
159 High Street
West Drayton
Middlesex UB7 7XB
Tel: (08954)45522/46415
Tlx: 21958

YUGOSLAVIA

Belram S.A.
83 Avenue des Mimosas
1150 Brussels, Belgium
Tel: 734 33 32 734 26-19
Tlx: 21790

Canadian Distributors/Representatives

DISTRIBUTORS OF CANADA

BRITISH COLUMBIA

Burnaby (V5G 4J7)
RAE Industrial Elec. Ltd.
3455 Gardner Court
(604) 291-8866
Tlx: 04-356533
Twx: 610-929-3065

ONTARIO, Mississauga (L4V 1M5)

Hamilton/Avnet, #59
6845 Rexwood Dr.
(416) 677-7432
Twx: 610-492-8867

ONTARIO, Ottawa (K2C 3P2)

Future Elec.
Baxter Centre
1050 Baxter Rd.
(613) 820-8313

ONTARIO, Nepean (K2E 7L5)

Hamilton/Avnet, #60
2110 Colonnade Road
(613) 226-1700
Tlx: 0534971

ONTARIO, Downsview (M3H 5S9)

Future Electronics
4800 Dufferin St.
(416) 663-5563

QUEBEC, Pointe Claire (H9R 5C7)

Future Elec.
237 Hymus Blvd.
(514) 731-7441
Twx: 610-421-3251

QUEBEC, St. Laurent (H4S 1M2)

Hamilton/Avnet, #65
2670 Sabourin St.
(514) 331-6443
Twx: 610-421-3731

REPRESENTATIVES OF CANADA

ISLINGTON, ONTARIO M9B 6E3

Pipe Thompson, Ltd.
5468 Dundas St., West Suite 206
(416) 236-2355
Twx: 610-492-4367

NORTH GOWER, ONTARIO K0A 2T0

Pipe Thompson, Ltd.
Rural Route #2
(613) 258-4067
Twx: 610-492-4367

Worldwide Sales Offices (Cont'd)

Other International Distributors/Representatives

AUSTRALIA

STC Cannon Components PTY. LTD.
248 Wickham Road - P.O. Box 62
Moorabbin, Victoria 3189
Tel: Melbourne 555-1566
Tlx: Melbourne AA 30877
Cable: CANNONLEC - MELBOURNE

BRAZIL

Cosele Comercio e Servicos
Electronicos Ltda
Rua Da Consolacao, 867
01310 Sao Paulo
Tel: 255-1733
Tlx: 1130869-CSEL-BR

INDIA

Zenith Electronics
541 Panchratna
Mama Parmanand Marg
Bombay 400004
Tel: 384214
Tlx: 011-3152

Authorized U.S. Agent:
Fegu Electronics Inc.
3308 Middlefield Rd.
Palo Alto, CA 94306
Tel: (415)493-1788
Tlx: 345599

ISRAEL

Telsys Ltd.
12, Kehilat Venetsia St.
Tel Aviv
Tel: 482126-7-8
Tlx: 032392

JAPAN

Teijin Advanced Products Corp
1-1 Uchisaiwai-cho, 2-Chome
Chiyoda-Ku, Tokyo, 100
Tel: (03)506-4670
Tlx: J-23548

KOREA

Exim Co. Ltd.
155-12 Yumri-Dong,
Mapo-Ku
Seoul
Tel: 715-4933
Tlx: BROXIM K25253

LATIN AMERICA

Intetra Inc.
2629 Terminal Blvd.
Mt. View, CA 94043
Tel: (415)967-8818
Tlx: 345545 Intetra MNTV
Cable: INTECTRA

MALAYSIA

Carter Semiconductor
(M.) SDN. Berhad
Jalan Lapangan Terbang
Ipoh, Perak
Tel: 513400
Tlx: MA44050
Cable: CARXISTOR IPOH

NEW ZEALAND

S.T.C. Auckland
10 Margot St.
Epsom, Auckland 3
Tel: 500-019
Tlx: NZ21888

PHILIPPINES

Alexan Commercial
812 Elicano St
P.O. Box 4459, Manila
Tel: 405923
Tlx: 27484

Dynamics, Inc.

FTI Complex,
Taguig, Metro Manila

Stanford Microsystems, Inc.

FCI Building
416 Dasmarias 4 St.
Manila

SINGAPORE & MALAYSIA

Carter Semiconductor PTE. Ltd.
807, 8th Floor Front Block
Orchard Road, Orchard Towers
Tel: 235 6653
Tlx: RS 36443

Reliability Singapore PTE Ltd

26, Kallang Place
Blk 7, Unit 3F
Singapore 12

SOUTH AFRICA

ElectroLink (Pty) Ltd.
P.O. Box 1020
Cape Town 8000
Tel: 215-350
Tlx: 572-7320

TAIWAN

Don Business Corp. 3 FL
354 Chang Chung Rd.
Taipei
Tel: 571-2911
Tlx: 25641 DONBC
Cable: "DONBC" TAIPEI

THAILAND

Choakchai Electronic Supplies
128/22 Thanon Atsadang
Bangkok 2
Tel: 221-0432-221-5384
Cable: SAHAIPHAT

VENEZUELA

P. Benavides S.R.L.
Avitinas a Rio Edificio
Rio Caribe, Local 9
Caracas
Tel: 52 92 97
Tlx: 21801 PBTH



small signal
FET design catalog
November 1982